

Low-Jitter Precision LVPECL Oscillator

Features

- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ± 10 ppm, ± 20 ppm, ± 25 ppm, ± 50 ppm
- Wide Temperature Range
 - Ext. Industrial: -40°C to $+105^{\circ}\text{C}$
 - Industrial: -40°C to $+85^{\circ}\text{C}$
 - Ext. Commercial: -20°C to $+70^{\circ}\text{C}$
- High Supply Noise Rejection: -50 dBc
- Wide Frequency Range: 2.3 MHz to 460 MHz
- Small Industry Standard Footprints:
 - 2.5 mm $\times$ 2.0 mm, 3.2 mm $\times$ 2.5 mm, 5.0 mm $\times$ 3.2 mm, and 7.0 mm $\times$ 5.0 mm
- Excellent Shock and Vibration Immunity
 - Qualified to MIL-STD-883
- High Reliability
 - 20x Better MTF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25V to 3.63V
- Standby and Output Enable Function
- Lead Free and RoHS Compliant
- LVDS and HCSL Versions Available

Applications

- Storage Area Networks
 - SATA, SAS, Fibre Channel
- Passive Optical Networks
 - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video and Surveillance

General Description

The DSC1102 and DSC1122 series of high performance oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1102 has a standby feature allowing it to completely power down when EN pin is pulled low; whereas for DSC1122, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the smallest 2.5 mm $\times$ 2.0 mm, and are drop-in replacements for standard 6-lead LVPECL quartz crystal oscillators.

Block Diagram

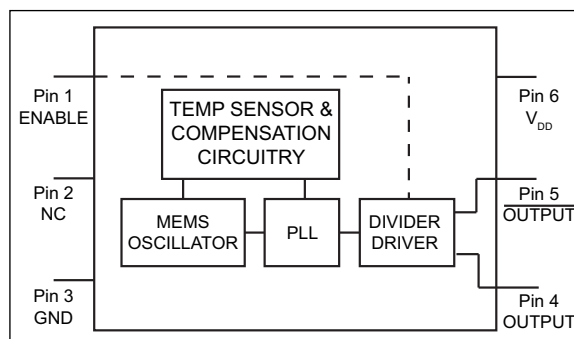


TABLE 1: OUTPUT ENABLE MODES

EN Pin	DSC1102	DSC1122
High	Outputs Active	Outputs Active
NC	Outputs Active	Outputs Active
Low	Standby	Outputs Disabled

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage	–0.3V to +4.0V
Input Voltage	–0.3V to $V_{DD} + 0.3V$
ESD Protection (HBM)	4 kV
ESD Protection (MM)	400V
ESD Protection (CDM)	1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Specifications: $V_{DD} = 3.3V$; $T_A = +25^{\circ}C$ unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.63	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSC1102, EN pin low, Output is disabled
		—	20	22		DSC1122, EN pin low, Output is disabled
Frequency Stability	Δf	—	—	± 10	ppm	Includes frequency variation due to initial tolerance, temp., and power supply voltage.
		—	—	± 20		
		—	—	± 25		
		—	—	± 50		
Aging - First Year	Δf_{Y1}	—	—	± 5	ppm	One year at $+25^{\circ}C$
Aging - After First Year	Δf_{Y2+}	—	—	$< \pm 1$	ppm/yr	Year two and beyond at $+25^{\circ}C$
Start-up Time (Note 2)	t_{SU}	—	—	5	ms	$T = +25^{\circ}C$
Input Logic Levels	V_{IH}	$0.75 \times V_{DD}$	—	—	V	Input logic high
	V_{IL}	—	—	$0.25 \times V_{DD}$		Input logic low
Output Disable Time (Note 3)	t_{DA}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSC1102
		—	—	20	ns	DSC1122
Enable Pull-Up Resistor (Note 4)	R_{PU}	—	40	—	k Ω	Pull-up resistor exists
LVPECL Outputs						
Supply Current	I_{DD}	—	56.5	58	mA	Output Enabled, $R_L = 50\Omega$
Output Logic Levels	V_{OH}	$V_{DD} - 1.08$	—	—	V	Output logic high, $R_L = 50\Omega$
	V_{OL}	—	—	$V_{DD} - 1.55$		Output logic low
Peak-to-Peak Output Swing	—	—	800	—	mV	Single-Ended

Note 1: Pin 6 V_{DD} should be filtered with a 0.1 μF capacitor.

2: t_{SU} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures below define the parameters.

4: Output is enabled if pad is floated or not connected.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Specifications: $V_{DD} = 3.3V$; $T_A = +25^\circ C$ unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Transition Time (Note 3)	t_r	—	250	—	ps	Rise time, 20% to 80%
	t_f					Fall time, $R_L = 50\Omega$, $C_L = 0$ pF
Frequency	f_0	2.3	—	460	MHz	—
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter	J_{PER}	—	2.5	—	ps _{RMS}	—
Integrated Phase Noise	J_{PH}	—	0.25	—	ps _{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.38	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz

- Note 1:** Pin 6 V_{DD} should be filtered with a 0.1 μF capacitor.
- 2:** t_{SU} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.
- 3:** Output Waveform and Test Circuit figures below define the parameters.
- 4:** Output is enabled if pad is floated or not connected.

TEMPERATURE SPECIFICATIONS

(Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-20	—	+70	°C	Ordering Option E
		-40	—	+85	°C	Ordering Option I
		-40	—	+105	°C	Ordering Option L
Max. Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	-55	—	+150	°C	—
Soldering Temperature	—	—	—	+260	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

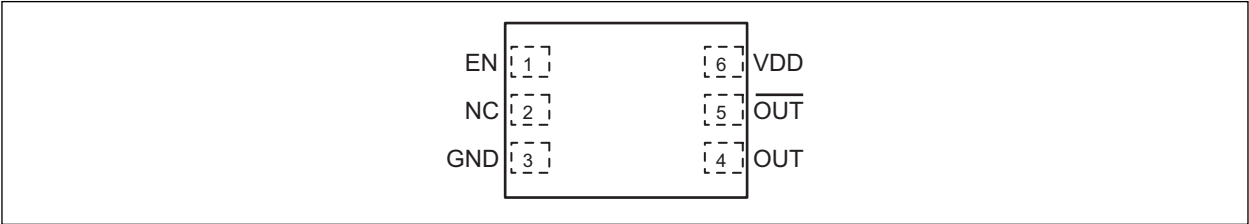


FIGURE 2-1: Pin Configuration, 6-Lead VDFN

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	EN	Enable or Standby.
2	NC	Leave unconnected or connect to ground.
3	GND	Ground.
4	OUT	Output.
5	$\overline{\text{OUT}}$	Complementary Output.
6	VDD	Supply Voltage.

3.0 NOMINAL PERFORMANCE PARAMETERS

Unless specified otherwise, T = +25°C, V_{DD} = 3.3V.

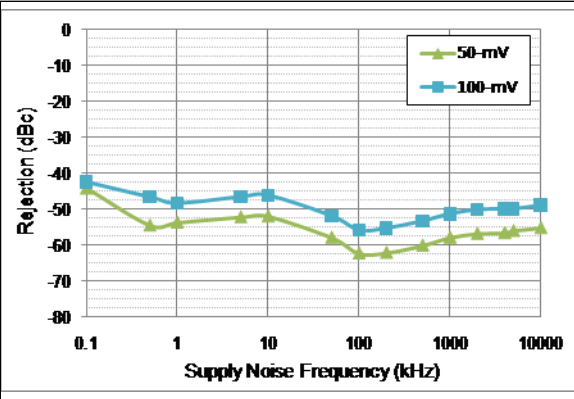


FIGURE 3-1: Power Supply Rejection Ratio.

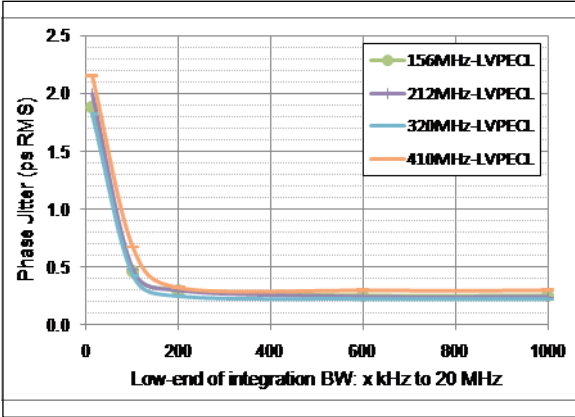


FIGURE 3-2: Phase Jitter (Integrated Phase Noise).

3.1 Output Waveform

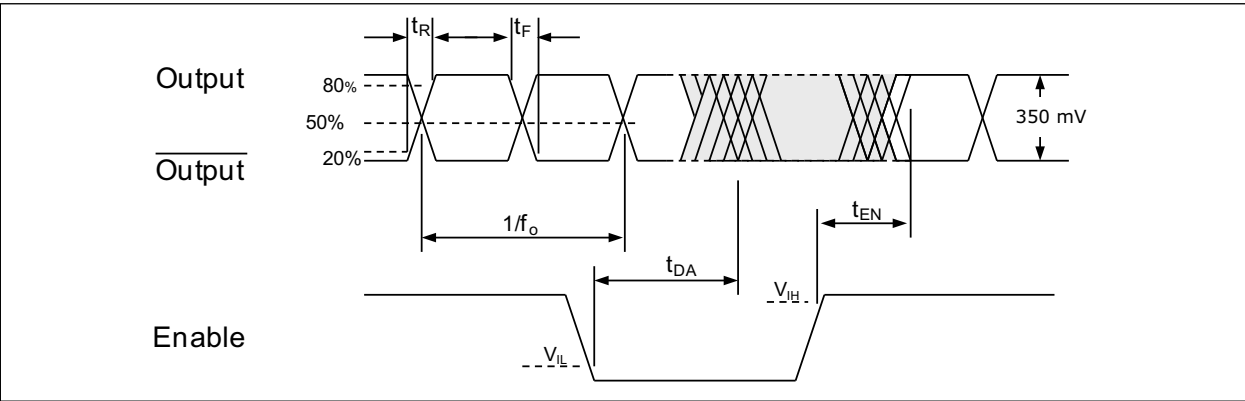


FIGURE 3-3: Output Waveform.

3.2 Typical Termination Scheme

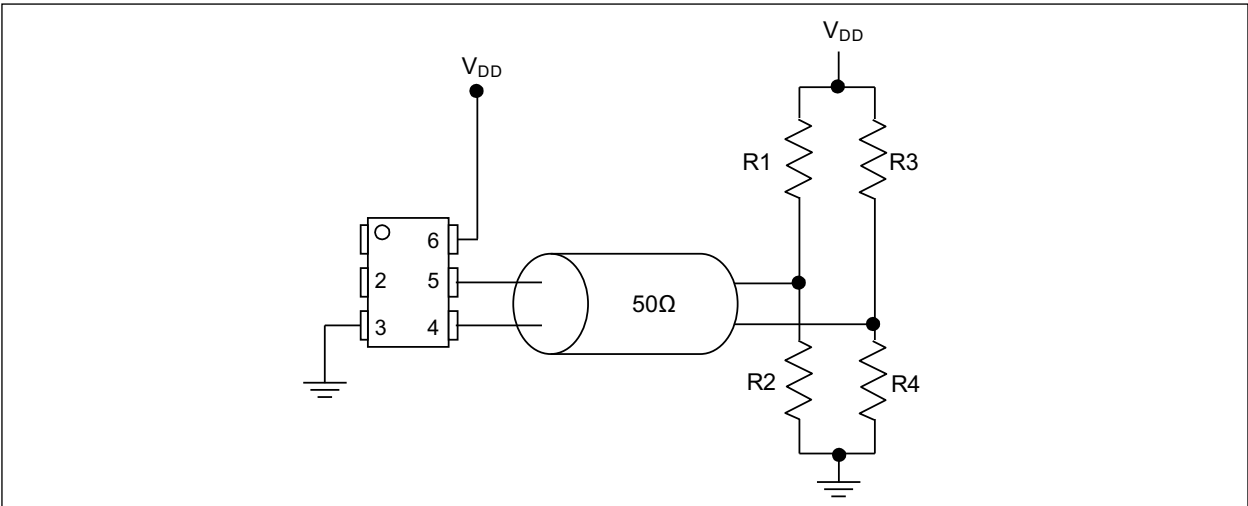


FIGURE 3-4: Typical Termination Scheme.

The values for R1, R2, R3, and R4 in the termination scheme depend on what V_{DD} is used. Table 3-1 lists the recommended values for each resistor depending on V_{DD}.

TABLE 3-1: RECOMMENDED RESISTOR VALUES

V _{DD}	R1, R3	R2, R4
3.3V	130Ω	82Ω
2.5V	249Ω	62Ω

3.3 Test Circuit

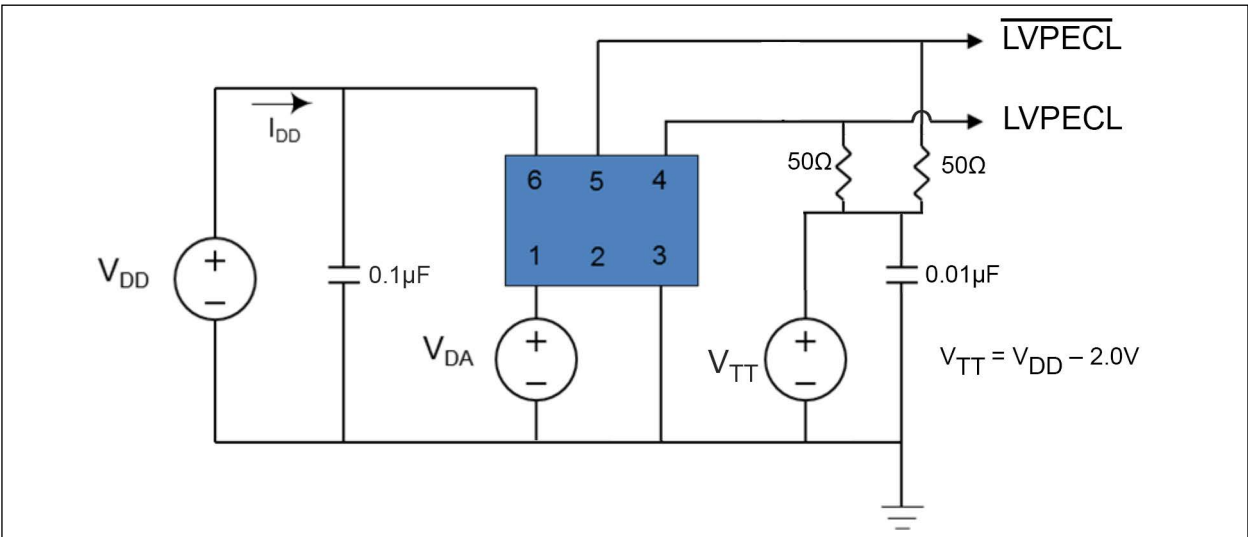


FIGURE 3-5: Test Circuit.

3.4 Recommended Board Layout

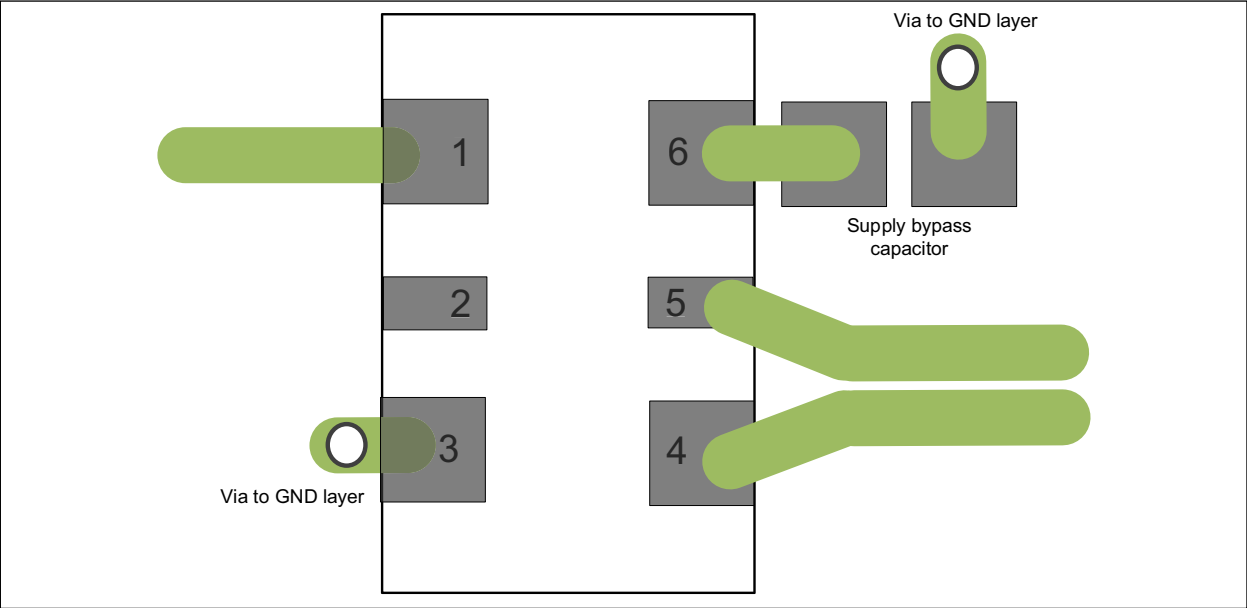
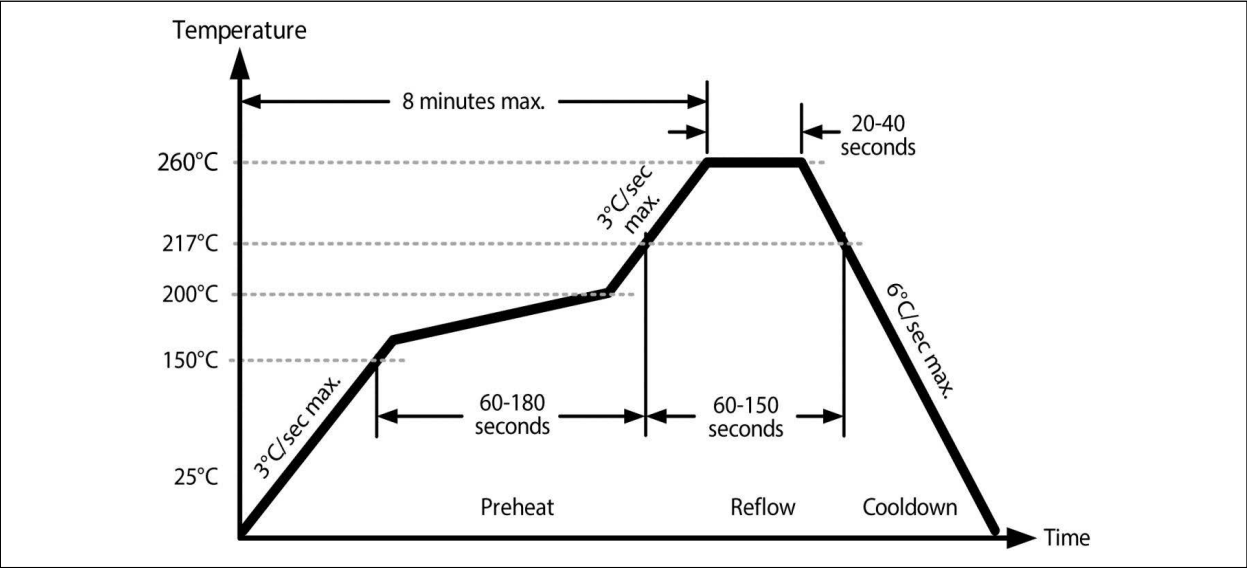


FIGURE 3-6: Recommended Board Layout.

3.5 Solder Reflow Profile

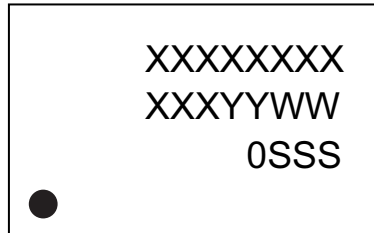


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60-180 sec.
Time Maintained above 217°C	60-150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20-40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

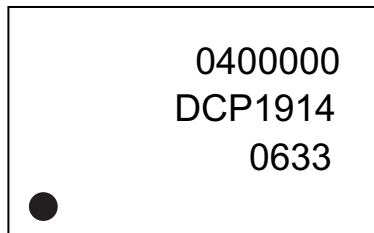
4.0 PACKAGE MARKING INFORMATION

4.1 Package Marking Information

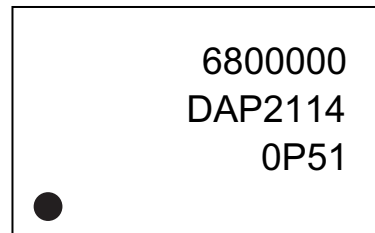
6-Lead LVPECL*



Example 1*



Example 2*



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

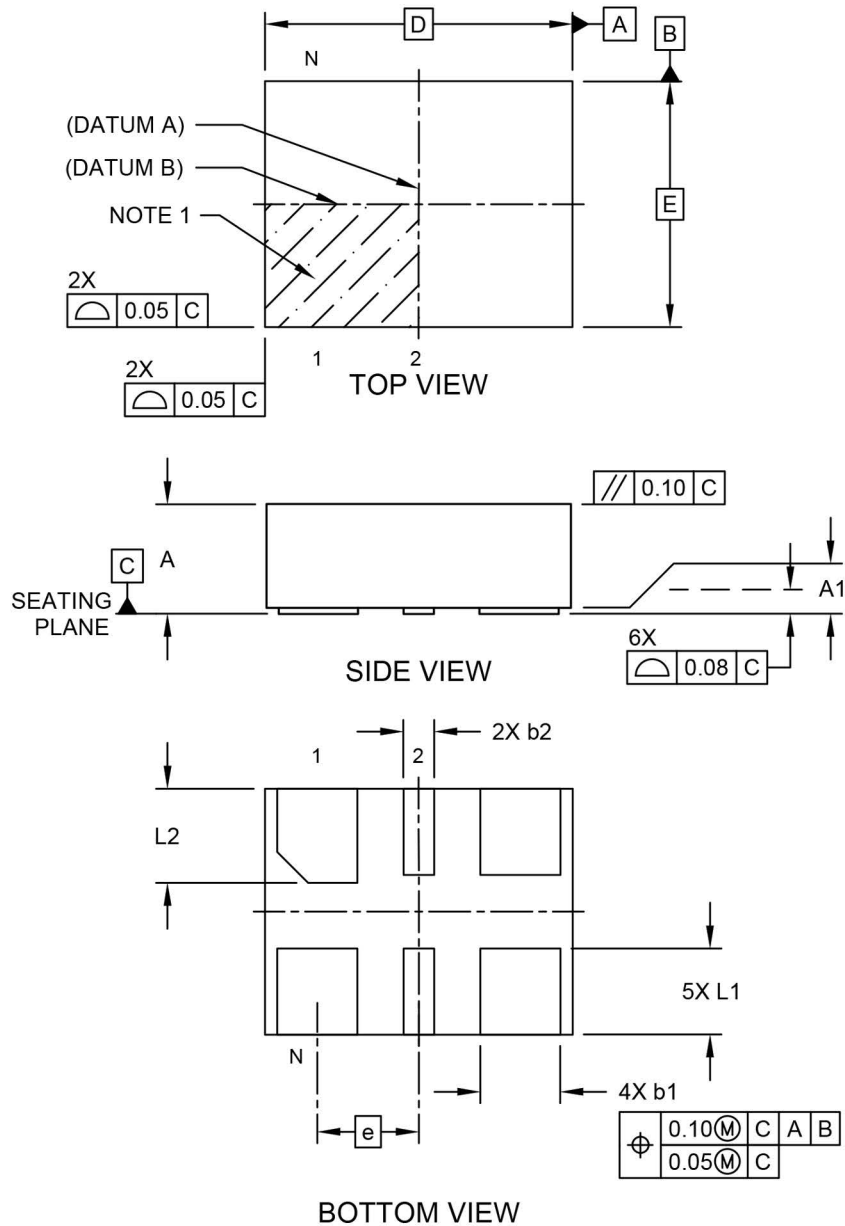
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: Devices may not include a top-line frequency marking. Product identity and output frequency are defined by the ordering code and accompanying documentation. Devices without a frequency marking remain fully compliant with all applicable datasheet specifications.

6-Lead 2.5 mm × 2.0 mm VDFN (J7A) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

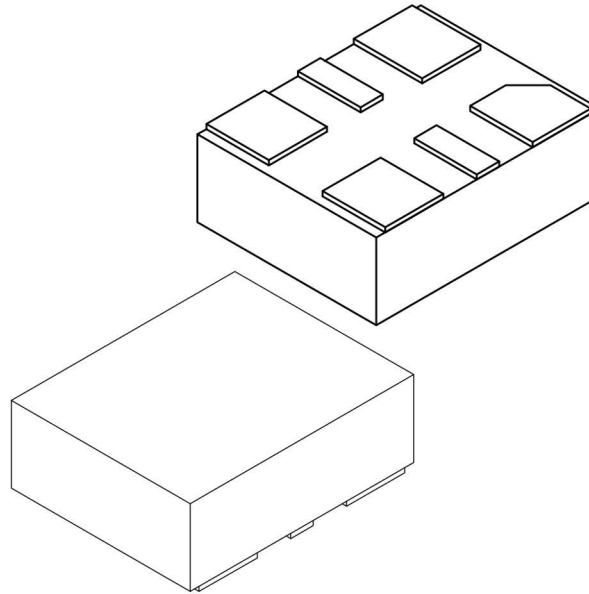


Microchip Technology Drawing C04-1005-J7A Rev E Sheet 1 of 2

© 2024 Microchip Technology Inc.

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.825 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	2.50 BSC		
Overall Width	E	2.00 BSC		
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

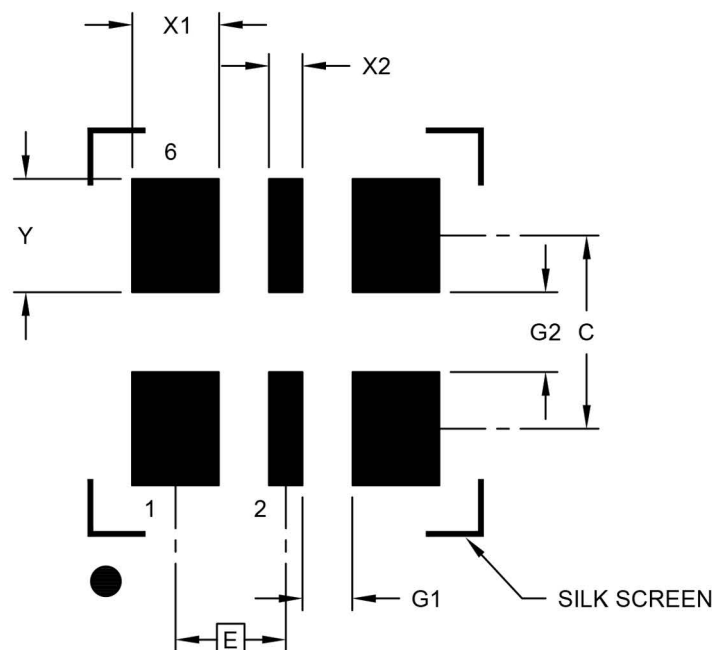
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005-J7A Rev E Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.825 BSC		
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

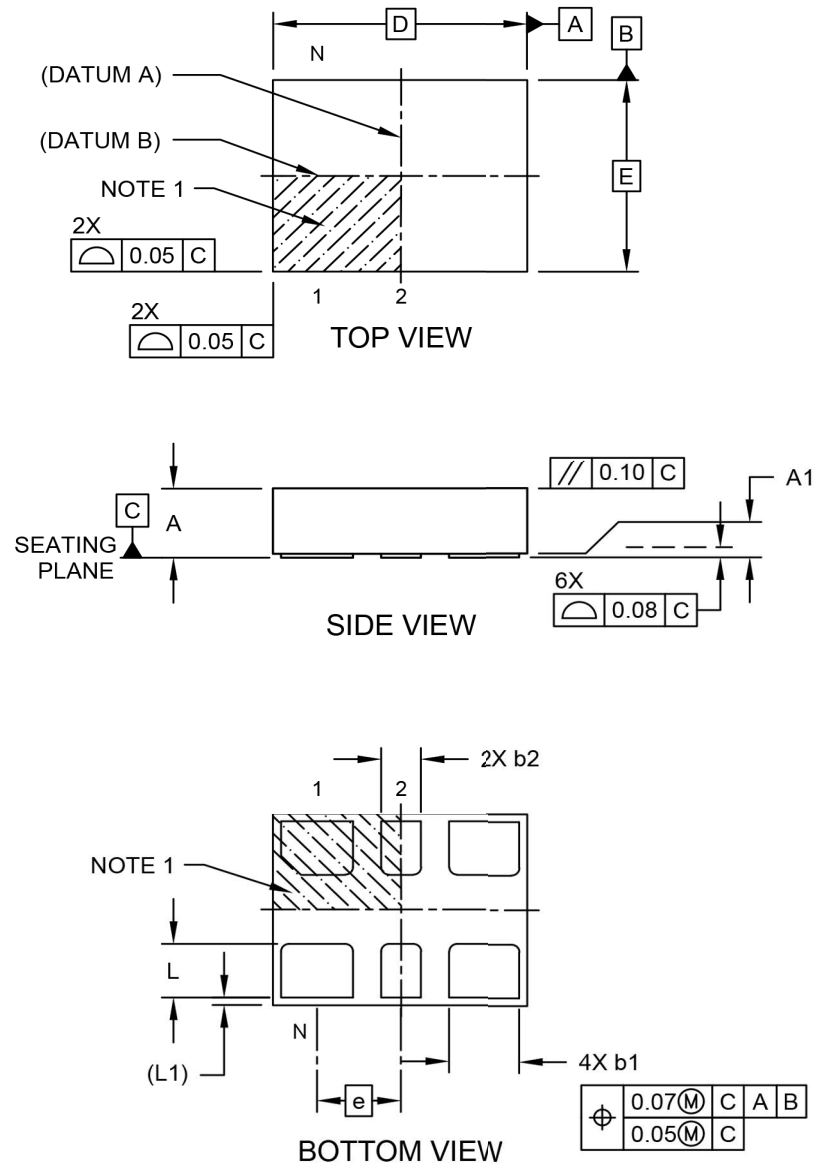
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005-J7A Rev E

6-Lead 3.2 mm × 2.5 mm VDFN (H5A) Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

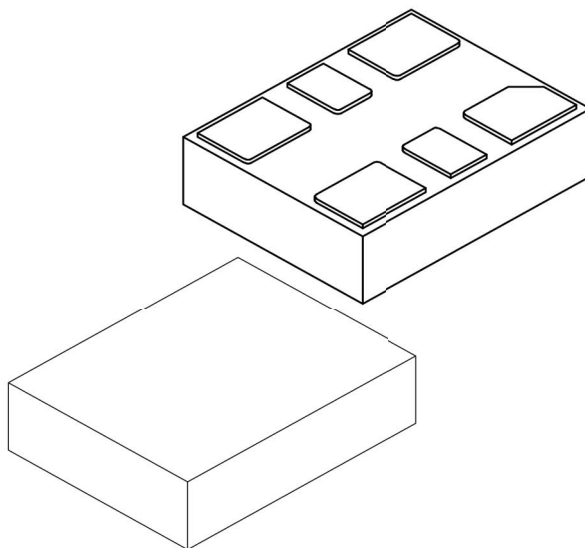


Microchip Technology Drawing C04-1007-H5A Rev C Sheet 1 of 2

© 2024 Microchip Technology Inc.

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	1.05 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	3.20 BSC		
Overall Width	E	2.50 BSC		
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1	0.10 REF		

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

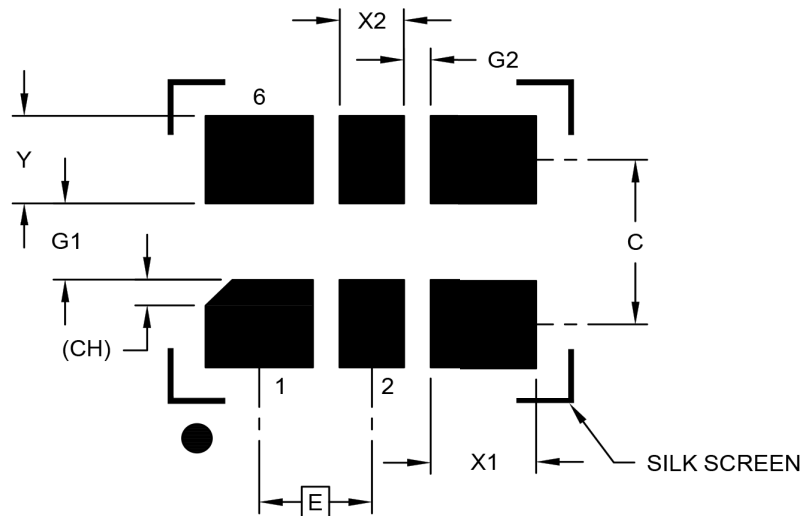
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007-H5A Rev C Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.05 BSC	
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.75		
Space Between Contacts (X3)	G2	0.25		
Pin 1 Index Chamfer (X4)	CH		0.25	

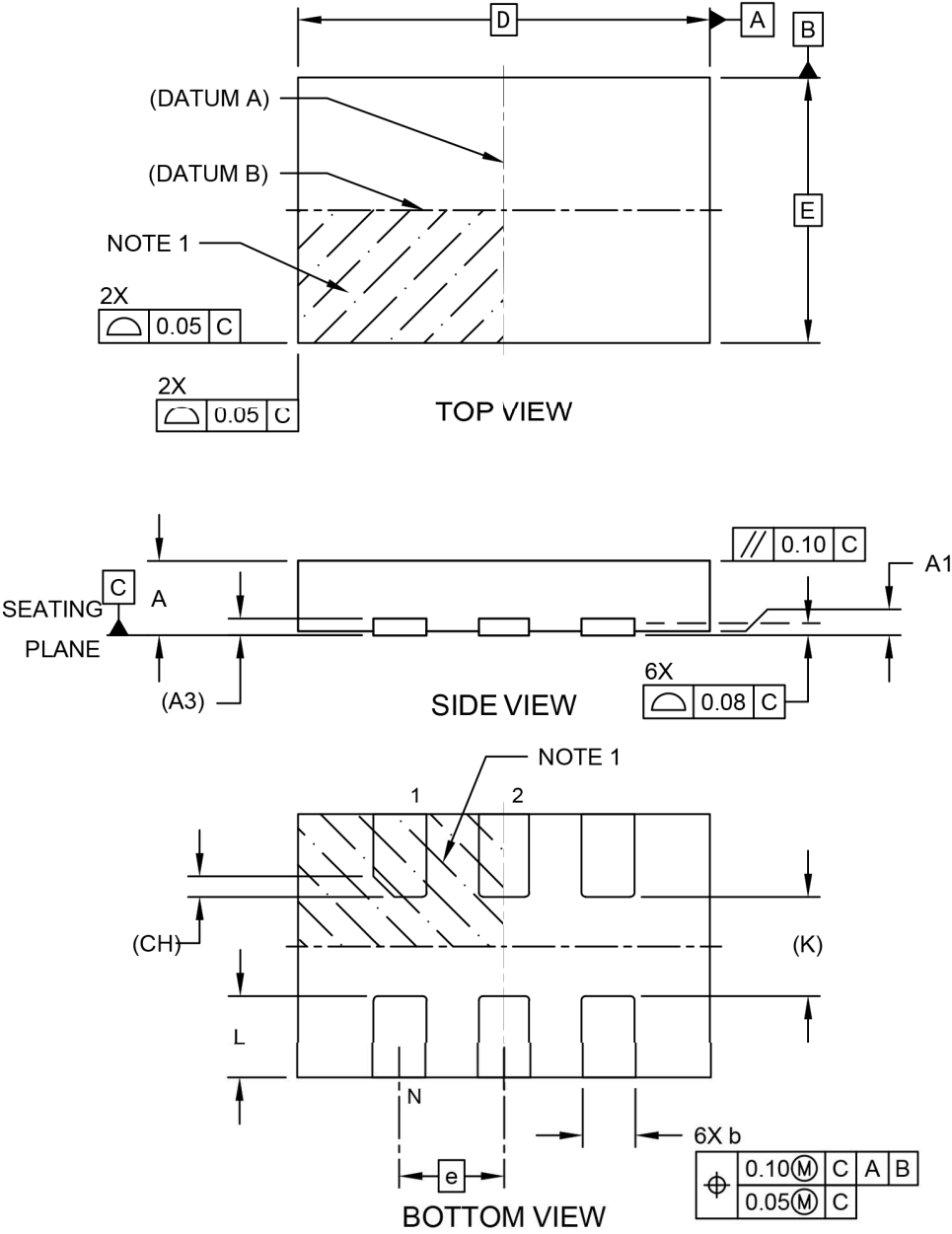
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007-H5A Rev C

6-Lead 3.2 mm × 5.0 mm VDFN (H7A) Package Outline and Recommended Land Pattern

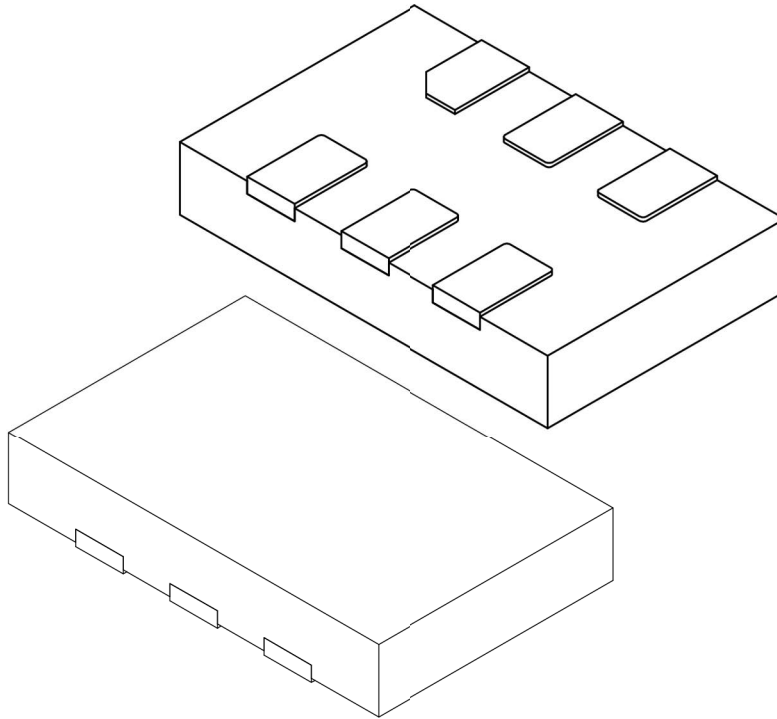
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1009-H7A Rev B Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	1.27 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	5.00 BSC		
Overall Width	E	3.20 BSC		
Terminal Width	b	0.59	0.64	0.69
Terminal Length	L	0.90	1.00	1.10
Terminal 1 Index Chamfer	CH	0.25 REF		
Terminal-to-Terminal	K	1.20 REF		

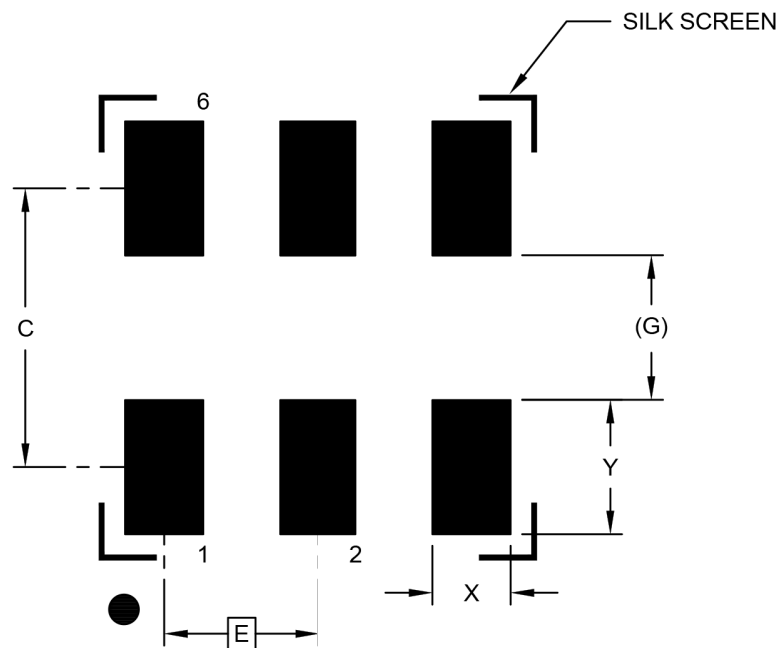
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1009-H7A Rev B Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

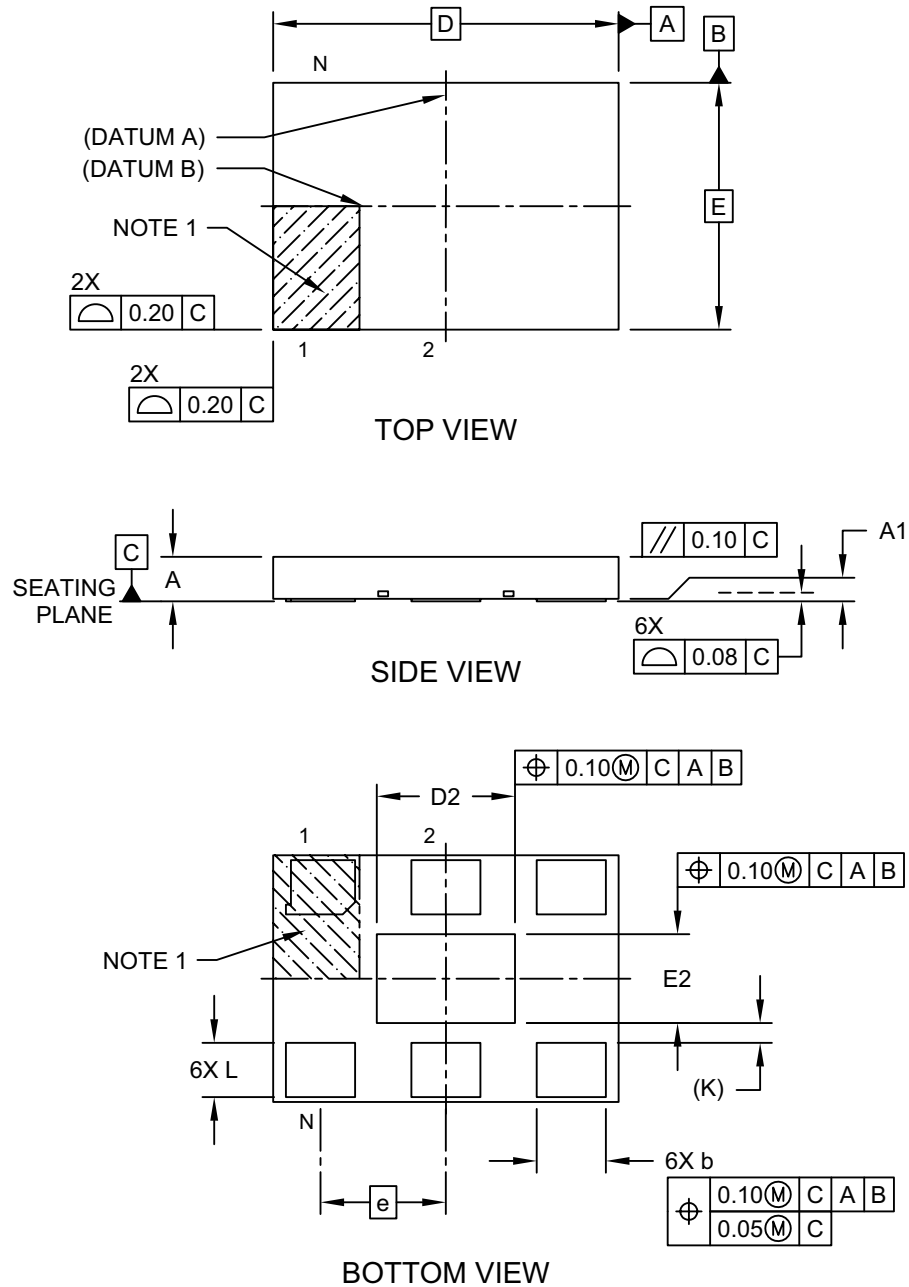
Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		2.30	
Contact Pad Width (X6)	X			0.64
Contact Pad Length (X6)	Y			1.10
Contact Pad to Contact Pad (X4)	G		1.20 REF	

- Notes:
- 1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3009-H7A Rev B

6-Lead 7.0 mm × 5.0 mm VDFN (H8A) Package Outline and Recommended Land Pattern

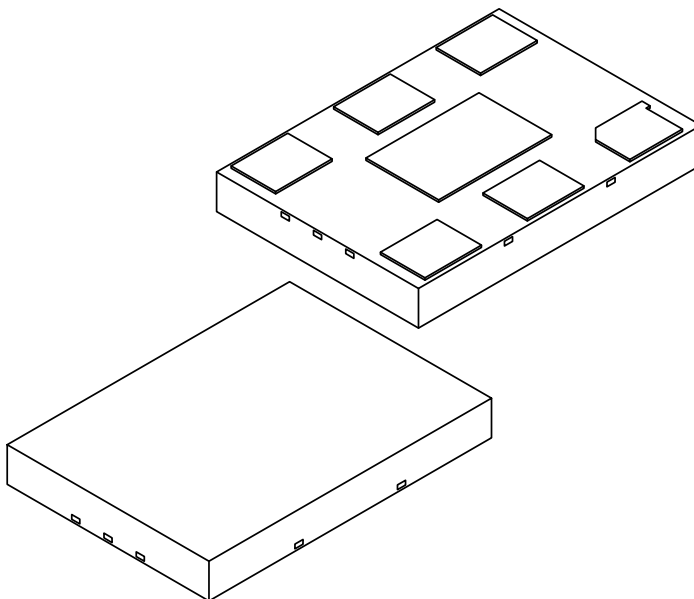
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1010A Sheet 1 of 2

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	2.54		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	7.00 BSC		
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	1.70	1.80	1.90
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.00	1.10	1.20
Terminal-to-Exposed-Pad	K	0.20 REF		

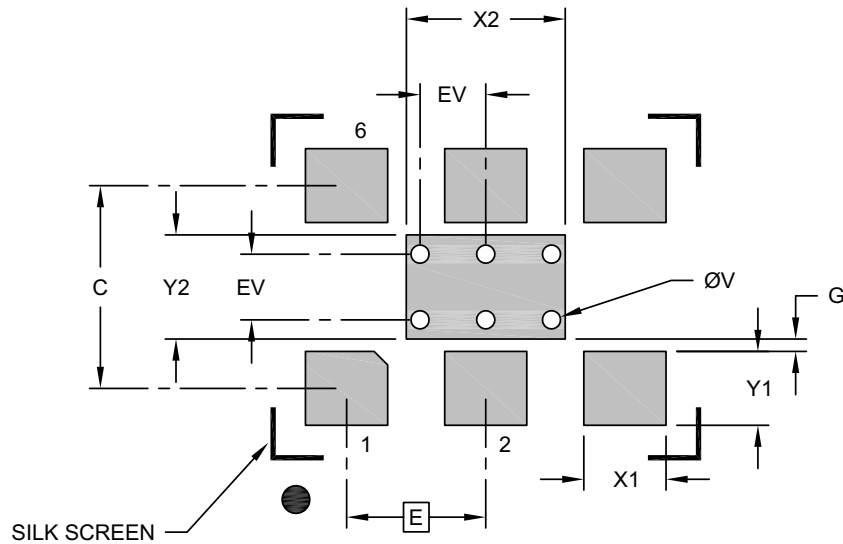
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1010A Sheet 2 of 2

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	2.54 BSC		
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			1.90
Contact Pad Spacing	C		3.70	
Contact Pad Width (X6)	X1			1.50
Contact Pad Length (X6)	Y1			1.35
Contact Pad to Center Pad (X2)	G	0.20		
Thermal Via Diameter (X6)	V		0.33	
Thermal Via Pitch	EV		1.20	

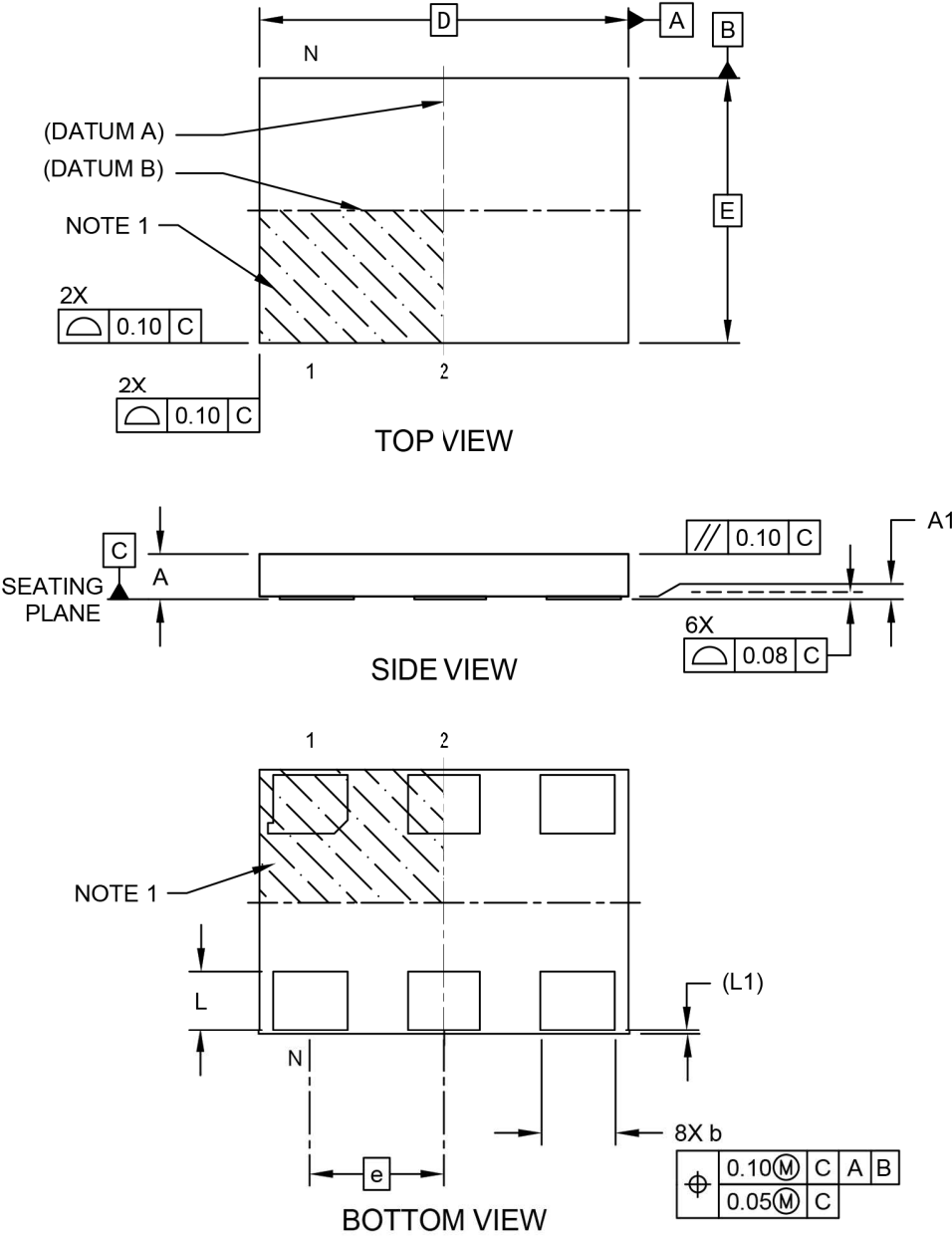
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3010A

6-Lead 7.0 mm × 5.0 mm VDFN (HPA) Package Outline and Recommended Land Pattern

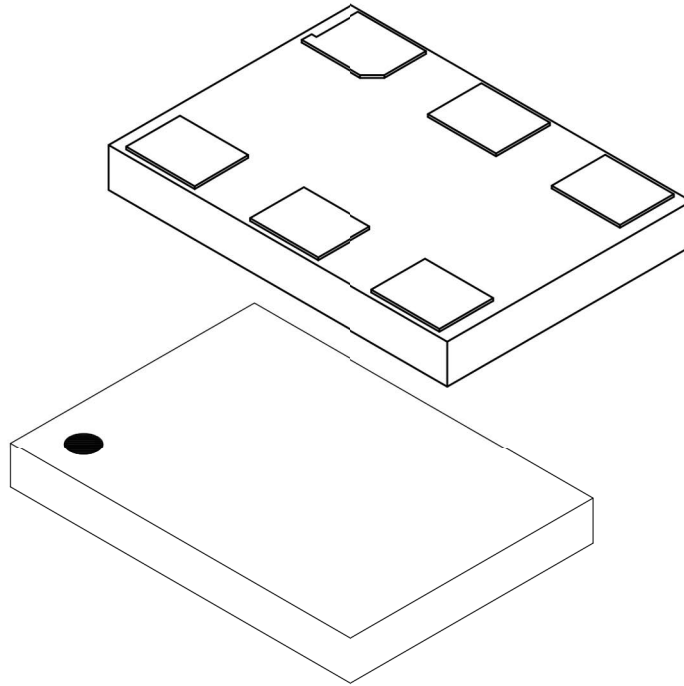
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1227-HPA Rev B Sheet 1 of 2

6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		6		
Pitch	e		2.54 BSC		
Overall Height	A		0.80	0.85	0.90
Standoff	A1		0.00	0.02	0.05
Overall Length	D		7.00 BSC		
Overall Width	E		5.00 BSC		
Terminal Width	b		1.30	1.40	1.50
Terminal Length	L		1.00	1.10	1.20
Pullback	L1		0.10 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

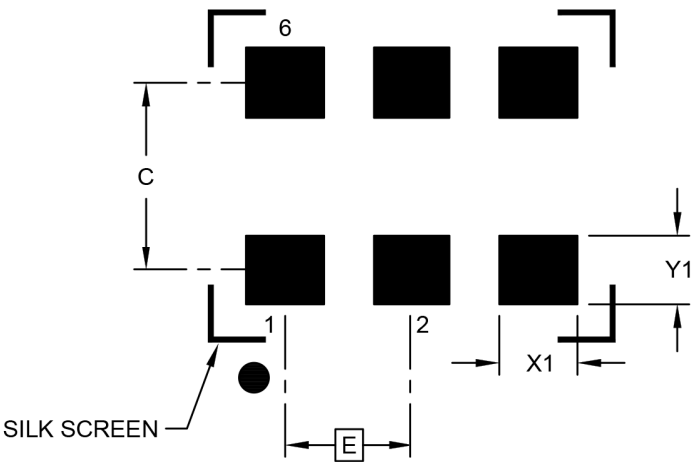
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1227-HPA Rev B Sheet 2 of 2

6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Urits		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.54 BSC		
Contact Pad Spacing	C		3.90	
Contact Pad Width (X6)	X1			1.55
Contact Pad Length (X6)	Y1			1.40

- Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3227-HPA Rev B

APPENDIX A: REVISION HISTORY

Revision A (October 2019)

- Initial creation of document DSC1102/22 to Microchip data sheet template DS20006254A.
- Minor text changes throughout.

Revision B (November 2025)

- Updated [Package Marking Information](#) drawing.
- Updated all package outline drawings (PODs) to the latest versions, and replaced legacy POD for CDFN package with current Microchip VDFN package POD (H7A 5032).
- Replaced CDFN references in [Product Identification System](#) page with current VDFN ones.
- Updated back matter ([Microchip Information](#)).

Revision C (March 2026)

- Added notes regarding order quantities and packing options to the [Product Identification System](#) section.

Revision D (July 2026)

- Added a note at the end of the [Package Marking Information](#) section about frequency marking.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		X	X	X	-XXX.XXXX	X
Device		Package	Temperature Range	Stability	Frequency	Packaging Option
Device:		DSC1102:	Low-Jitter Precision LVPECL Oscillator with Standby Pin			
		DSC1122:	Low-Jitter Precision LVPECL Oscillator with Output Enable			
Package:		A	=	6-Lead 7.0 mm × 5.0 mm VDFN		
		B	=	6-Lead 5.0 mm × 3.2 mm VDFN		
		C	=	6-Lead 3.2 mm × 2.5 mm VDFN		
		D	=	6-Lead 2.5 mm × 2.0 mm VDFN		
		N	=	6-Lead 7.0 mm × 5.0 mm VDFN w/o center pad		
Temperature Range:		E	=	-20°C to +70°C (Extended Commercial)		
		I	=	-40°C to +85°C (Industrial)		
		L	=	-40°C to +105°C (Extended Industrial)		
Stability:		1	=	±50 ppm		
		2	=	±25 ppm		
		3	=	±20 ppm		
		5	=	±10 ppm		
Frequency: (Note 1)		xxx.xxxx	=	2.3 MHz to 460 MHz (User Defined)		
Packing Option: (Note 2, Note 3, Note 4)		<blank>	=	Tube		
		T	=	1000/Reel		

Examples:

a) DSC1102AE1-053.5000:

DSC1102, 6-Lead 7.0 mm × 5.0 mm VDFN, Ext. Commercial Temp. Range, ±50 ppm Stability, 53.5 MHz Frequency, Tube

b) DSC1122BI2-246.8100T:

DSC1122, 6-Lead 5.0 mm × 3.2 mm VDFN, Industrial Temp. Range, ±25 ppm Stability, 246.81 MHz Frequency, 1000/Reel

c) DSC1102CL5-156.2500:

DSC1102, 6-Lead 3.2 mm × 2.5 mm VDFN, Ext. Industrial Temp. Range, ±10 ppm Stability, 156.25 MHz Frequency, Tube

d) DSC1122DE3-094.5500T:

DSC1122, 6-Lead 2.5 mm × 2.0 mm VDFN, Industrial Temp. Range, ±20 ppm Stability, 94.55 MHz Frequency, 1000/Reel

- Note 1:** Please visit the Microchip [ClockWorks® Configurator](http://clockworks.microchip.com/timing) to configure the part number for customized frequency.
- Note 2:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
- Note 3:** On orders for bulk CPNs, product may be supplied in either cut tape (without a reel) or tube packaging, depending on availability.
- Note 4:** For Tape & Reel orders that are <1000pcs, product may be supplied on cut tape (without a reel) depending on availability.

NOTES:

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.