

12-Bit, 6 GSPS/10.25 GSPS, RF Analog-to-Digital Converter

FEATURES

- ▶ High instantaneous dynamic range
- ▶ NSD
 - ▶ -155.1 dBFS/Hz at 10 GSPS with -9 dBFS, 170 MHz input
 - ▶ -153 dBFS/Hz at 10 GSPS with -1 dBFS, 170 MHz input
- ▶ SFDR: 70 dBFS at 10 GSPS with -1 dBFS, 1000 MHz input
- ▶ SFDR excluding H2 and H3 (worst other spur): -89 dBFS at 10 GSPS with -1 dBFS, 1000 MHz input
- ▶ Low power dissipation: 4.2 W typical at 10 GSPS
- ▶ Integrated input buffer (6.5 GHz input bandwidth)
 - ▶ 1.4 V p-p full-scale analog input with $R_{IN} = 50 \Omega$
 - ▶ Overvoltage protection
- ▶ Low latency, high speed parallel output port
- ▶ Fast overrange detection for efficient AGC
- ▶ On-chip temperature sensor
- ▶ On-chip negative voltage generators
- ▶ Low CER: $<1 \times 10^{-16}$
- ▶ Reconfigurable support for [AD9213](#) native mode
- ▶ 12 mm × 12 mm, 192-ball BGA-ED package

FUNCTIONAL BLOCK DIAGRAM

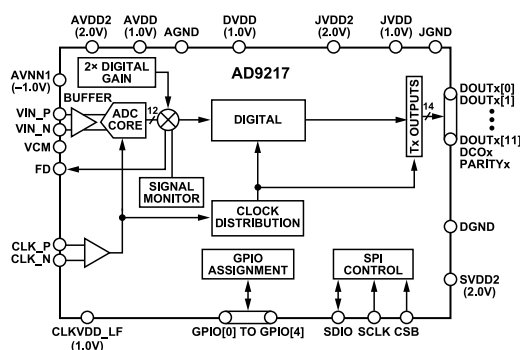


Figure 1.

GENERAL DESCRIPTION

The AD9217 is a single, 12-bit, 6 GSPS/10.25 GSPS, radio frequency (RF) analog-to-digital converter (ADC) with a 6.5 GHz input bandwidth. The AD9217 supports high dynamic range frequency and time domain applications requiring wide instantaneous bandwidth and low conversion error rates (CER).

The AD9217 features a low latency, high speed, parallel CML output interface that supports full bandwidth operation with compatible FPGA/ASIC receivers. The AD9217 can be reconfigured to operate in native AD9213 mode for applications requiring additional digital processing and JESD204B output support. Refer to the AD9213 data sheet when operating the AD9217 in AD9213 mode.

The AD9217 achieves dynamic range and linearity performance while consuming 4.2 W typical. The device is based on an interleaved pipeline architecture and features a proprietary calibration and randomization technique that suppresses interleaving spurious artifacts into its noise floor. The linearity performance of the AD9217 is preserved by a combination of on-chip dithering and calibration, which results in excellent spurious-free performance over a wide range of input signal conditions.

The AD9217 is offered in a [192-ball ball grid array \(BGA\) package](#) and is specified over a junction temperature range of -20°C to +115°C.

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REVISION HISTORY**6/2026—Revision A: Initial Version**

SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, analog input (A_{IN}) = -1.0 dBFS. Minimum/maximum specifications represent performance at $-20^{\circ}\text{C} \leq T_J \leq +115^{\circ}\text{C}$, unless otherwise noted. Typical specifications represent performance at $T_J = 70^{\circ}\text{C}$.

Register 0x1617 Bit 0 DC_COUPLED_MODE_EN = 0 (default value).

Table 1.

Parameter	AD9217-6G			AD9217-10G			Unit
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	12			12			Bits
ACCURACY							
No Missing Codes		Guaranteed			Guaranteed		
Offset Error	-10	-0.6	+9	-11	0	+11	LSB
Gain Error	-3.1	11.1	+19.2	-7.0	7.4	+17.0	%FSR
Differential Nonlinearity (DNL)	-0.5	± 0.25	+0.5	-0.5	± 0.3	+0.6	LSB
Integral Nonlinearity (INL)	-4.8	± 0.7	+7.4	-8.2	± 2.4	+6.2	LSB
ANALOG INPUTS							
Differential Input Voltage Range (Internal $V_{REF} = 0.5\text{ V}$)		1.4			1.4		V p-p
Resistance (R_{IN})	47.8	50	52.2	47.8	50.0	52.2	Ω
Capacitance		1			1		pF
Internal Common-Mode Voltage (V_{CM})		0.5			0.5		V
Analog Full Power Bandwidth (Internal Termination)		6.5			6.5		GHz
Input Referred Noise		1.61			1.72		LSB _{RMS}
POWER SUPPLIES							
BVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
BVNN1	-1.025	-1.0	-0.975	-1.025	-1.0	-0.975	V
AVNN1	-1.025	-1.0	-0.975	-1.025	-1.0	-0.975	V
BVNN2 (Internally Generated)	-2.05	-2.0	-1.95	-2.05	-2.0	-1.95	V
BVDD3 (Internally Generated)	2.925	3.0	3.075	2.925	3.0	3.075	V
AVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
CLKVDD_LF	0.975	1.0	1.025	0.975	1.0	1.025	V
PLLVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
AVDDFS8	0.975	1.0	1.025	0.975	1.0	1.025	V
FVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
VDD_NVG	0.975	1.0	1.025	0.975	1.0	1.025	V
RVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
SVDD2	1.75	2.0	2.05	1.75	2.0	2.05	V
JVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
DVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
JVTT	0.975	1.0	1.025	0.975	1.0	1.025	V
JVDD	0.975	1.0	1.025	0.975	1.0	1.025	V
TMU_AVDD2	1.95	2.0	2.05	1.95	2.0	2.05	V
TMU_DVDD1	0.975	1.0	1.025	0.975	1.0	1.025	V
I_{BVDD2}		109	143		112	147	mA
I_{BVNN1}		-115	-149		-116	-151	mA
I_{AVNN1}		-1.8	-2.1		-1.8	-2	mA
I_{BVNN2}^1	N/A ²	N/A ²	N/A ²	N/A ²	N/A ²	N/A ²	mA
I_{BVDD3}^1	N/A ²	N/A ²	N/A ²	N/A ²	N/A ²	N/A ²	mA
I_{AVDD}		1730	2240		2200	2800	mA
I_{CLKVDD_LF}		28	34		31	37	mA
$I_{PLLVDD2}$		1	2		1	2	mA
$I_{AVDDFS8}$		26	44		38	56	mA
I_{FVDD}		25	28		31	35	mA

SPECIFICATIONS

Table 1. (Continued)

Parameter	AD9217-6G			AD9217-10G			Unit
	Min	Typ	Max	Min	Typ	Max	
$I_{VDD_NVG}^3$		155	193		159	195	mA
$I_{VDD_NVG}^4$		383	479		387	478	mA
I_{RVDD2}		32	35		35	38	mA
I_{SVDD2}		0.3	1		0.3	1	mA
I_{JVDD2}		22	25		24	27	mA
I_{DVDD}		330	693		527	927	mA
I_{JVTT}		126	209		142	211	mA
I_{JVDD}		304	479		473	649	mA
I_{TMU_AVDD2}		1.7	2		1.7	2	mA
I_{TMU_DVDD1}		0.25	1		1	2	mA
Power Consumption ⁵							
Total Power Dissipation (Including Output Drivers) ⁶		3.3	4.6		4.2	5.6	W
Power-Down		114			114		mW
Standby		2.7			2.7		W

¹ Internally supplied.

² N/A means not applicable.

³ Current when AVNN1 and BVNN1 are supplied by an external source.

⁴ Current when AVNN1 and BVNN1 are supplied by VNEG_OUT.

⁵ Power and supply currents are typical unless otherwise noted.

⁶ Total power when AVNN1 and BVNN1 are supplied by VNEG_OUT.

AC SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, $A_{IN} = -1.0$ dBFS. Minimum/maximum specifications represent performance at $-20^{\circ}\text{C} \leq T_J \leq +115^{\circ}\text{C}$, unless otherwise noted. Typical specifications represent performance at $T_J = 70^{\circ}\text{C}$.

Register 0x1617 Bit 0 DC_COUPLED_MODE_EN = 0 (default value).

Table 2.

Parameter	AD9217-6G			AD9217-10G			Unit
	Min	Typ	Max	Min	Typ	Max	
NOISE SPECTRAL DENSITY (NSD)							
At 170 MHz, -1 dBFS		-153			-153		dBFS/Hz
At 170 MHz, -9 dBFS		-153.8			-155.1		dBFS/Hz
At 170 MHz, -30 dBFS		-153.9			-155.7		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)							
Input Frequency (f_{IN}) = 170 MHz		58.2			55.9		dBFS
$f_{IN} = 1000$ MHz		56.8			55.8		dBFS
$f_{IN} = 2600$ MHz	50.1	52.3		43.8	51.0		dBFS
$f_{IN} = 4000$ MHz		50.2			49.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)							
$f_{IN} = 170$ MHz		58.2			55.6		dBFS
$f_{IN} = 1000$ MHz		56.6			55.6		dBFS
$f_{IN} = 2600$ MHz	48.8	52.3		42.7	50.8		dBFS
$f_{IN} = 4000$ MHz		49.3			49.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)							
$f_{IN} = 170$ MHz		9.4			8.9		Bits
$f_{IN} = 1000$ MHz		9.1			8.9		Bits

SPECIFICATIONS

Table 2. (Continued)

Parameter	AD9217-6G			AD9217-10G			Unit
	Min	Typ	Max	Min	Typ	Max	
$f_{IN} = 2600$ MHz		8.4			8.1		Bits
$f_{IN} = 4000$ MHz		7.9			7.9		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC							
$f_{IN} = 170$ MHz		81			70		dBFS
$f_{IN} = 1000$ MHz		71			70		dBFS
$f_{IN} = 2600$ MHz	60	76		62	65		dBFS
$f_{IN} = 4000$ MHz		57			60		dBFS
SECOND HARMONIC (H2)							
$f_{IN} = 170$ MHz		-90			-71		dBFS
$f_{IN} = 1000$ MHz		-89			-77		dBFS
$f_{IN} = 2600$ MHz		-76	-60		-65	-62	dBFS
$f_{IN} = 4000$ MHz		-57			-60		dBFS
THIRD HARMONIC (H3)							
$f_{IN} = 170$ MHz		-81			-70		dBFS
$f_{IN} = 1000$ MHz		-71			-70		dBFS
$f_{IN} = 2600$ MHz		-76	-66		-72	-65	dBFS
$f_{IN} = 4000$ MHz		-67			-74		dBFS
WORST OTHER (WO), EXCLUDING SECOND OR THIRD HARMONIC ($ WO = SFDR$ EXCLUDING H2 OR H3)							
$f_{IN} = 170$ MHz		-89			-88		dBFS
$f_{IN} = 1000$ MHz		-95			-89		dBFS
$f_{IN} = 2600$ MHz		-85	-76		-89	-72	dBFS
$f_{IN} = 4000$ MHz		-82			-86		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1} - f_{IN2}$), f_{IN1} AND $f_{IN2} = -7.0$ dBFS							
$f_{IN1} = 1842$ MHz, $f_{IN2} = 1847$ MHz		-80			-77		dBFS
$f_{IN1} = 2138$ MHz, $f_{IN2} = 2143$ MHz		-75			-76		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1} - f_{IN2}$), f_{IN1} AND $f_{IN2} = -15.0$ dBFS							
$f_{IN1} = 1842$ MHz, $f_{IN2} = 1847$ MHz		-108			-99		dBFS
$f_{IN1} = 2138$ MHz, $f_{IN2} = 2143$ MHz		-100			-101		dBFS

DIGITAL SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, $A_{IN} = -1.0$ dBFS. Minimum/maximum specifications represent performance at $-20^{\circ}\text{C} \leq T_J \leq +115^{\circ}\text{C}$, unless otherwise noted. Typical specifications represent performance at $T_J = 70^{\circ}\text{C}$.

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK_P, CLK_N)				
Logic Compliance		Low voltage positive emitter coupled logic (LVPECL)		
Differential Input Voltage	300	800	1800	mV p-p
Common-Mode Input Voltage		0.675		V
Input Resistance (Differential)		106		Ω
Input Capacitance		0.9		pF
LOGIC INPUTS (SDIO, SCLK, CSB, GPIO, PWDN)				
Logic Compliance		Complementary metal-oxide semiconductor (CMOS)		

SPECIFICATIONS

Table 3. (Continued)

Parameter	Min	Typ	Max	Unit
Voltage				
Logic 1	$0.70 \times \text{SVDD2}$			V
Logic 0	0		$0.30 \times \text{SVDD2}$	V
Input Resistance (Single-Ended)		44		k Ω
LOGIC OUTPUT (SDIO, GPIO, FD)				
Logic Compliance		CMOS		
Voltage				
Logic 1, Output Logic Current High (I_{OH}) = 4 mA	$\text{SVDD2} - 0.45$			V
Logic 0, Output Logic Current Low (I_{OL}) = 4 mA	0		0.45	V
RESET (RSTB) INPUT				
Logic Compliance		CMOS		
Voltage				
Logic 1	$0.70 \times \text{SVDD2}$			V
Logic 0	0		$0.30 \times \text{SVDD2}$	V
Input Resistance		77		k Ω

SWITCHING SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, $A_{IN} = -1.0$ dBFS. Minimum/maximum specifications represent performance at $-20^{\circ}\text{C} \leq T_J \leq +115^{\circ}\text{C}$, unless otherwise noted. Typical specifications represent performance at $T_J = 70^{\circ}\text{C}$.

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK (CLK)				
Maximum Clock Rate			10.25	GSPS
Minimum Clock Rate	3.5			GSPS
Clock Duty Cycle	45	50	55	% duty cycle
LATENCY				
Pipeline Latency (t_{PD})		225		Clock cycles
Fast Detect (FD) Latency		170		Clock cycles
OUTPUT PARAMETERS (DOUT_x[x], PARITY_x, DCO_x)				
Logic Compliance		CML		
Differential Output Voltage	560	770		mV p-p
Differential Termination Impedance	100	120		Ω
Rise Time (t_R) (20% to 80% into 100 Ω Load)		26		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		26		ps
DCO Frequency (Operates at 1/2 CLK Rate) (CK_{FREQ})	1.75		5.125	GSPS
DCO Duty Cycle (CK_{DUTY})	49	50	51	% duty cycle
DCO to Data (DOUT) Delay (CK_{DLY})	-200	+25	+200	ps
Data (DOUT) to Data (DOUT) Skew ($D_{D_{SKEW}}$)	-250		+250	ps
Data Period (D_{PERIOD})	97.56	100		ps
WAKE-UP TIME				
Standby		1		ms
Power-Down		25		ms
APERTURE				
Delay (t_A)		120		ps
Uncertainty (Jitter, t_J)		50		(f_s) rms

SPECIFICATIONS

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL PORT INTERFACE (SPI) TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	4			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK can be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK can be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 2)	10			ns

Timing Diagrams

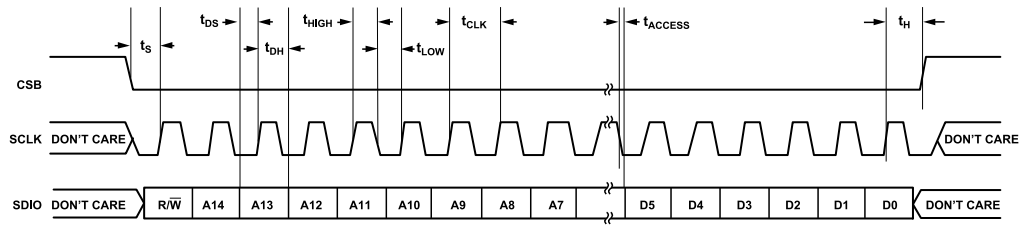


Figure 2. Serial Port Interface Timing Diagram (MSB First)

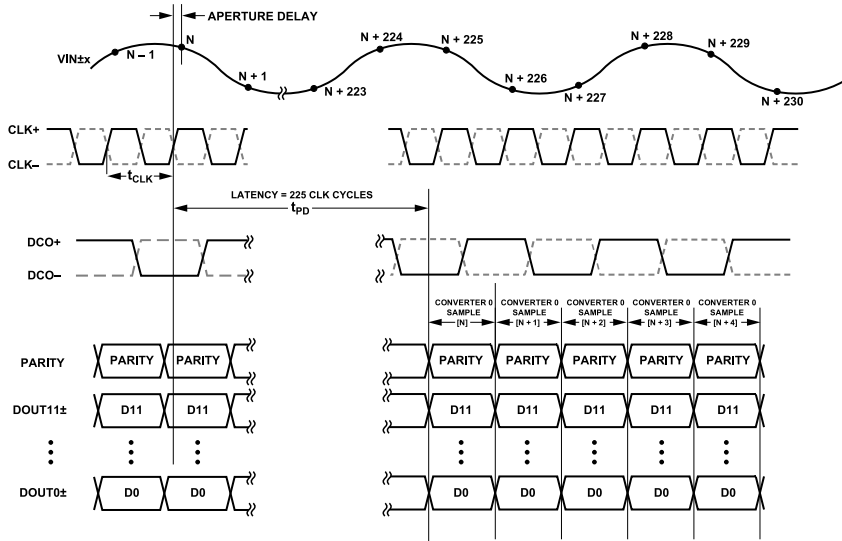


Figure 3. Parallel Data Output Timing Diagram

SPECIFICATIONS

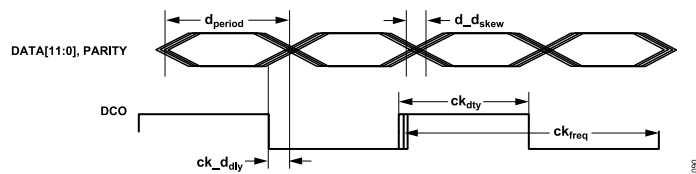


Figure 4. Data and Data Clock Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Pins	
BVDD2 to AGND	2.2 V
BVNN1 to AGND	−1.1 V
AVNN1 to GND	−1.1 V
AVDD to AGND	1.1 V
CLKVDD_LF to AGND	1.1 V
PLLVD2 to AGND	2.2 V
AVDDFS8 to AVSSFS8	1.1 V
FVDD to AGND	1.1 V
VDD_NVG to VSS_NVG	1.1 V
RVDD2 to AGND	2.2 V
SVDD2 to DGND	2.2 V
DVDD to DGND	1.1 V
JVTT to JGND	1.1 V
JVDD to JGND	1.1 V
JVDD2 to JGND	2.2 V
TMU_AVDD2 to AGND	2.2 V
TMU_DVDD1 to AGND	1.1 V
Ground Pins	
AVSSFS8 to DGND	−0.3 V to +0.3 V
VSS_NVG to DGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
AGND to JGND	−0.3 V to +0.3 V
DGND to JGND	−0.3 V to +0.3 V
Input/Output Pins	
VIN_x to AGND	−0.125 V to AVDD + 0.150 V
CLK_x to AGND	AGND − 0.3 V to CLKVDD_LF + 0.3 V
CSB, RSTB, PDWN, SCLK, FD, GPIO[x], SDIO to DGND	DGND − 0.3 V to SVDD2 + 0.3 V
TMU_REFx to TMU_AGND	AGND − 0.3 V to TMU_AVDD2 + 0.3 V
VCM to AGND	AGND − 0.3 V to RVDD2 + 0.3 V
DOUT_x[x], PARITY_x, DCO_x to JGND	JGND − 0.3 V to JVTT + 0.3 V

Table 6. (Continued)

Parameter	Rating
Storage Temperature, T _A	−40°C to +150°C
Operating Junction Temperature (T _J)	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

θ_{JB} is the junction to board thermal resistance.

Table 7. Thermal Resistance

Package Type ¹	θ_{JA}	θ_{JC}	θ_{JB}	Unit
BP-192-1	20.5	1.6	9.2	°C/W

¹ The specified thermal resistance values are simulated based on JEDEC specifications in compliance with JESD51-12.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

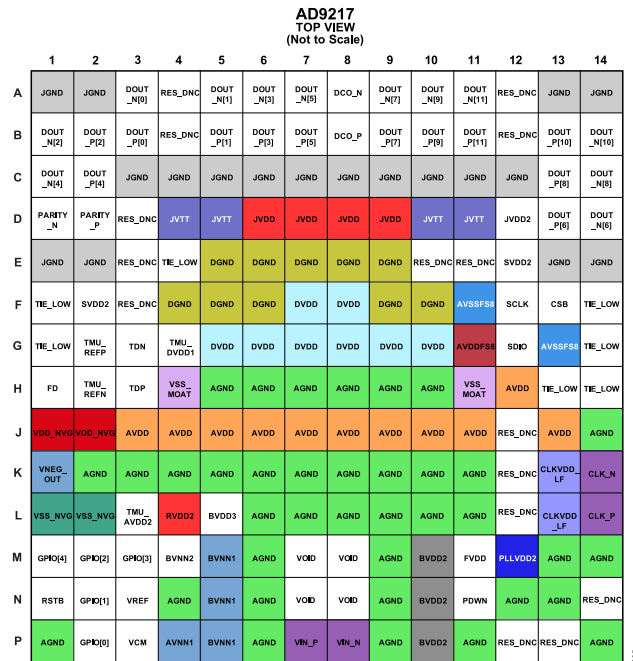


Figure 5. Pin Configuration (Top View, Not to Scale)

Table 8. Pin Function Descriptions

Pin No.	Ball Mnemonic	Ball Type	Signal Type	Description
A1, A2, A13, A14, C3 to C12, E1, E2, E13, E14	JGND	Ground	Not applicable	Digital Output Ground.
A3, B3	DOUT_N[0], DOUT_P[0]	Output	CML	Bit 0 Differential Pair (LSB).
A5, B5	DOUT_N[1], DOUT_P[1]	Output	CML	Bit 1 Differential Pair.
B1, B2	DOUT_N[2], DOUT_P[2]	Output	CML	Bit 2 Differential Pair.
A6, B6	DOUT_N[3], DOUT_P[3]	Output	CML	Bit 3 Differential Pair.
C1, C2	DOUT_N[4], DOUT_P[4]	Output	CML	Bit 4 Differential Pair.
A7, B7	DOUT_N[5], DOUT_P[5]	Output	CML	Bit 5 Differential Pair.
D14, D13	DOUT_N[6], DOUT_P[6]	Output	CML	Bit 6 Differential Pair.
A9, B9	DOUT_N[7], DOUT_P[7]	Output	CML	Bit 7 Differential Pair.
C14, C13	DOUT_N[8], DOUT_P[8]	Output	CML	Bit 8 Differential Pair.
A10, B10	DOUT_N[9], DOUT_P[9]	Output	CML	Bit 9 Differential Pair.
B14, B13	DOUT_N[10], DOUT_P[10]	Output	CML	Bit 10 Differential Pair.
A11, B11	DOUT_N[11], DOUT_P[11]	Output	CML	Bit 11 Differential Pair (MSB).
A8, B8	DCO_N, DCO_P	Output	CML	Data Clock Output Differential Pair.
D1, D2	PARITY_N, PARITY_P	Output	CML	Parity Bit Differential Pair.
A4, A12, B4, B12, D3, E3, E10, E11, F3, J12, K12, L12, N3, N14, P12, P13	RES_DNC	Not applicable	Not applicable	Reserved. Do not connect.
D4, D5, D10, D11	JVTT	Supply	Not applicable	Output Driver Termination Voltage, 1 V Supply.
D6 to D9	JVDD	Supply	Not applicable	Digital Circuitry Supply, 1 V Supply.
D12	JVDD2	Supply	Not applicable	2 V Supply for Digital Outputs.
E4, F1, G1, F14, G14, H13, H14	TIE_LOW	Input	CMOS	Internal Use Only. Connect these pins to ground.
E5 to E9, F4 to F6, F9, F10	DGND	Ground	Not applicable	Digital Ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Ball Mnemonic	Ball Type	Signal Type	Description
E12, F2	SVDD2	Supply	Not applicable	2 V Nominal Supply for Digital Input/Output and SPI. Supports operation at 1.75 V minimum for compatibility with 1.8 V logic.
F7, F8, G5 to G10	DVDD	Supply	Not applicable	1 V Supply for Digital Core.
F11, G13	AVSSFS8	Ground	Not applicable	Ground for AVSSFS8 Supply Domain. Connect these pins to ground.
F12	SCLK	Input	Not applicable	Main SPI Clock Pin.
F13	CSB	Input	Not applicable	Chip Select Pin for SPI.
G2, H2	TMU_REFP, TMU_REFN	Input	Static	TMU Reference Supply and Ground. Connect TMU_REFP to a clean, 2 V reference supply on the board that is $\leq$ TMU_AVDD2. Connect TMU_REFN to clean ground on the board.
G3, H3	TDN, TDP	Input/Output	Static	Temperature Diode Cathode/Anode. These pins can be left floating if unused.
G4	TMU_DVDD1	Supply	Not applicable	Temperature Measurement Unit (TMU) Digital Domain Supply.
G11	AVDDFS8	Supply	Not applicable	1 V Supply for Clocks with $f_s/8$ Energy.
G12	SDIO	Input/output	Not applicable	Main SPI Input/Output Pin.
H1	FD	Output	CMOS	Fast Detect Pin.
H4, H11	VSS_MOAT	Ground	Not applicable	Ground for Isolation Guard Ring. Connect to ground.
H5 to H10, J14, K2 to K11, L6 to L11, M6, M9, M13, M14, N4, N6, N9, N12, N13, P1, P6, P9, P11, P14	AGND	Ground	Not applicable	Ground for ADC.
H12, J3 to J11, J13	AVDD	Supply	Not applicable	Analog Core 1 V Supply for ADC.
J1, J2	VDD_NVG	Supply	Not applicable	1 V supply for onboard Negative Voltage Generator (NVG).
K1	VNEG_OUT	Output	Not applicable	Internally Generated -1 V Output.
K13, L13	CLKVDD_LF	Supply	Not applicable	1 V Supply for Clock Buffer.
K14, L14	CLK_N, CLK_P	Input	Not applicable	Clock Inputs, High Frequency.
L1, L2	VSS_NVG	Ground	Not applicable	Supply Voltage (VSS) for NVG.
L3	TMU_AVDD2	Supply	Not applicable	TMU 2 V Analog Supply.
L4	RVDD2	Supply	Not applicable	TOP_REF 2 V Supply.
L5	BVDD3	Supply	Not applicable	Internally Generated 3 V Supply for Input Buffer.
M1, M2, M3, N2, P2	GPIO[4], GPIO[2], GPIO[3], GPIO[1], GPIO[0]	Input/output	Not applicable	General-Purpose Input/Output Pins. These pins can be left floating in default configuration.
M4	BVNN2	Supply	Not applicable	Internally Generated -2 V Supply for Input Buffer.
M5, N5, P5	BVNN1	Supply	Not applicable	-1 V Supply for Input Buffer.
M7, M8, N7, N8	VOID	Not applicable	Not applicable	No Balls at These Locations.
M10, N10, P10	BVDD2	Supply	Not applicable	2 V supply for Input Buffer.
M11	FVDD	Supply	Not applicable	1 V Supply for Reference ADC (REF_ADC).
M12	PLLVD2	Supply	Not applicable	2.0 V LDO Supply.
N1	RSTB	Input	Not applicable	Chip Reset, Active Low.
N11	PDWN	Input	CMOS	Active High Power-Down/Standby Mode Control.
P3	VCM	Output	Static	Export VCM.
P4	AVNN1	Supply	Not applicable	-1 V Supply for TOP_REF.
P7, P8	VIN_P, VIN_N	Input	RF	ADC Inputs, High Frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9217-6G

Nominal supply voltages, sampling rate = 6 GSPS, 1.4 V p-p full-scale differential input, $A_{IN} = -1.0$ dBFS, $T_J = 70^\circ\text{C}$, 128k FFT, unless otherwise noted.

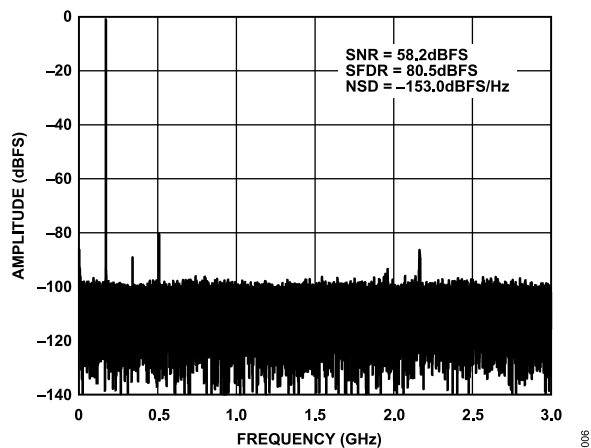


Figure 6. Single-Tone FFT with $f_{IN} = 170$ MHz, 6 GSPS

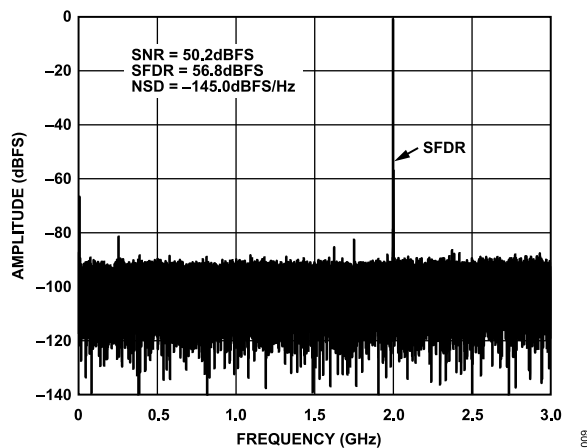


Figure 9. Single-Tone FFT with $f_{IN} = 4$ GHz, 6 GSPS

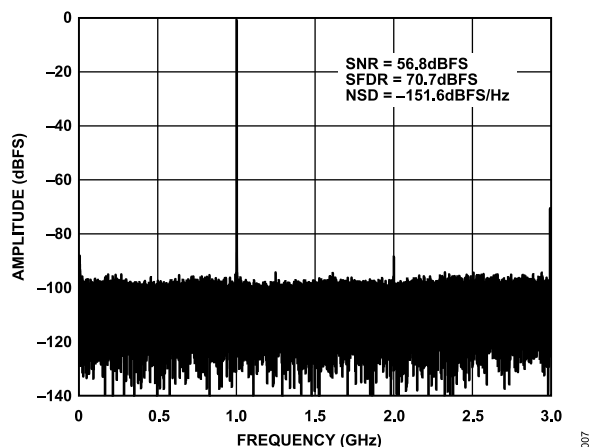


Figure 7. Single-Tone FFT with $f_{IN} = 1$ GHz, 6 GSPS

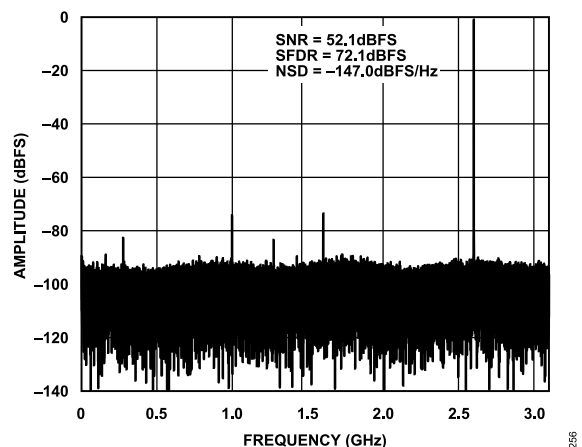


Figure 10. Single Tone FFT with $f_{IN} = 2.6$ GHz, Sampling Frequency = 6.2 GSPS

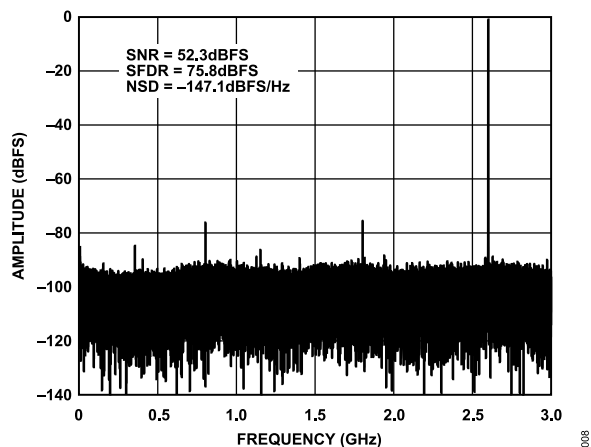


Figure 8. Single-Tone FFT with $f_{IN} = 2.6$ GHz, 6 GSPS

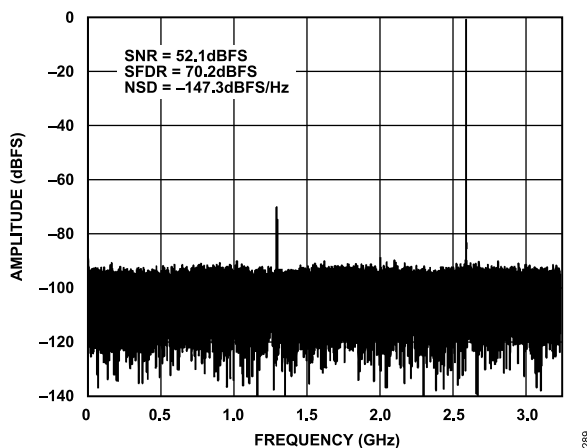
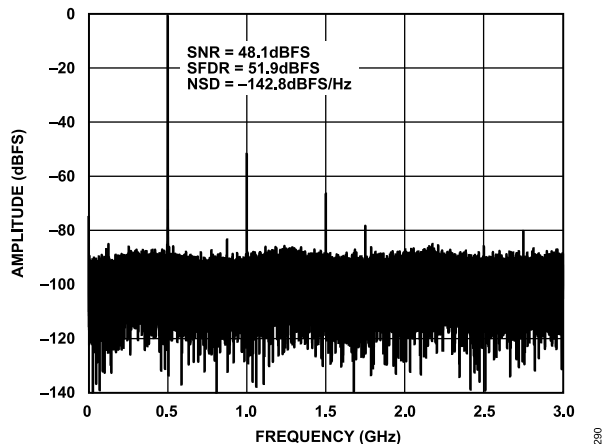
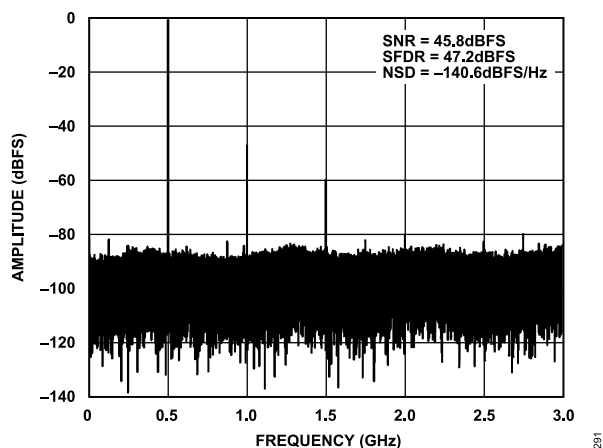
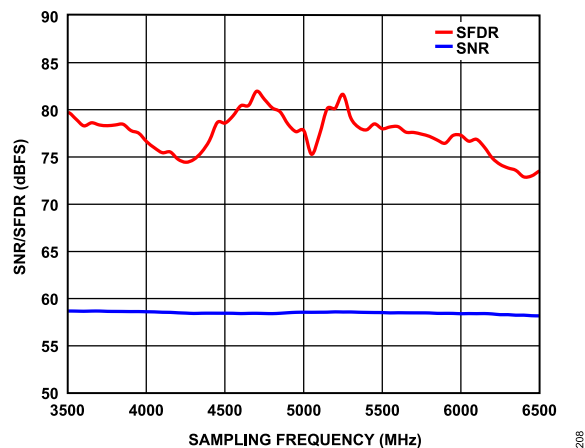
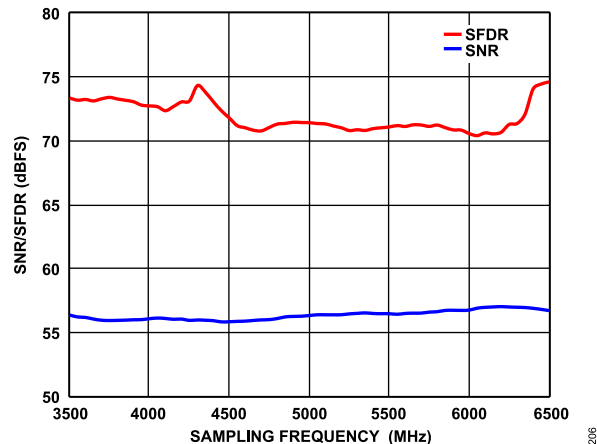
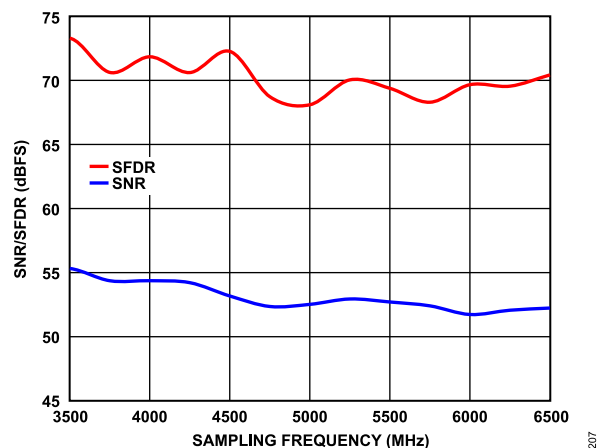
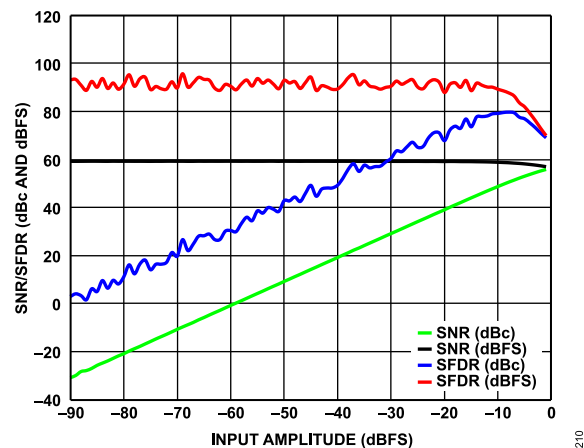
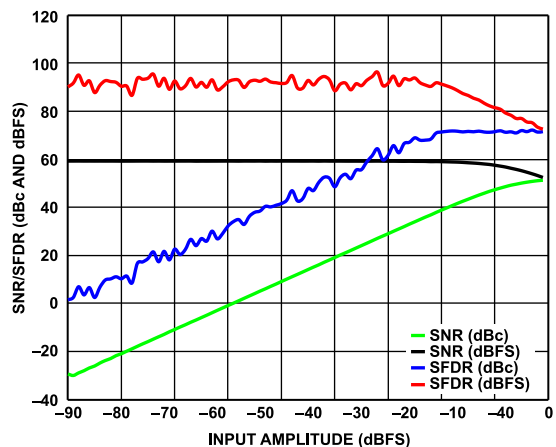


Figure 11. Single Tone FFT with $f_{IN} = 2.6$ GHz, Sampling Frequency = 6.5 GSPS

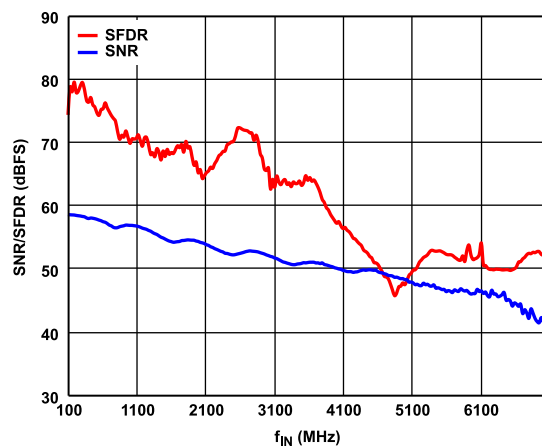
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 12. Single-Tone FFT with $f_{IN} = 5.5$ GHz, 6 GSPSFigure 13. Single-Tone FFT with $f_{IN} = 6.5$ GHz, 6 GSPSFigure 14. SNR/SFDR vs. Sampling Frequency, $f_{IN} = 170$ MHz, 6 GSPSFigure 15. SNR/SFDR vs. Sampling Frequency, $f_{IN} = 1000$ MHz, 6 GSPSFigure 16. SNR/SFDR vs. Sampling Frequency, $f_{IN} = 2.6$ GHz, 6 GSPSFigure 17. SNR/SFDR vs. Input Amplitude, $f_{IN} = 1000$ MHz, 6 GSPS

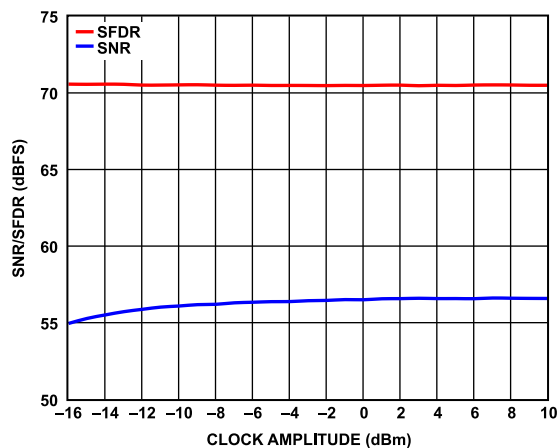
TYPICAL PERFORMANCE CHARACTERISTICS



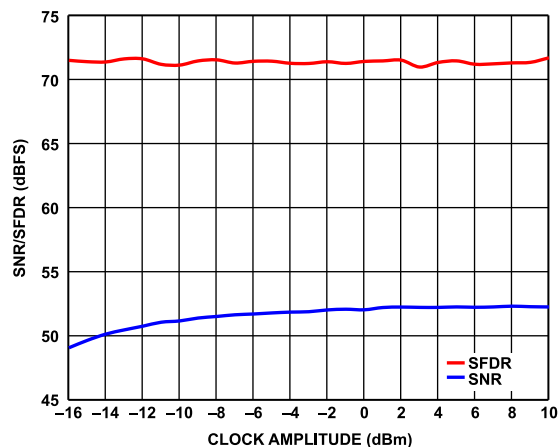
211

Figure 18. SNR/SFDR vs. Input Amplitude (A_{IN}), $f_{IN} = 2600$ MHz, 6 GSPS

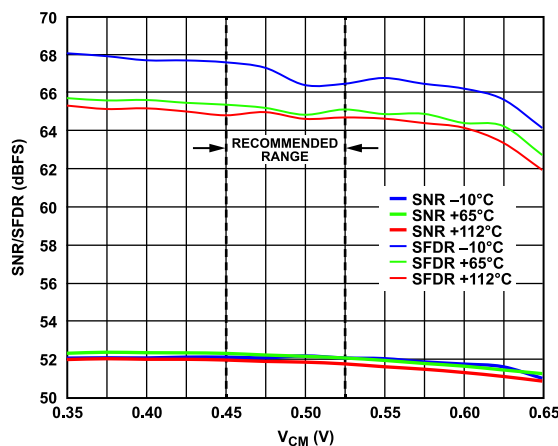
217

Figure 19. SNR/SFDR vs. f_{IN} , $A_{IN} = -1$ dBFS, 6 GSPS

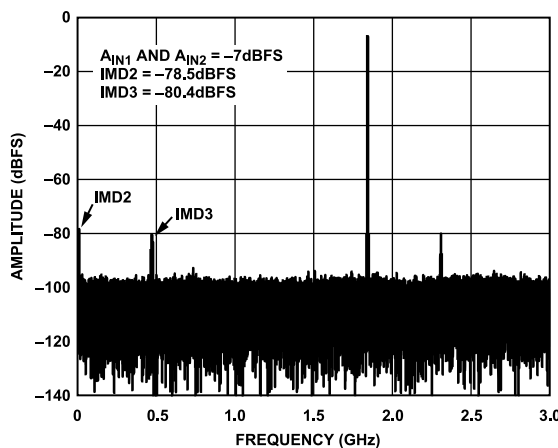
228

Figure 20. SNR/SFDR vs. Clock Amplitude at $f_{IN} = 1000$ MHz, 6 GSPS

229

Figure 21. SNR/SFDR vs. Clock Amplitude at $f_{IN} = 2600$ MHz, 6 GSPS

232

Figure 22. SNR/SFDR vs. V_{CM} , 6 GSPS

238

Figure 23. Two-Tone FFT, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS, 6 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

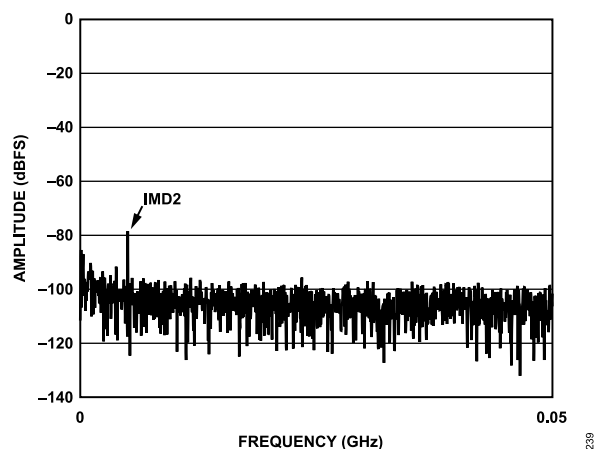


Figure 24. Two-Tone FFT, IMD2 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 23), 6 GSPS

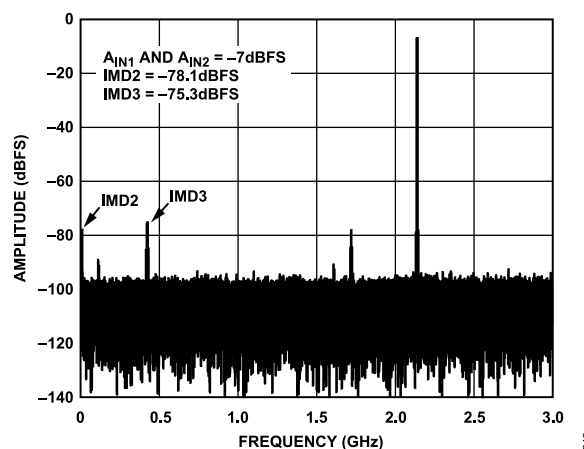


Figure 27. Two-Tone FFT, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS, 6 GSPS

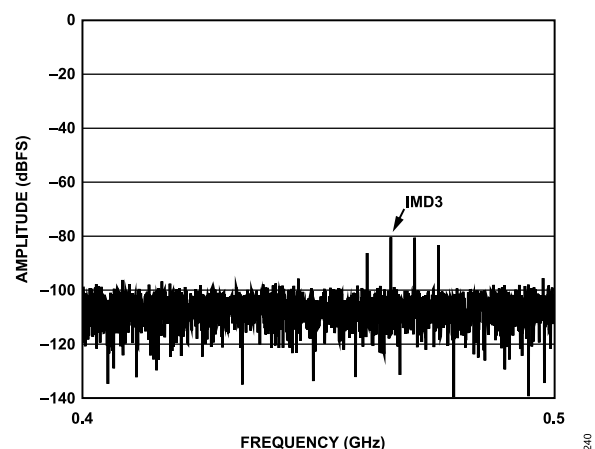


Figure 25. Two-Tone FFT, IMD3 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 23), 6 GSPS

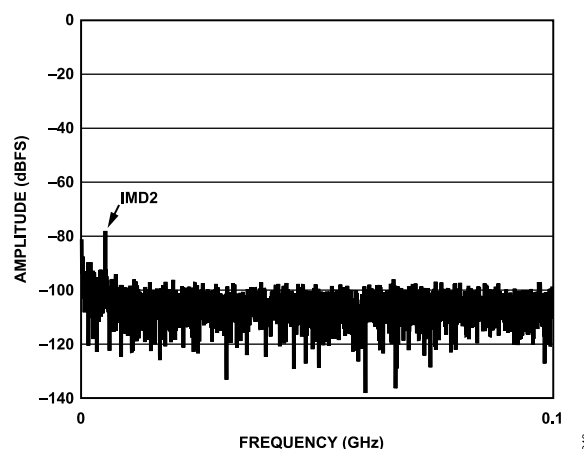


Figure 28. Two-Tone FFT, IMD2 Zoom In, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS, 6 GSPS

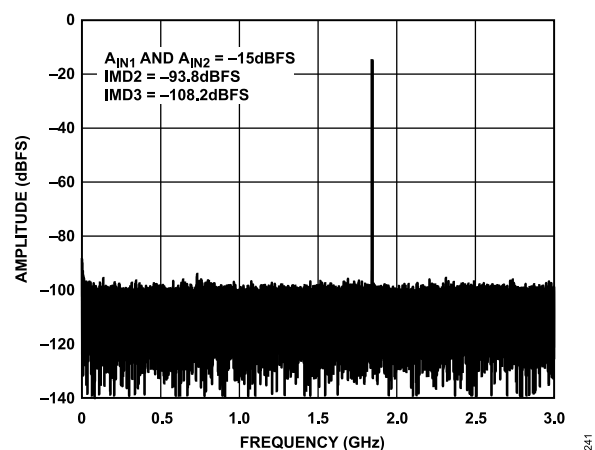


Figure 26. Two-Tone FFT, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS, 6 GSPS

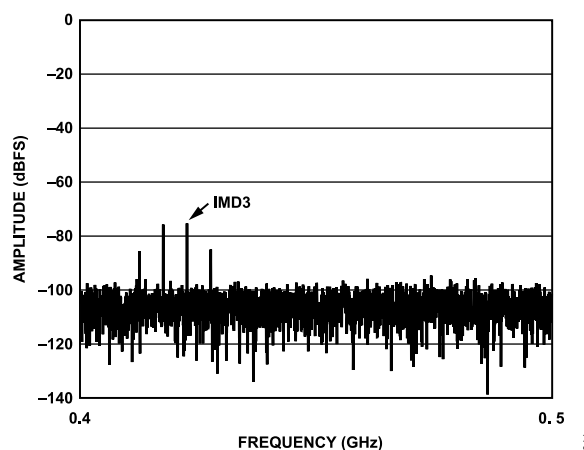


Figure 29. Two-Tone FFT, IMD3 Zoom In, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS, 6 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

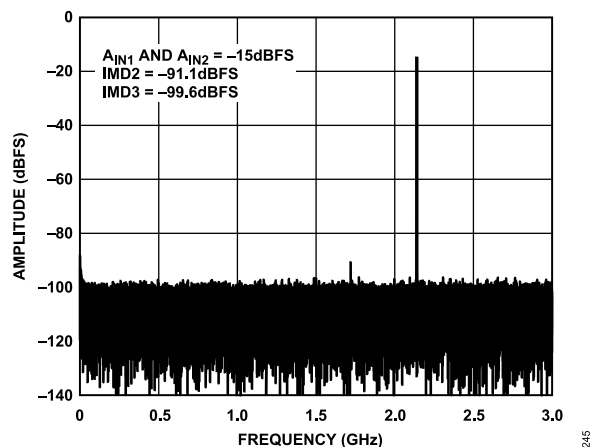


Figure 30. Two-Tone FFT, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS, 6 GSPS

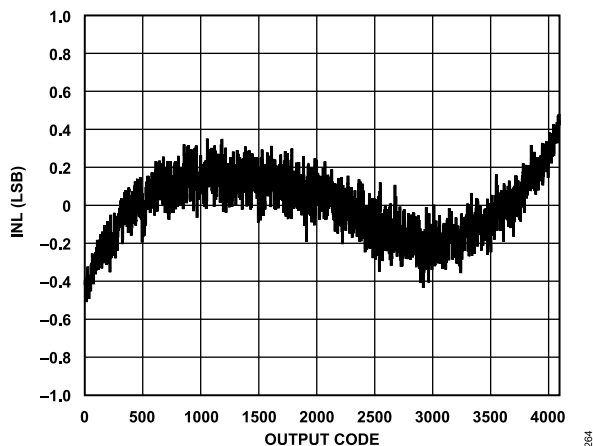


Figure 31. INL at $f_{IN} = 170$ MHz, 6 GSPS

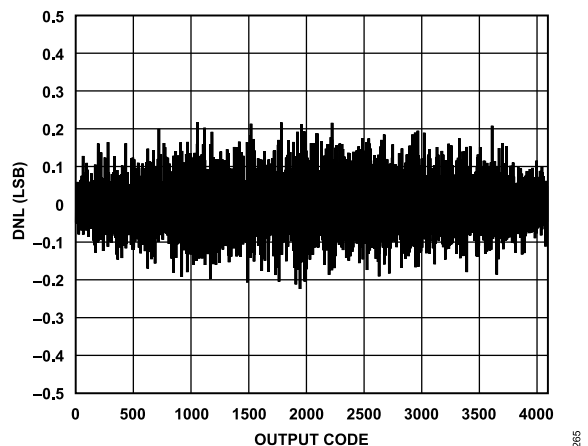


Figure 32. DNL at $f_{IN} = 170$ MHz, 6 GSPS

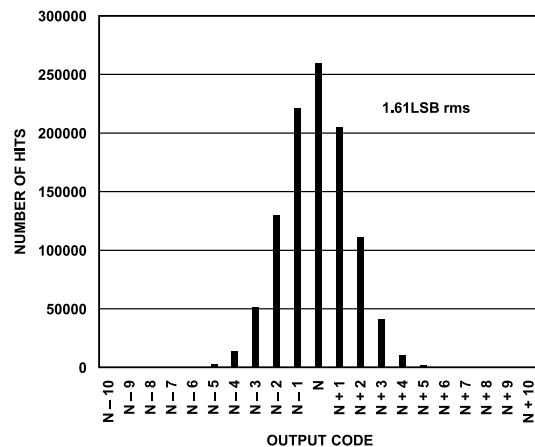


Figure 33. Input Referred Noise Histogram, 6 GSPS

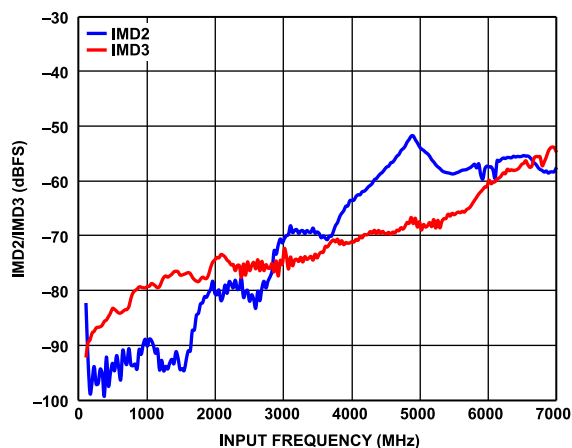


Figure 34. IMD2/IMD3 vs. Input Frequency ($A_{IN} = -7$ dBFS), 10 MHz Spacing, 6 GSPS

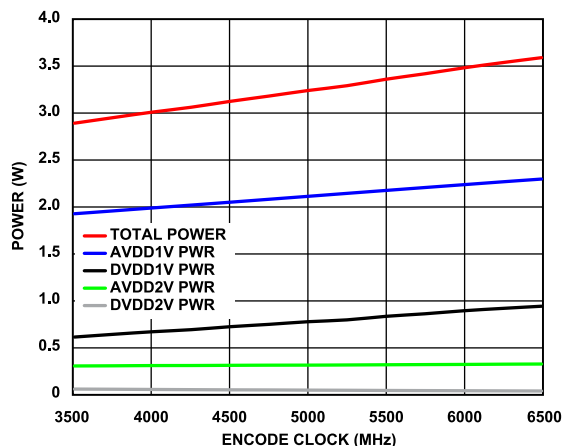


Figure 35. Power vs. Encode Clock (f_S), $f_{IN} = 2600$ MHz

TYPICAL PERFORMANCE CHARACTERISTICS

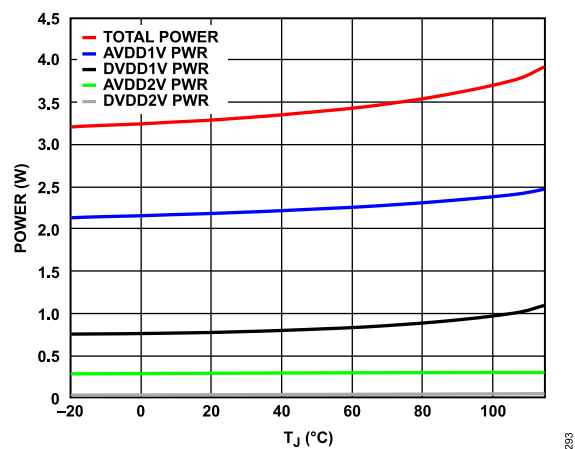


Figure 36. Power vs. Junction Temperature (T_J), $f_{IN} = 2600\text{ MHz}$, 6 GSPS

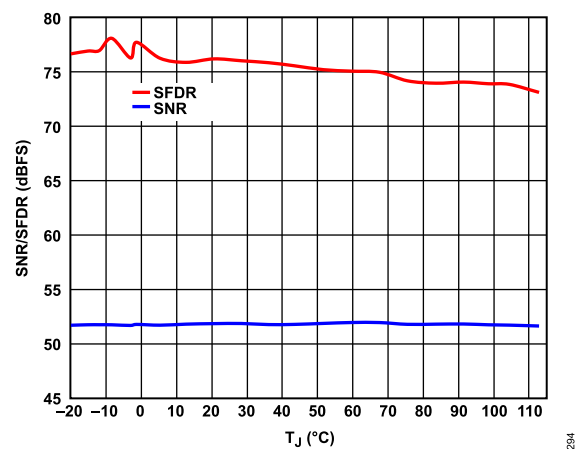


Figure 37. SNR/SFDR vs. T_J , $f_{IN} = 2600\text{ MHz}$, 6 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

AD9217-10G

Nominal supply voltages, sampling rate = 10 GSPS, 1.4 V p-p full-scale differential input, $A_{IN} = -1.0$ dBFS, $T_J = 70^\circ\text{C}$, 128k FFT, unless otherwise noted.

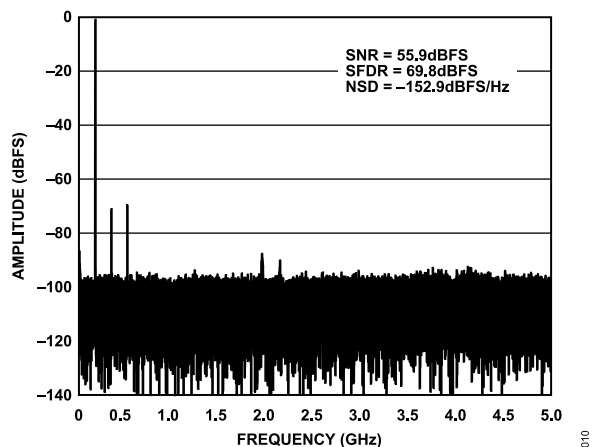


Figure 38. Single-Tone FFT with $f_{IN} = 170$ MHz, 10 GSPS

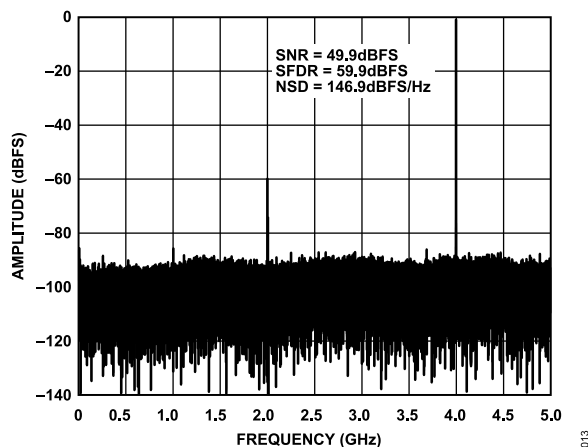


Figure 41. Single-Tone FFT with $f_{IN} = 4$ GHz, 10 GSPS

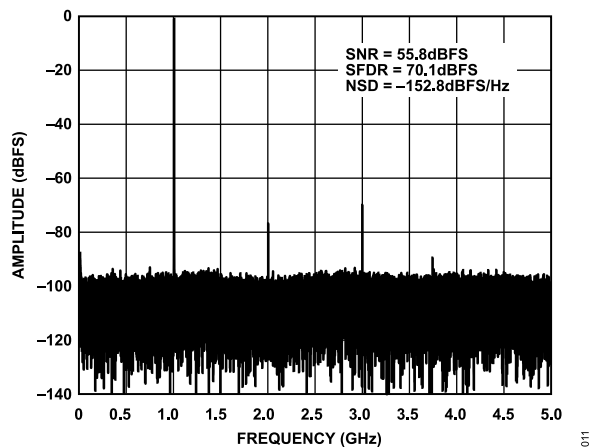


Figure 39. Single-Tone FFT with $f_{IN} = 1$ GHz, 10 GSPS

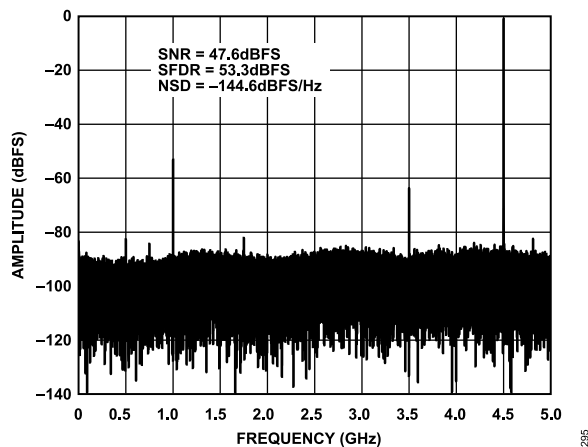


Figure 42. Single-Tone FFT with $f_{IN} = 5.5$ GHz, 10 GSPS

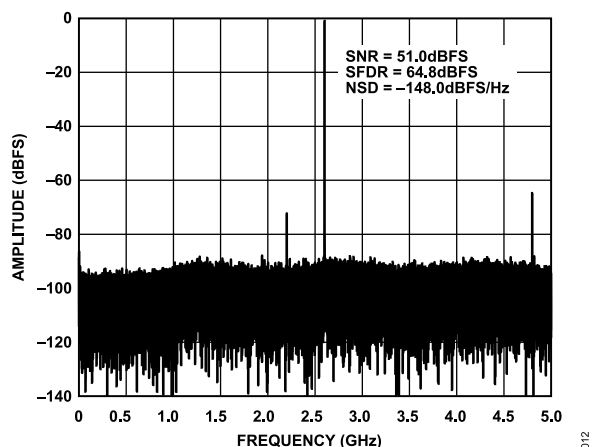


Figure 40. Single-Tone FFT with $f_{IN} = 2.6$ GHz, 10 GSPS

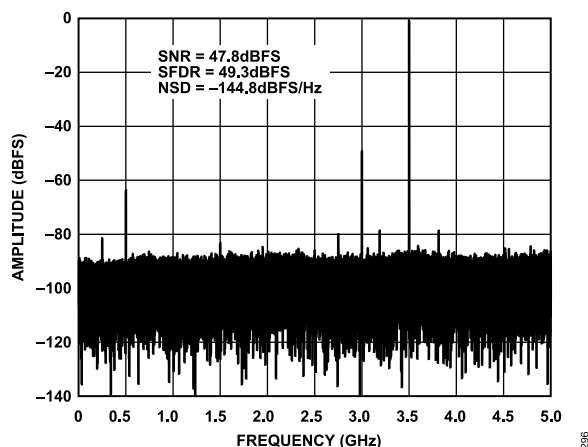
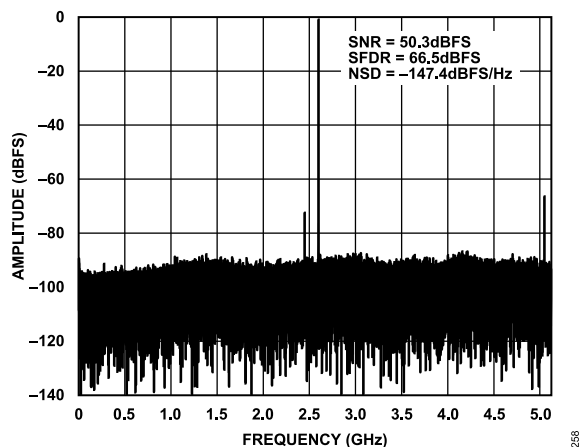
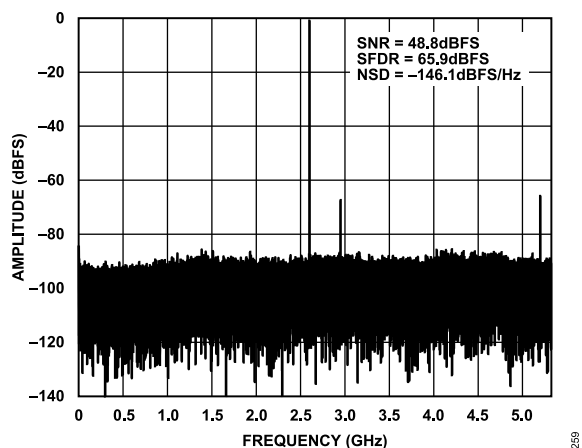
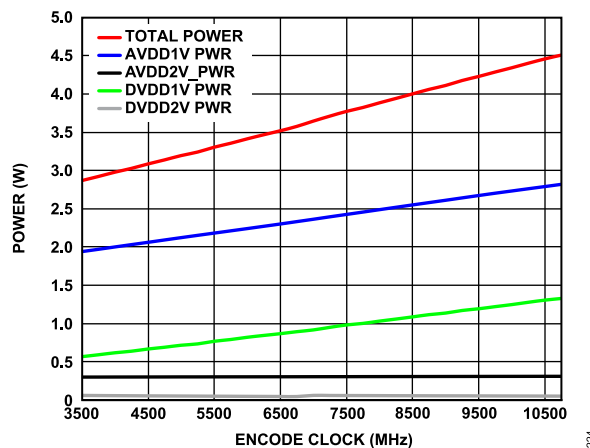
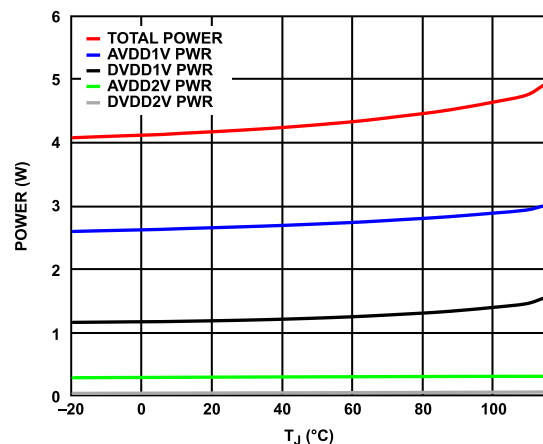
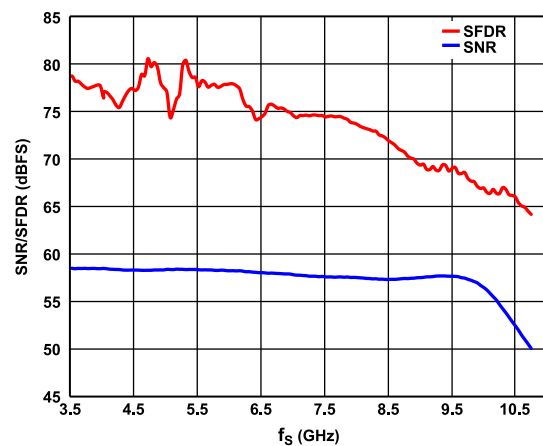
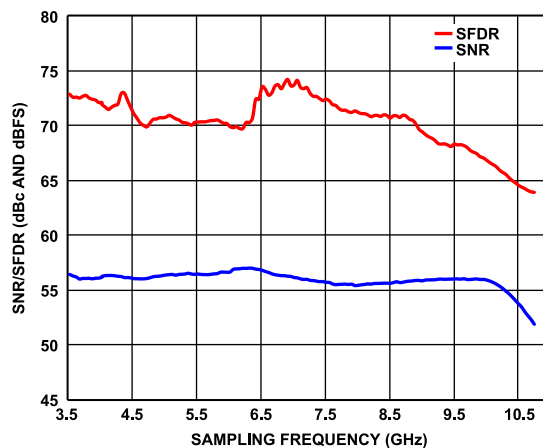
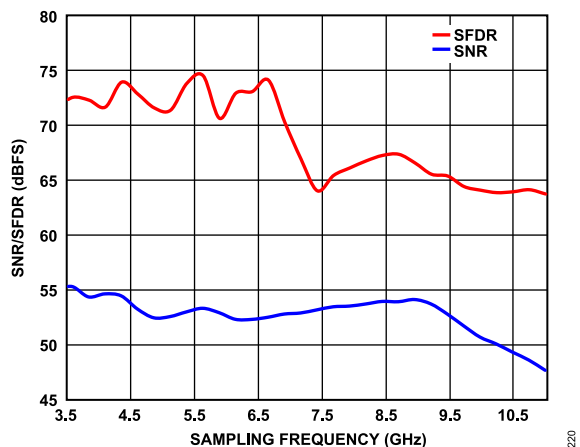
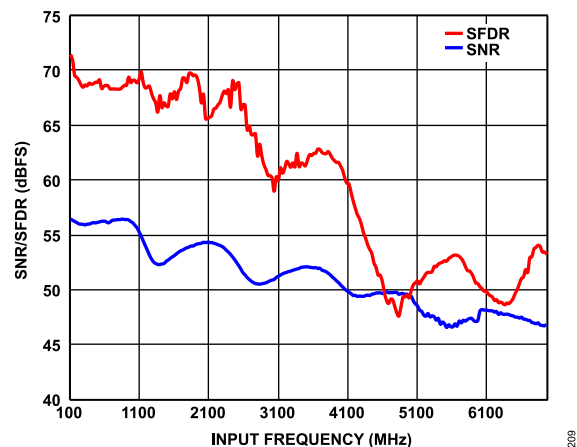
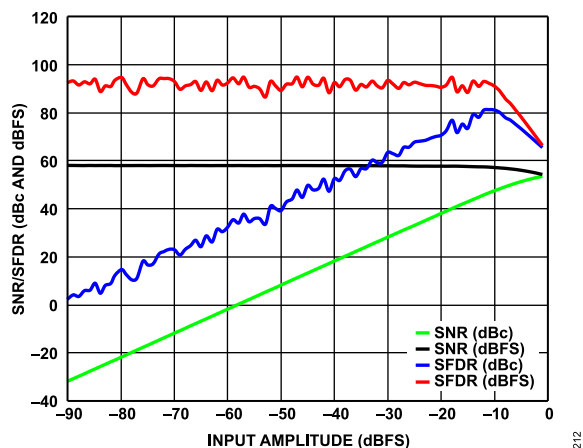
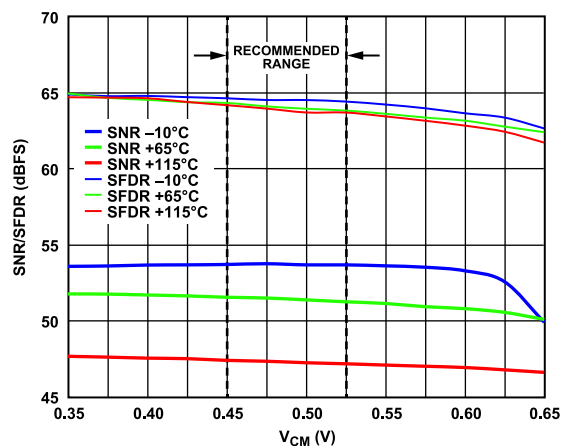
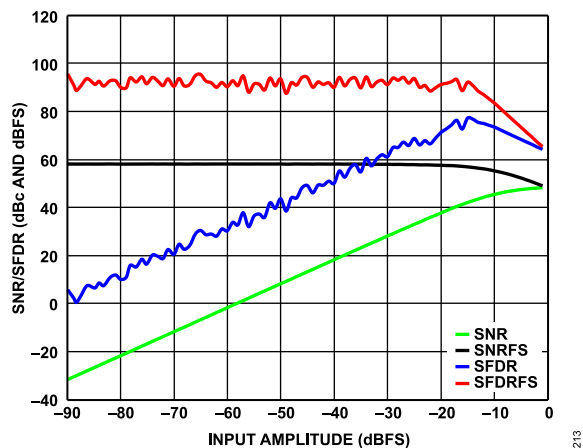
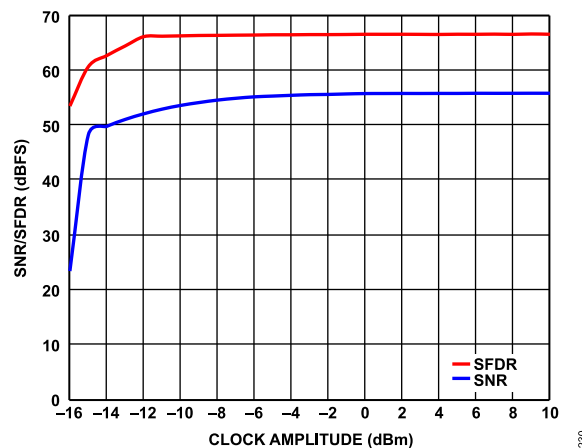


Figure 43. Single-Tone FFT with $f_{IN} = 6.5$ GHz, 10 GSPS

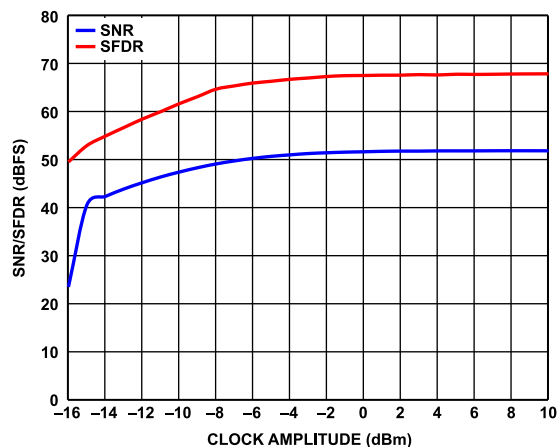
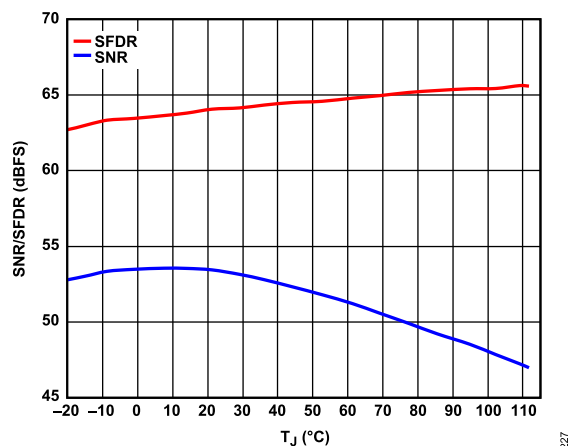
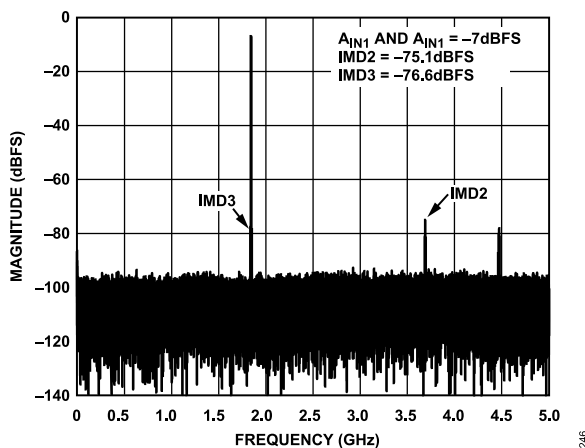
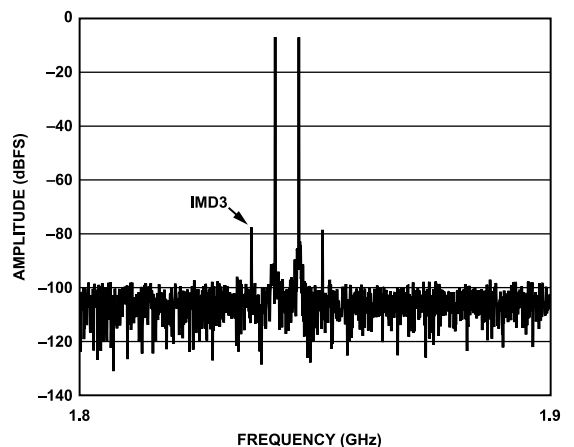
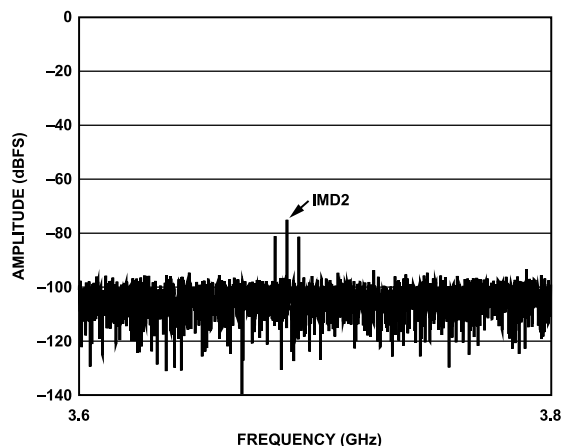
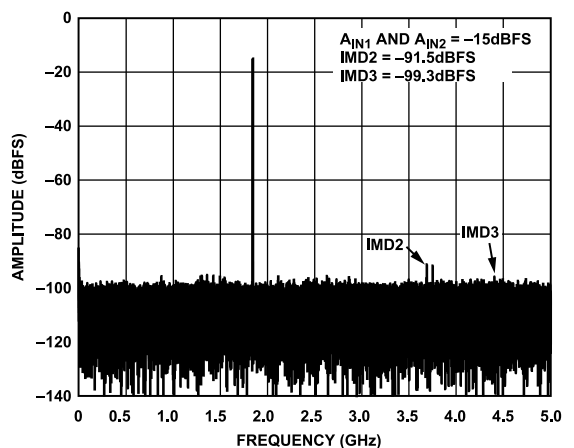
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 44. Single-Tone FFT with $f_{IN} = 2.6$ GHz, 10.25 GSPSFigure 45. Single Tone FFT with $f_{IN} = 2.6$ GHz, 10.75 GSPSFigure 46. Total Power vs. Encode Clock (f_s), $f_{IN} = 170$ MHz, 10 GSPSFigure 47. Power vs. Junction Temperature (T_J), $f_{IN} = 2600$ MHz, 10 GSPSFigure 48. SNR/SFDR vs. Sampling Frequency, $f_{IN} = 170$ MHzFigure 49. SNR/SFDR vs. Sampling Frequency (f_s), $f_{IN} = 1000$ MHz, 10 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 50. SNR/SFDR vs. Sampling Frequency, $f_{IN} = 2600$ MHz, 10 GSPSFigure 53. SNR/SFDR vs. Input Frequency (f_{IN}), $A_{IN} = -1$ dBFS, 10 GSPSFigure 51. SNR/SFDR vs. Input Amplitude, $f_{IN} = 1000$ MHz, 10 GSPSFigure 54. SNR/SFDR vs. V_{CM} , 10 GSPSFigure 52. SNR/SFDR vs. Input Amplitude (A_{IN}), $f_{IN} = 2600$ MHz, 10 GSPSFigure 55. SNR/SFDR vs. Clock Amplitude, $f_{IN} = 1000$ MHz, 10 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 56. SNR/SFDR vs. Clock Amplitude, $f_{IN} = 2600$ MHz, 10 GSPSFigure 57. SNR/SFDR vs. T_J , $f_{IN} = 2600$ MHz, 10 GSPSFigure 58. Two-Tone FFT, 10 GSPS, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFSFigure 59. Two-Tone FFT, IMD3 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 58), 10 GSPSFigure 60. Two-Tone FFT, IMD2 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 58), 10 GSPSFigure 61. Two-Tone FFT, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS, 10 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

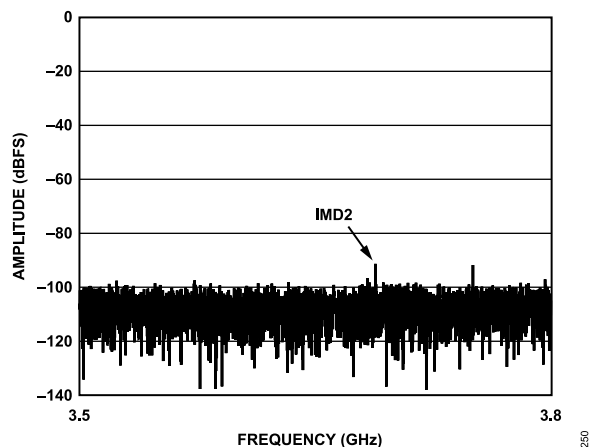


Figure 62. Two-Tone FFT, IMD2 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS (see Figure 61), 10 GSPS

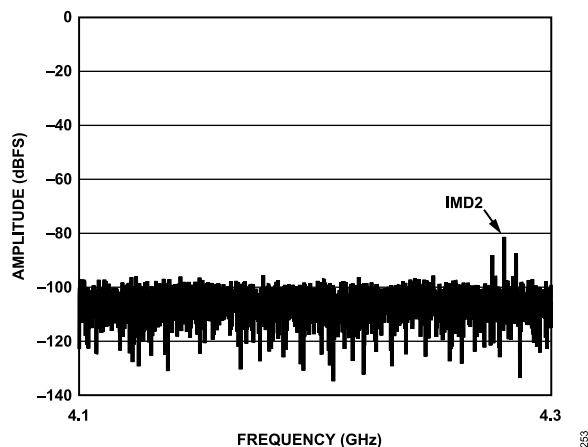


Figure 65. Two-Tone FFT, IMD2 Zoom In, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 64), 10 GSPS

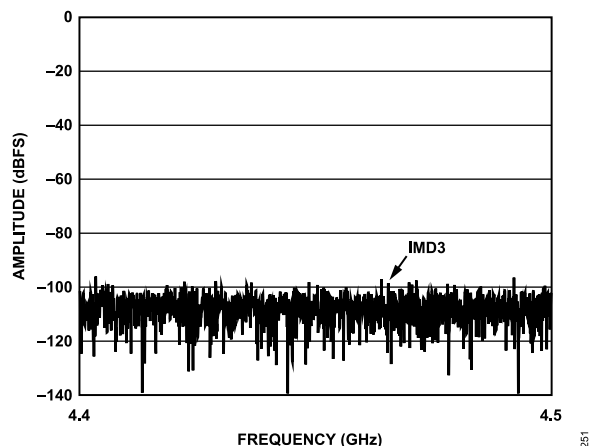


Figure 63. Two-Tone FFT, IMD3 Zoom In, $f_{IN1} = 1841.5$ MHz, $f_{IN2} = 1846.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS (see Figure 61), 10 GSPS

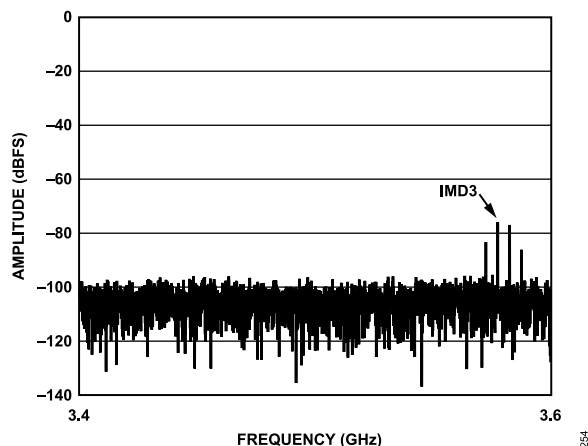


Figure 66. Two-Tone FFT, IMD3 Zoom In, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS (see Figure 64), 10 GSPS

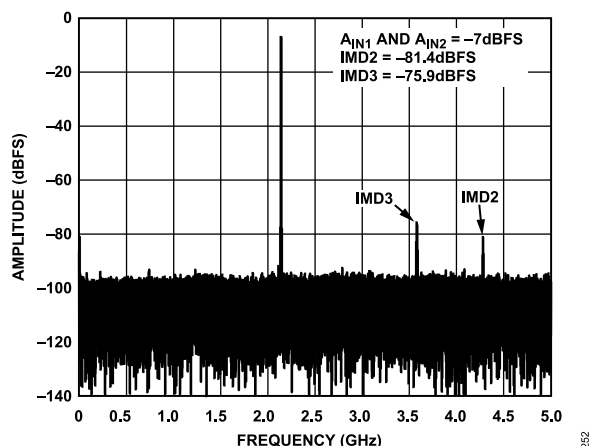


Figure 64. Two-Tone FFT, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -7$ dBFS, 10 GSPS

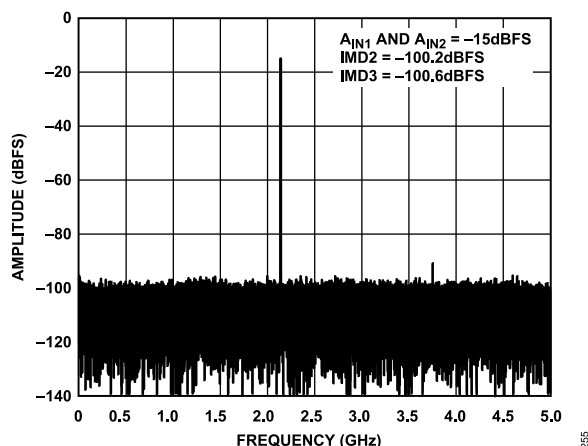


Figure 67. Two-Tone FFT, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, A_{IN1} and $A_{IN2} = -15$ dBFS, 10 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

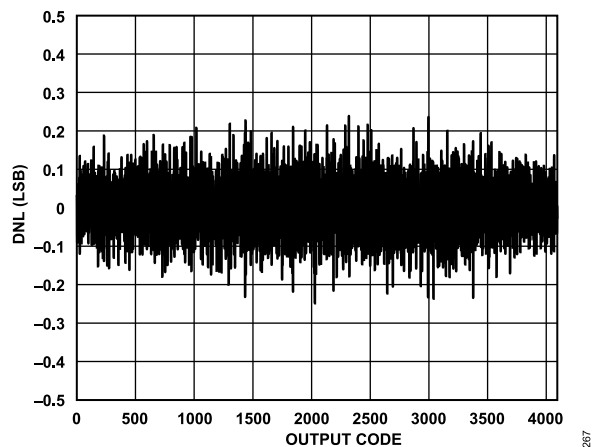
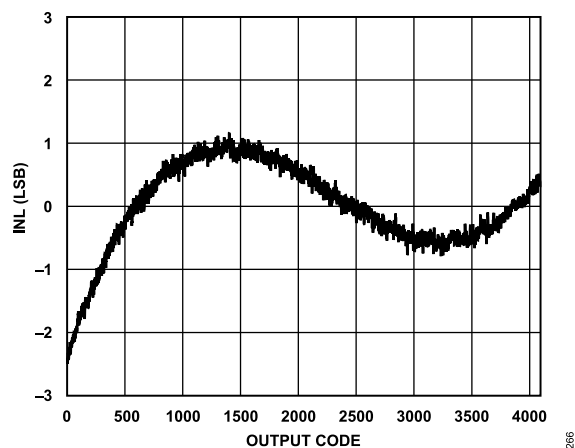
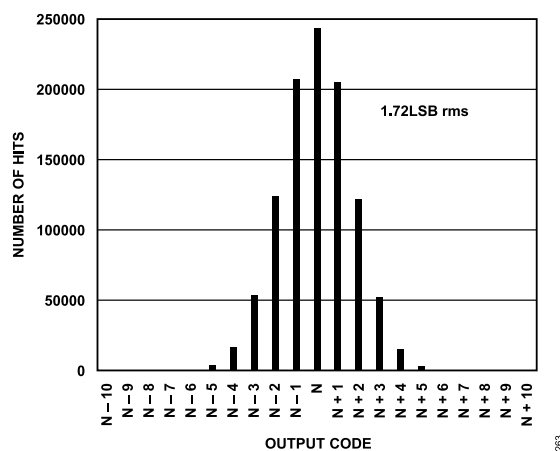
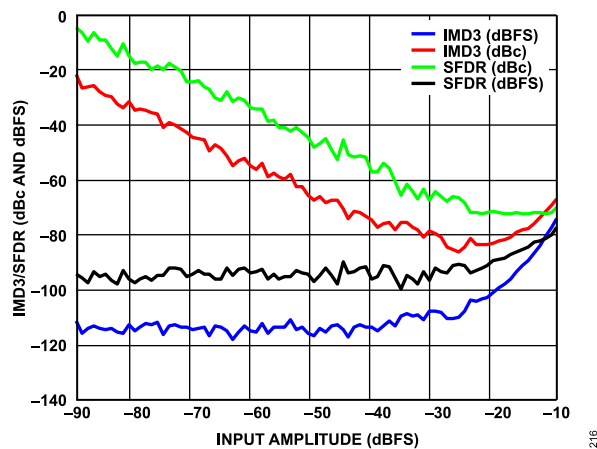
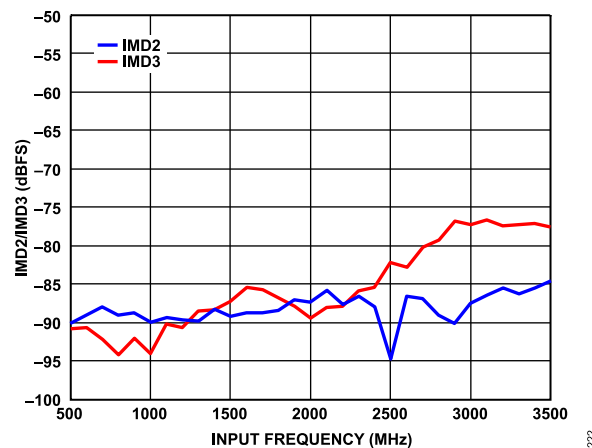
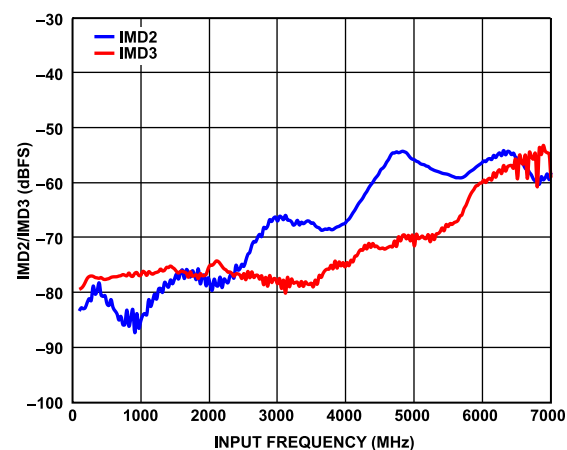
Figure 68. DNL at $f_{IN} = 170$ MHz, 10 GSPSFigure 69. INL at $f_{IN} = 170$ MHz, 10 GSPS

Figure 70. Input-Referred Noise Histogram, 10 GSPS

Figure 71. IMD3/SFDR vs. Input Amplitude, $f_{IN1} = 2137.5$ MHz, $f_{IN2} = 2142.5$ MHz, 10 GSPSFigure 72. IMD2/IMD3 vs. Input Frequency, ($A_{IN} = -7$ dBFS), 100 MHz Spacing, 10 GSPSFigure 73. IMD2/IMD3 vs. Input Frequency ($A_{IN} = -7$ dBFS), 10 MHz Spacing, 10 GSPS

TYPICAL PERFORMANCE CHARACTERISTICS

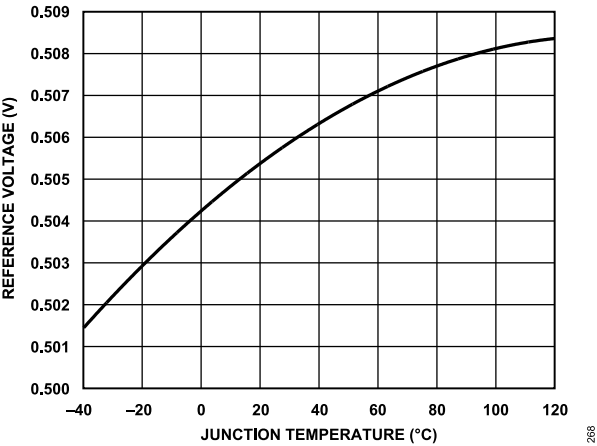


Figure 74. Reference Voltage vs. Junction Temperature, 10 GSPS

EQUIVALENT CIRCUITS

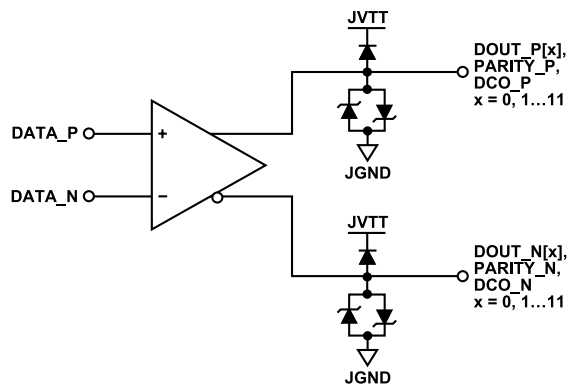


Figure 75. Digital Outputs

100

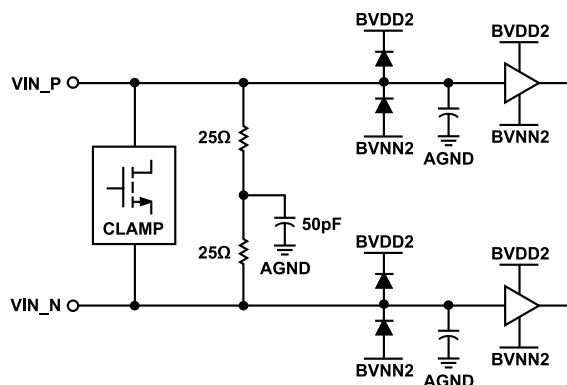


Figure 76. Analog Inputs

101

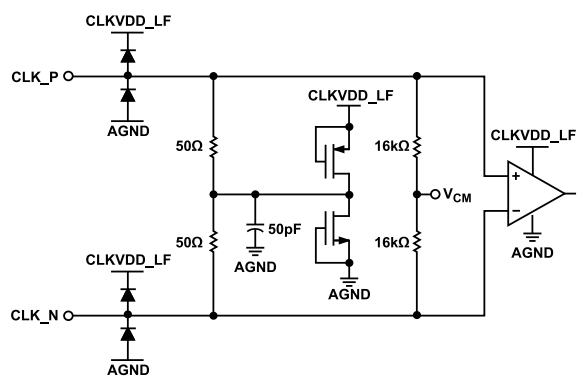


Figure 77. Clock Inputs

102

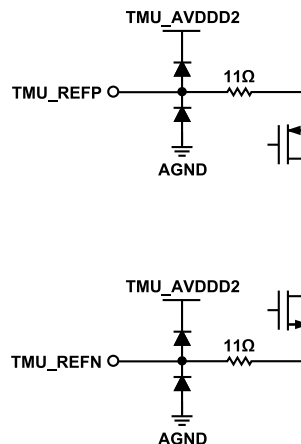


Figure 78. TMU_REFx Inputs

106

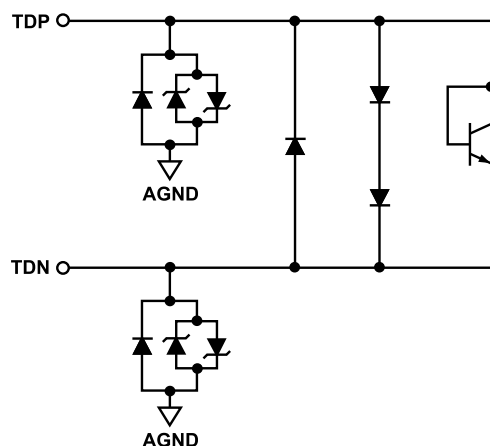
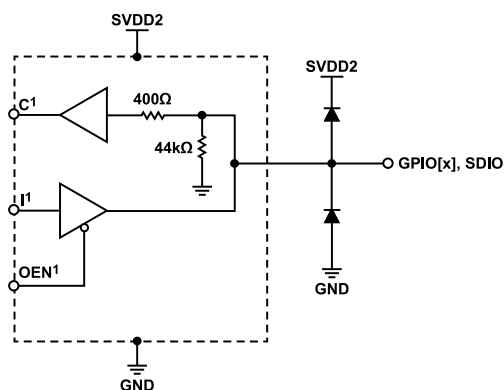


Figure 79. TDx Temperature Diodes

107



¹C, I, AND OEN ARE INTERNAL NODES AND ARE NOT USER ACCESSIBLE.

109

Figure 80. GPIO[x] and SDIO

EQUIVALENT CIRCUITS

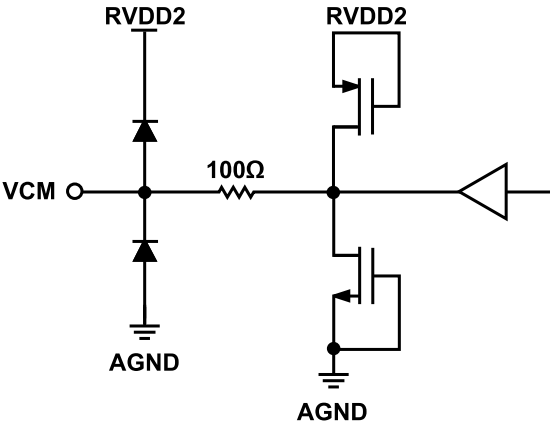
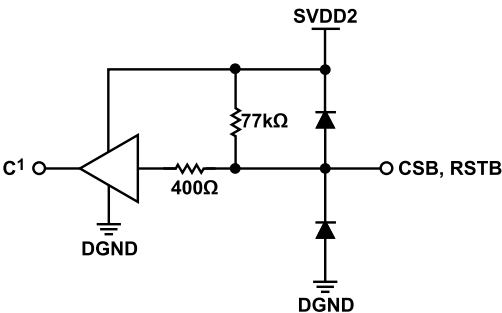


Figure 81. VCM

110



¹C IS AN INTERNAL NODE AND IS NOT USER ACCESSIBLE.

112

Figure 82. CSB and RSTB

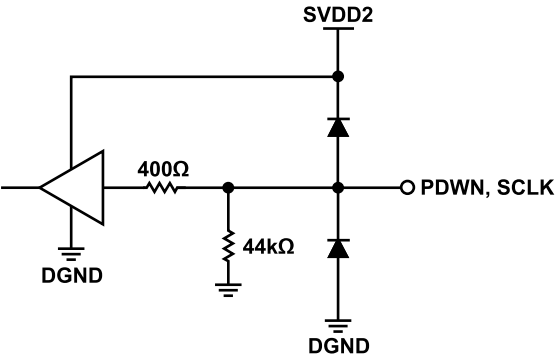
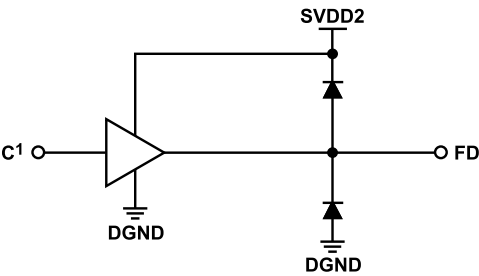


Figure 83. PDWN and SCLK

113



¹C IS AN INTERNAL NODE AND IS NOT USER ACCESSIBLE.

114

Figure 84. FD

THEORY OF OPERATION

The AD9217 is a single, 12-bit ADC with high speed parallel CML outputs. The ADC is designed to sample wide bandwidth analog signals of up to 6.5 GHz. The AD9217 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The AD9217 analog input features wide input bandwidth that supports a variety of input ranges. An integrated voltage reference eases design considerations.

A programmable threshold detector allows monitoring of the signal power in the digital backend of the ADC. If the signal level exceeds the programmable threshold, the FD indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

ADC ARCHITECTURE

The architecture of the AD9217 consists of an input buffered, pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal of 50 Ω . The equivalent circuit diagram of the analog input termination is shown in [Figure 76](#). The input buffer is optimized for high linearity, low noise, and low power.

The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample. Simultaneously, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9217 is a differential buffer. The internal common-mode voltage of the buffer is $AVDD/2$ (nominally 0.5 V). The clock signal alternately switches the input circuit between sample mode and hold mode.

At radio frequencies, care must be taken when designing the network between the signal source and the AD9217 inputs.

Additional loading affects bandwidth and possibly signal integrity. For more information, refer to the *Analog Dialogue* article [Transformer-Coupled Front-End for Wideband A/D Converters](#) (Volume 39, April 2005). In general, the specific configuration and component values depend on the application.

For best dynamic performance, the source impedances driving VIN_P and VIN_N must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Differential Input Configurations

There are several ways to drive the AD9217, either actively or passively. However, optimal performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration, because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9217.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimal performance of the AD9217. For higher frequencies, remove some of the front-end passive components to ensure wideband operation.

Input Common Mode

The analog inputs of the AD9217 are internally biased to the common mode (0.50 V) by default.

In dc-coupled applications, the V_{CM} of the signal source must be biased to 0.50 V to ensure proper ADC operation. For these applications, the internal biasing of the input buffer must be disabled, and the dc offset nulling must also be disabled.

The following is pseudo code for the register writes to configure the input buffer for dc coupling.

For dc coupling, without using the VCM output pin, make the following writes: Register 0x1617 = 0x01, dc coupling mode, nulling disabled, and Register 0x151A = 0x00, internal biasing disabled, VCM output disabled.

For DC coupling, with the VCM output pin enabled, make the following writes: Register 0x1617 = 0x01, dc coupling mode, nulling disabled, and Register 0x151A = 0x02, internal biasing disabled, VCM output enabled (for providing VCM level to a driver amplifier).

After writing to Register 0x1617, Register 0x1600, Bit 0 must be set to apply the latest setting.

The VCM output can be used to set the VCM of an amplifier driving AD9217. The VCM output buffer has a series output resistance of 100 Ω . A load on the VCM pin reduces the output voltage, which must be accounted for when loading the VCM output. The VCM output is not intended to drive high fanout, multiple load applications.

See [Figure 22](#) and [Figure 54](#) for information regarding variation in typical performance with respect to the V_{CM} .

Input Overvoltage Clamp

The AD9217 has an on-chip overvoltage clamp placed differentially across the ADC analog inputs to protect the input buffer of the device from large voltage excursions, as shown in [Figure 85](#). During an overvoltage event, this N-type metal-oxide semiconductor (NMOS) clamp effectively shorts the on-chip, 50 Ω , differential input termination, attenuating the input level. The clamping circuit detects differential overvoltage. The clamp attenuation is at its maximum at

THEORY OF OPERATION

$f_{IN} < 250$ MHz. When the $f_{IN} > 250$ MHz, clamp circuit attenuation levels are lower. Higher input frequencies result in a higher clamp threshold and a higher clamped input level.

Adding board-level circuitry to protect the ADC inputs from periodic, large voltage excursions often compromises system performance. This built in clamp allows increased typical input voltage levels and improved system performance.

During an overvoltage event, the active clamp circuit reduces the on-chip, ADC input $50\ \Omega$ differential termination (load termination resistance seen by the ADC signal source).

This reduction can cause reflections back to the circuitry that drives the ADC. Ensure that the driving circuitry is not damaged by potential large signals created with these reflections.

The user must ensure system reliability at their system specific conditions.

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9217. This internal reference is used to set the full-scale input range of the ADC.

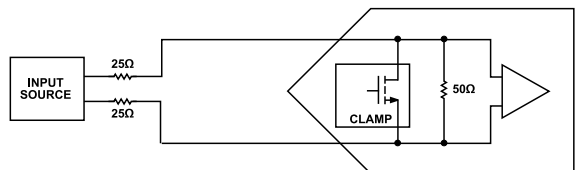


Figure 85. Input Overvoltage Clamp

THEORY OF OPERATION

CLOCK INPUT CONSIDERATIONS

The AD9217 has a low jitter clock receiver. For optimum performance, drive the AD9217 sample clock inputs (CLK_x) with a differential signal. This signal is typically ac-coupled to the CLK_x pins via a transformer or clock drivers. These pins are biased internally and require no additional external biasing.

Clock Jitter

High speed, high resolution ADCs are sensitive to the quality of the clock signal.

The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated with the following equation:

$$SNR = 20 \times \log 10 (2 \times \pi \times f_A \times t_J) \quad (1)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications.

Higher frequencies are increasingly sensitive to jitter (see [Figure 86](#)).

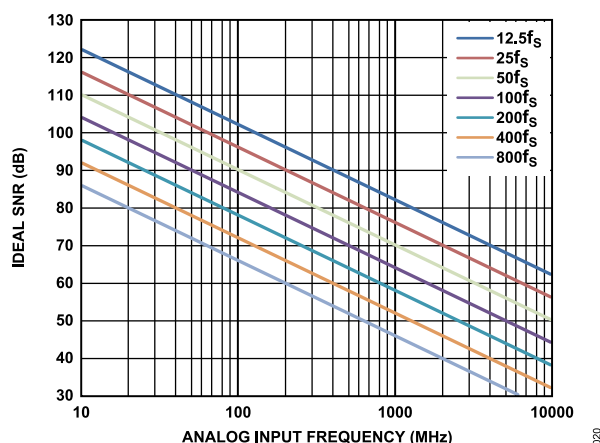


Figure 86. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter can affect the dynamic range of the AD9217. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the [AN-501 Application Note](#) and the [AN-756 Application Note](#) for more information about jitter performance as it relates to ADCs.

Power-Down/Standby Mode

The AD9217 has an active high PDWN pin that can be used to configure the device in power-down or standby mode.

Temperature Diode and Sensor

A thermal monitoring unit (TMU) is designed into the AD9217. The die temperature can be read by SPI as described in the [TMU](#) section.

The AD9217 also contains a diode-based temperature sensor for measuring the temperature of the die. This diode can be used in conjunction with external support components to serve as a coarse temperature sensor to monitor the internal die temperature.

TMU

The AD9217 contains a TMU that functions as a digital thermometer. The TMU is comprised of five sensors placed at different chip locations. The on-die temperature value is measured and digitized through an ADC.

At any given time, the value from the sensor with the highest temperature is stored in Register 0x1609, Bits[7:0] and Register 0x160A, Bits[7:0]. These values combine to give a 16-bit maximum temperature word. Similarly, the value from the sensor with the lowest temperature is stored in Register 0x160D, Bits[7:0] and Register 0x160E, Bits[7:0], and these values combine to give a 16-bit minimum temperature word.

The nine MSBs of each 16-bit temperature word are the integer portion of the die temperature in twos complement. The seven LSBs represent the fractional portion of the temperature, that is, the digits to the right of the decimal place. For example, the most significant of the seven LSBs represents 2^{-1} and the next bit to the right is 2^{-2} .

The following procedure is an example of obtaining the value of the sensor that produces the highest temperature reading. The procedure to reading the minimum temperature is the same as the procedure to read the maximum temperature, but with different register addresses, depending on which temperature level is read.

To obtain the maximum temperature, read Register 0x1609 (maximum temperature word containing the eight LSBs) and Register 0x160A (maximum temperature word containing the eight MSBs).

For example,

1. Register 0x1609 = 0x76 = 01110110b.
2. Register 0x160A = 0x2C = 00101100b.
3. Concatenate the MSBs to the LSBs to give a 16-bit word: Register 0x2C76 = 0010110001110110b.
4. The nine MSBs of this word represent the twos complement integer value of the temperature in degrees Celsius:

001011000 (twos complement) = 88 (decimal).
5. The seven LSBs of the 16-bit word are the fractional portion where the most significant (left most) bit value is 2^{-1} , the next is 2^{-2} , and so on. Using this convention, 1110110 = 0.92188 (decimal).

Therefore, the die temperature reported by the highest reading sensor is $88^{\circ}\text{C} + 0.92188^{\circ}\text{C} = 88.92188^{\circ}\text{C}$. The accuracy of the TMU is typically $\pm 2^{\circ}\text{C}$, and the fractional portion of the temperature value has limited significance.

Table 9. TMU Register Summary

Address	Register Name	Bits	Description	Reset	Access
0x1609	MAX_TEMPERATURE_LSB	[7:0]	Bits[7:0] of maximum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160A	MAX_TEMPERATURE_MSB	[7:0]	Bits[15:8] of maximum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160D	MIN_TEMPERATURE_LSB	[7:0]	Bits[7:0] of minimum temperature of all temperature sensors. Q9.7 format.	0x0	R
0x160E	MIN_TEMPERATURE_MSB	[7:0]	Bits[15:8] of minimum temperature of all temperature sensors. Q9.7 format.	0x0	R

ADC FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9217 contains fast detect circuitry to monitor the threshold and assert the FD pin.

FAST THRESHOLD DETECTION (FD)

The fast detect bit is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

Figure 87 shows the operation of the upper threshold and lower threshold registers, along with the dwell time registers.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x101 and Register 0x102. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 200 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\text{Upper Threshold Magnitude (dBFS)} = 20\log(\text{Threshold Magnitude}/2^{11}) \quad (2)$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x103 and Register 0x104. The fast detect lower threshold register is an 11-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\text{Lower Threshold Magnitude (dBFS)} = 20\log(\text{Threshold Magnitude}/2^{11}) \quad (3)$$

For example, to set an upper threshold of -6 dBFS, write 0x3FF to Register 0x101 and Register 0x102. To set a lower threshold of -10 dBFS, write 0x287 to Register 0x103 and Register 0x104.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x105 and Register 0x106.

In addition to the fast detect configuration registers (Register 0x100 through Register 0x106), Register 0x160F, Bit 0 must be set to enable the FD pin. After writing to Register 0x160F, Register 0x1600, Bit 0 must be set to apply the latest setting.

Write Register 0x160F = 0x01 (fast detect (FD) pin enable).

Write Register 0x1600 = 0x01 (self clearing transfer bit).

See the [Memory Map](#) section for more details.

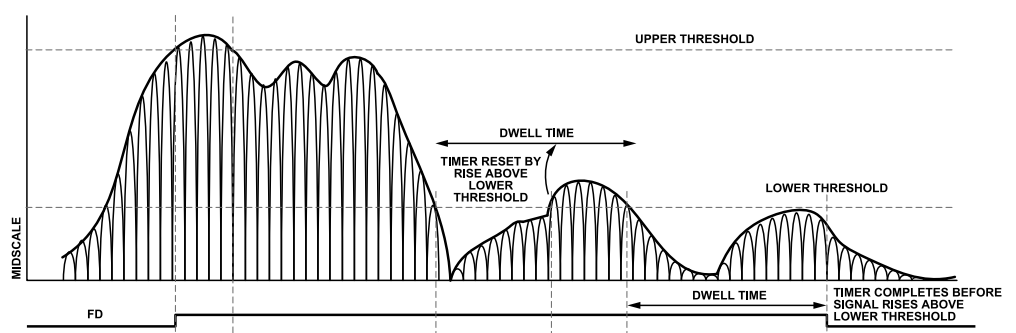


Figure 87. Threshold Settings for FD Signal

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained by reading back the internal values from the SPI port. A global, 24-bit programmable period controls the duration of the measurement. Figure 88 shows the simplified block diagram of the signal monitor block.

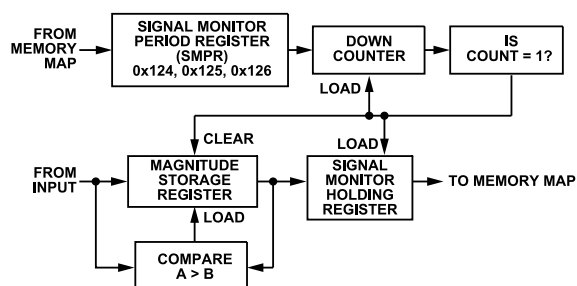


Figure 88. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is an 11-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$\text{Peak Magnitude (dBFS)} = 20\log(\text{Peak Detector Value}/2^{11}) \quad (4)$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor

period register (SMPR). The peak detector function is enabled by setting Bits 1 and 4 of Register 0x127 and Bit 0 of Register 0x131 in the signal monitor control register. The 24-bit SMPR must be programmed in Register 0x124 to Register 0x126 before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 11-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure continues.

To monitor value can be read as a Q11.9 value from Register 0x120, Register 0x121, or Register 0x122. The signal monitor runs continuously. However, this value is only updated by the user setting Bit 0 in Register 0x127. The value is stored until a subsequent update is requested by the user.

DIGITAL OUTPUTS

HIGH SPEED PARALLEL INTERFACE

The digital outputs of the AD9217 use Analog Devices, Inc., advanced physical interface (PHY) technology to incorporate a parallel data interface capable of 10 GSPS. This value matches the AD9217 maximum sample rate while also minimizing the interface latency. As with traditional parallel interfaces, the number of data outputs equals the number of converter bits. In the case of the AD9217, the number of converter bits is 12. The interface also includes a single data clock output operating at one half the ADC sample rate and a parity bit. All outputs are differential. Therefore, the total number of required balls is 28.

A functional block diagram for the output drivers is shown in [Figure 89](#).

Data Outputs

It is recommended that all AD9217 data output connections to the receiving logic device be ac-coupled using 1 nF capacitors. Each output bit stream on the AD9217 can be scrambled to maintain the dc balance on each data lane. For die to die applications, dc-coupling without scrambling is acceptable. Scrambling is enabled by setting Register 0x4B1, Bit 0 to Logic 1. The scrambler operates on 16 consecutive bits using the same algorithm used for JESD204B ($1 + x^{14} + x^{15}$). The default state of the scrambler is off (Register 0x4B1, Bit 0 = 0). During calibration, the scrambler must remain off. After calibration is complete, enable the scrambler for transmission of sample data for the purposes of dc balance and the reduction of spurious content in the data.

The output driver features controlled, 100 Ω differential impedance and supports de-emphasis/swing control via a three tap (–1, 0, and +1) FIR filter to overcome channel loss and channel impedance discontinuities.

Parity Output

A parity bit is generated for each 12-bit sample to detect any single bit errors or any errors that result from channel to channel misalignment. The parity bit is passed along simultaneously with the data sample and is determined prior to being scrambled.

Parity is defined as the number of ones in the 12-bit sample. By default, if the total number of ones is even, the parity bit = 0, if the total number of ones is odd, the parity bit = 1. The parity bit can be inverted by setting the SPI register bit, Register 0x4B0, Bit 0, to 1.

AC-couple the differential parity signal going to the logic device using 1 nF capacitors.

Data Clock Output

The data clock operates at one half the data rate. Therefore, data is transmitted on both the rising and falling edges of the data clock. The data and the parity bit operate at up to 10.25 Gbps, while the data clock output operates up to 5.125 GHz. [Figure 4](#) shows the timing relationship between the data and parity bits relative to the clock. [Table 4](#) shows the electrical specifications.

AC-couple the differential clock signal going to the logic device using 1 nF capacitors.

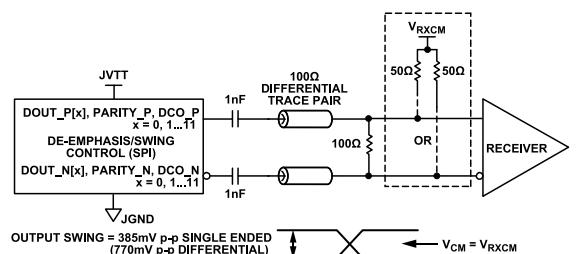


Figure 89. Transmitter Driver Block Diagram

DIGITAL OUTPUTS

PHY Output Controls

The DOUT[11:0], DCO, and PARITY outputs are all driven by the Analog Devices high speed PHYs. Therefore, each output features associated de-emphasis and output voltage swing controls. This configuration provides the end user with the flexibility to compensate for performance constraints that may be introduced by the PCB design.

De-Emphasis

De-emphasis can be enabled to help compensate for any system dependent insertion loss between the ADC output and receiver that may inhibit the ability of the receiver to properly recover data. By default, de-emphasis is disabled. Register 0x5C2 to Register 0x5D1 control the tap weight setting for the pre-tap de-emphasis of each of the 12 data channels. The pre-tap de-emphasis can be set to compensate for up to 6 dB of precursor intersymbol interference (ISI) in 3 dB increments. Register 0x5BA to Register 0x5C1 control the tap weight setting for the post-tap de-emphasis for each of the 12 data channels. The post-tap de-emphasis can be set to compensate for up to 12 dB of postcursor ISI in 3 dB increments.

Output Line Rates

The high speed parallel output interface PLL is configured to operate correctly at the sample rates associated with each AD9217 speed grade. The AD9217BBPZ-10G is configured by default to operate from 6.8 GSPS to 10.25 GSPS. If the AD9217BBPZ-10G is to be operated at less than 6.8 GBPS, the following registers must be written:

- ▶ Write Register 0x570, Bit 0 = 0 to power down the PLL.
- ▶ Write Register 0x5AA, Bit 0 = 1 to enable the PLL dividers.
- ▶ Write Register 0x57A, Bits[2:0] = 2 to set the input to divide by 4.
- ▶ Write Register 0x57A, Bits[5:4] = 3 to set the output to divide by 4.
- ▶ Write Register 0x57B, Bits[7:0] = 8 to set the multiplier for use in integer division calculation.
- ▶ Write Register 0x570, Bit 0 = 1 to power up the PLL.

Output Voltage Swing

The output swing of the differential data outputs are set relative to the JVTT supply. V_{SWING} is adjustable from $0.500 \times \text{JVTT}$ to $1.00 \times \text{JVTT}$ using Register 0x5B2 to Register 0x5B9. It is recommended to use the default setting of $0.850 \times \text{JVTT}$ for most applications.

Calibration

To properly align the 12 data bits and the parity bit of the high speed parallel interface in the receiving device, a calibration sequence is required. This sequence relies on the receiver to alter the registers in the transmitter through the SPI interface. This communication allows the system to move through the alignment calibration steps listed as follows:

1. The transmitter and receiver power up.
2. Data and clock alignment occur.
 - a. The receiver writes to the transmitter register to send the clock and data alignment pattern.
 - b. The transmitter changes the datapath mux and sends out clock and data pattern.
 - c. The receiver aligns the data to clock.
3. Channel word alignment occurs.
 - a. The receiver writes to the transmitter register to send the channel word alignment pattern.
 - b. The transmitter changes the datapath mux and sends out the channel word alignment pattern.
 - c. The receiver locates the correct work boundary for each channel.
4. Channel to channel alignment occurs.
 - a. The receiver writes to the transmitter register to send the channel alignment pattern.
 - b. The transmitter changes the datapath mux to send out the channel to channel alignment pattern.
 - c. The receiver delays each channel as needed to align all bits to the channel with the most delay.
5. Break word/ADC Data transfer occurs.
 - a. The receiver writes to the transmitter register to send the ADC data.
 - b. The transmitter changes the data pattern to send out the break pattern and then follows by sending out the ADC data.
6. The receiver monitors the parity bit and determines if recalibration is needed.

Table 10 describes the details of the calibration operation sequence. The sequence is initiated by the system software and is then automatically carried out in the FPGA by the calibration state machine. This sequence assumes all other functions of the ADC are configured, including the selection of the high speed parallel interface as the digital output interface (Register 0x480, Bit 0 = 1) and the powering on of the appropriate channel PHYs (Register 0x5B0 to Register 0x5B1).

Parity Error Monitoring

The users system FPGA (receiver) computes the parity of the incoming data samples and compares this result to the parity bit input received from the ADC (transmitter) output. If the computed receiver parity value does not match the transmitter parity value, the parity error flag is raised in the user FPGA code. The system software determines if and when recalibration of the parallel data link is needed, based on the parity error information it receives from the FPGA.

DIGITAL OUTPUTS

Table 10. Calibration Operation Sequence

Step No.	Action	Device	Details
1	Data capture start asserted	System software FPGA	System start-up procedure initiated by software The user system FPGA code initiates a start capture
2	FPGA sets DUT scrambling off and sets pattern to clock/data alignment pattern (default is 0xAAAA)	FPGA AD9217	Data and clock alignment initiated by the FPGA Register 0x4B1, Bit 0 = 0, scrambler off; Register 0x4A0, Bits[3:0] = 1, select Pattern 1 (Register 0x481 to Register 0x482)
	FPGA transceivers configured	FPGA	Writes appropriate SPI bits
	FPGA transceiver clock data recovery locks	FPGA	Reads appropriate SPI bits to verify bit alignment
3	FPGA sets DUT pattern to channel word alignment pattern (default is 0xFF00)	FPGA AD9217	Word alignment initiated by the FPGA Register 0x4A0, Bits[3:0] = 2; select Pattern 2 (Register 0x483 to Register 0x484)
	FPGA transceiver comma detect used to align to word alignment pattern	FPGA	Reads appropriate SPI bits to verify word alignment
4	FPGA sets DUT pattern to channel alignment pattern (default is 0xB496)	FPGA AD9217	Channel alignment initiated by the FPGA Register 0x4A0, Bits[3:0] = 4; select Pattern 4 (Register 0x487 to Register 0x488)
	FPGA RTL deskews channels	FPGA	Reads appropriate SPI bits to verify channel alignment
5	FPGA sets DUT pattern to ADC data	FPGA AD9217	Set mux for ADC data transmission Register 0x4A0, Bits[3:0] = 0; select ADC data
	DUT sends break word then ADC data	AD9217	Break word (0x3333) is sent automatically once then ADC data is sent; Register 0x4A0, Bits[3:0] = 0
	FPGA optionally sets DUT scrambling on after break word seen	FPGA AD9217	Sets scrambling on (recommended) Register 0x4B1, Bit 0 = 1; scrambler on
6	FPGA starts capturing ADC data	FPGA	FPGA monitors parity bit

SERIAL PORT INTERFACE (SPI)

The AD9217 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the AD9217 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see [Table 11](#)). The SCLK (serial clock) pin is used to synchronize the read and write data presented to and from the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found [Figure 2](#) and [Table 5](#).

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device. This process is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial

port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the [Serial Control Interface Standard \(Rev. 1.0\)](#).

SPI ACCESSIBLE FEATURES

[Table 12](#) provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the [Serial Control Interface Standard \(Rev. 1.0\)](#). The AD9217 device specific features are described in the [Memory Map](#) section.

HARDWARE INTERFACE

The pins described in [Table 11](#) comprise the physical interface between the user programming device and the serial port of the AD9217. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the [AN-812 Application Note, Micro-controller-Based Serial Port Interface \(SPI\) Boot Circuit](#).

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9217 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Table 11. SPI Pins

Pin Name	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

Table 12. SPI Accessible Features

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock frequency change registers SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLES

Table 13 documents the default hexadecimal value for each hexadecimal address shown. All address locations that are not included in Table 13 are not currently supported for this device and should not be written.

Open and Reserved Locations

All address and bit locations that are not included in Table 13 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned. If the entire address location is open, do not write to this address location.

Default Values

After the AD9217 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 13.

Table 13. Register Map

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x0	SPI_CONFIG_A	7	SOFT_RESET_1		Initiates a Reset Equivalent to a Hard Reset. 0 Do nothing. 1 Reset the SPI and registers (self clearing).	0x0	R/W
		6	LSB_FIRST_1		LSB/MSB Bit Shift First. 0 Most significant bit shifted first. 1 Least significant bit shifted first.	0x0	R/W
		5	ADDR_ASCENSION_1		Multibyte SPI Operations Address Increment. 0 Auto-decrement. 1 Auto-increment.	0x0	R/W
		[4:3]	Reserved		Reserved.	0x0	R
		2	ADDR_ASCENSION_0		Multibyte SPI Operations Address Increment. 0 Auto-decrement. 1 Auto-increment.	0x0	R/W
		1	LSB_FIRST_0		LSB/MSB Bit Shift First. 0 MSB shifted first. 1 LSB shifted first.	0x0	R/W
		0	SOFT_RESET_0		Initiates a Reset Equivalent to a Hard Reset. 0 Do nothing. 1 Reset the SPI and registers (self clearing).	0x0	R/W
0x2	DEVICE_CONFIG	[7:2]	Reserved		Reserved.	0x3C	R
		[1:0]	OP_MODE		Operating Mode. 00 Normal operation. 10 Standby mode. 11 Power-down mode.	0x0	R/W
0x3	CHIP_TYPE	[7:0]	CHIP_TYPE		High Speed ADCs.	0x3	R

Logic Levels

An explanation of logic level terminology follows:

- Bit is set is synonymous with bit is set to Logic 1 or writing Logic 1 for the bit.
- Clear a bit is synonymous with bit is set to Logic 0 or writing Logic 0 for the bit.
- X denotes a don't care bit.

SPI Soft Reset

After issuing a soft reset by programming Register 0x000, the AD9217 requires 300 ms to recover. When programming the AD9217 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x4	CHIP_ID_LSB	[7:0]	CHIP_ID[7:0]		Chip ID.	0xE6	R
0x5	CHIP_ID_MSB	[7:0]	CHIP_ID[15:8]		Chip ID.	0x00	R
0xA	CHIP_SCRATCH	[7:0]	CHIP_SCRATCH		Chip Scratch Pad Register.	0x0	R/W
0xC	VENDOR_ID_LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID	0x56	R
0xD	VENDOR_ID_MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID	0x4	R
0x26	GEN_CTRL	[7:4]	Reserved		Reserved.	0x0	R
		3	CLK_SWITCH		Clock Ready (Self Clearing).	0x0	R/W
		[2:0]	Reserved		Reserved.	0x0	R
0x100	FD_CTRL	[7:3]	Reserved		Reserved.	0x0	R
		2	FD_FINE_EN		Enable Fast Detect on Corrected ADC Data. 0 Fast detect disabled. 1 Fast detect enabled.	0x0	R/W
		1	FD_FORCE_VAL		Force Value for the Fast Detect. This bit field value is forced on the FD pin when FD_FORCE is high.	0x0	R/W
		0	FD_FORCE		Force the Fast Detect Output Pin. 0 Normal operation of the fast detect pin. Force a value on the fast detect pin (see Bit 1). 1	0x0	R/W
0x101	FD_UP_THRESH_LSB	[7:0]	FD_UP_THRESH[7:0]		Fast Detect Upper Threshold Unsigned Number. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input is above the upper threshold value for one $f_s/16$ clock cycle.	0x0	R/W
0x102	FD_UP_THRESH_MSB	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	FD_UP_THRESH[10:8]		Fast Detect Upper Threshold Unsigned Number. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input is above the upper threshold value for one $f_s/16$ clock cycle.	0x0	R/W
0x103	FD_LOW_THRESH_LSB	[7:0]	FD_LOW_THRESH[7:0]		Fast Detect Lower Threshold Unsigned Number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input is below the lower threshold value for DWELL_THRESH time.	0x0	R/W
0x104	FD_LOW_THRESH_MSB	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	FD_LOW_THRESH[10:8]		Fast Detect Lower Threshold Unsigned Number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input is below the lower threshold value for DWELL_THRESH time.	0x0	R/W
0x105	FD_DWELL_THRESH_LSB	[7:0]	FD_DWELL_THRESH[7:0]		Fast Detect Dwell Time Counter Target. The fast detect goes low if the analog input is below the fast detect lower threshold value for FD_DWELL_THRESH time. This is a 16-bit counter. Value must be in multiples of 16.	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x106	FD_DWELL_THRESH_MSB	[7:0]	FD_DWELL_THRESH[15:8]		Fast Detect Dwell Time Counter Target. The fast detect goes low if the analog input is below the fast detect lower threshold value for FD_DWELL_THRESH time. This is a 16-bit counter. Value must be in multiples of 16.	0x0	R/W
0x120	SMON_STATUSN	[7:0]	SMON_STATUS		20-Bit Signal Monitor Serial Data Output Bits. Signal monitor data output status bits. Bits[19:9] have the peak magnitude value obtained over the programmable SMON_PERIOD.	0x0	R
0x123	SMON_STATUS_FCNT	[7:0]	SMON_STATUS_FCNT		Signal Monitor Frame Counter. Increments whenever period counter expires and the counter value can be read back from this bit field whenever the SMON_STATUS_UPDATE signal is pulled high.	0x0	R
0x124	SMON_PERIOD_0	[7:0]	SMON_PERIOD[7:0]		24-Bit Value That Sets the Number of Clock Cycles over Which the Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. Must be in multiples of 16.	0x0	R/W
0x125	SMON_PERIOD_1	[7:0]	SMON_PERIOD[15:8]		24-Bit Value That Sets the Number of Clock Cycles over Which the Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. Must be in multiples of 16.	0x0	R/W
0x126	SMON_PERIOD_2	[7:0]	SMON_PERIOD[23:16]		24-Bit Value That Sets the Number of Clock Cycles over Which the Signal Monitor Performs Operation. 24-bit period value over which the signal monitor performs the peak detection. Must be in multiples of 16.	0x0	R/W
0x127	SMON_STATUS_CTRL	[7:5]	Reserved		Reserved.	0x0	R
		4	SMON_PEAK_EN	0 1	Signal monitor peak detector enable. Disabled. Enabled.	0x0	R/W
		[3:1]	SMON_STATUS_RDSEL	1	Signal Monitor Status Readback Selection. Set to 0x1 for peak detector. Peak detector data.	0x0	R/W
		0	SMON_STATUS_UPDATE		A high transition on this signal causes the status value to change in the register map. When this bit field is pulled high, SMON_STATUS is updated with the next value of the peak magnitude.	0x0	R/W
0x131	SMON_CLK_EN	[7:1]	Reserved		Reserved.	0x0	R
		0	SMON_CLK_EN	0 1	SMON Output Clock Enable. Disabled. Enabled.	0x0	R/W
0x332	CLK_CHG_REQ	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	CLKCHGREQ		Request Sample Clock Frequency Change.	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x481	HSP_PAT_1_MSB	[7:0]	HSP_PAT_1_MSB		Bits[15:8] of Pattern 1.	0xAA	R/W
0x482	HSP_PAT_1_LSB	[7:0]	HSP_PAT_1_LSB		Bits[7:0] of Pattern 1.	0xAA	R/W
0x483	HSP_PAT_2_MSB	[7:0]	HSP_PAT_2_MSB		Bits[15:8] of Pattern 2.	0xFF	R/W
0x484	HSP_PAT_2_LSB	[7:0]	HSP_PAT_2_LSB		Bits[7:0] of Pattern 2.	0x0	R/W
0x485	HSP_PAT_3_MSB	[7:0]	HSP_PAT_3_MSB		Bits[15:8] of Pattern 3.	0xAA	R/W
0x486	HSP_PAT_3_LSB	[7:0]	HSP_PAT_3_LSB		Bits[7:0] of Pattern 3.	0xAA	R/W
0x487	HSP_PAT_4_MSB	[7:0]	HSP_PAT_4_MSB		Bits[15:8] of Pattern 4.	0xB4	R/W
0x488	HSP_PAT_4_LSB	[7:0]	HSP_PAT_4_LSB		Bits[7:0] of Pattern 4.	0x96	R/W
0x489	HSP_PAT_5_MSB	[7:0]	HSP_PAT_5_MSB		Bits[15:8] of Pattern 5.	0x0	R/W
0x48A	HSP_PAT_5_LSB	[7:0]	HSP_PAT_5_LSB		Bits[7:0] of Pattern 5.	0x0	R/W
0x48B	HSP_PAT_6_MSB	[7:0]	HSP_PAT_6_MSB		Bits[15:8] of Pattern 6.	0xFF	R/W
0x48C	HSP_PAT_6_LSB	[7:0]	HSP_PAT_6_LSB		Bits[7:0] of Pattern 6.	0xFF	R/W
0x48D	HSP_PAT_BK_MSB	[7:0]	HSP_PAT_BK_MSB		Bits[15:8] of Break Pattern.	0x33	R/W
0x48E	HSP_PAT_BK_LSB	[7:0]	HSP_PAT_BK_LSB		Bits[7:0] of Break Pattern.	0x33	R/W
0x48F	HSP_32B_ADD_PAT_1_MSB	[7:0]	HSP_32B_ADD_PAT_1_MSB		Bits [31:24] of Pattern 1.	0xAA	R/W
0x490	HSP_32B_ADD_PAT_1_LSB	[7:0]	HSP_32B_ADD_PAT_1_LSB		Bits[23:16] of Pattern 1.	0xAA	R/W
0x491	HSP_32B_ADD_PAT_2_MSB	[7:0]	HSP_32B_ADD_PAT_2_MSB		Bits [31:24] of Pattern 2.	0xAA	R/W
0x492	HSP_32B_ADD_PAT_2_LSB	[7:0]	HSP_32B_ADD_PAT_2_LSB		Bits[23:16] of Pattern 2.	0xAA	R/W
0x493	HSP_32B_ADD_PAT_3_MSB	[7:0]	HSP_32B_ADD_PAT_3_MSB		Bits[31:24] of Pattern 3.	0xAA	R/W
0x494	HSP_32B_ADD_PAT_3_LSB	[7:0]	HSP_32B_ADD_PAT_3_LSB		Bits[23:16] of Pattern 3.	0xAA	R/W
0x495	HSP_32B_ADD_PAT_4_MSB	[7:0]	HSP_32B_ADD_PAT_4_MSB		Bits[31:24] of Pattern 4.	0xAA	R/W
0x496	HSP_32B_ADD_PAT_4_LSB	[7:0]	HSP_32B_ADD_PAT_4_LSB		Bits[23:16] of Pattern 4.	0xAA	R/W
0x497	HSP_32B_ADD_PAT_5_MSB	[7:0]	HSP_32B_ADD_PAT_5_MSB		Bits[31:24] of Pattern 5.	0x0	R/W
0x498	HSP_32B_ADD_PAT_5_LSB	[7:0]	HSP_32B_ADD_PAT_5_LSB		Bits[23:16] of Pattern 5.	0x0	R/W
0x499	HSP_32B_ADD_PAT_6_MSB	[7:0]	HSP_32B_ADD_PAT_6_MSB		Bits[31:24] of Pattern 6.	0xFF	R/W
0x49A	HSP_32B_ADD_PAT_6_LSB	[7:0]	HSP_32B_ADD_PAT_6_LSB		Bits[23:16] of Pattern 6.	0xFF	R/W
0x49B	HSP_32B_ADD_PAT_BK_MSB	[7:0]	HSP_32B_ADD_PAT_BK_MSB		Bits[31:24] of Break Pattern.	0x33	R/W
0x49C	HSP_32B_ADD_PAT_BK_LSB	[7:0]	HSP_32B_ADD_PAT_BK_LSB		Bits[23:16] of Break Pattern.	0x33	R/W
0x4A0	HSP_PAT_SEL	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	HSP_PAT_SEL		HSP Pattern Select. Value 7 is a changing pattern set. Pattern 3 is repeated X73 times and Pattern 4 is repeated X74 times. X73 = HSP_PAT_REPEAT_SEL[7:4] and X74 = HSP_PAT_REPEAT_SEL[3:0]. Value 8 is a changing pattern set. Pattern 5 is repeated X85 times and Pattern 6 is repeated X85 times. X85 = HSP_PAT_REPEAT_SEL[7:4]. X86 = HSP_PAT_REPEAT_SEL[3:0]. 9 to 15 are not used.	0x0	R/W
				0x6	HSP Pattern 6.		
				0x5	HSP Pattern 5.		
				0x8	HSP Pattern 5 and HSP Pattern 6.		
				0x4	HSP Pattern 4.		
				0x3	HSP Pattern 3.		
				0x7	HSP Pattern 3 and HSP Pattern 4.		

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x4A1	HSP_PAT_REPEAT_SEL7	[7:4]	HSP_PAT3_REPEAT_CNT	0x2	HSP Pattern 2.	0x0	R/W
				0x1	HSP Pattern 1.		
				0x0	ADC data.		
				0x0	0.		
				0x1	1.		
				0x2	2.		
				0x3	4.		
				0x4	8.		
				0x5	16.		
				0x6	32.		
				0x7	64.		
		[3:0]	HSP_PAT4_REPEAT_CNT		HSP Pattern 4 Repeat Count	0x0	R/W
				0x0	0.		
				0x1	1.		
				0x2	2.		
				0x3	4.		
				0x4	8.		
				0x5	16.		
				0x6	32.		
				0x7	64.		
0x4A2	HSP_PAT_REPEAT_SEL8	[7:4]	HSP_PAT5_REPEAT_CNT		HSP Pattern 5 Repeat Count.	0x0	R/W
				0	0.		
				1	1.		
				10	2.		
				11	4.		
				100	8.		
				101	16.		
				110	32.		
				111	64.		
		[3:0]	HSP_PAT6_REPEAT_CNT		HSP Pattern 6 Repeat Count.	0x0	R/W
				0	0.		
				1	1.		
				10	2.		
				11	4.		
				100	8.		
				101	16.		
				110	32.		
				111	64.		
0x4A3	HSP_CLK_PAT_SEL	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	HSP_CLK_PAT_SEL		HSP Clock Pattern Select.	0x0	R/W
				000	Half rate clock pattern (0xAAAA) is sent on clock lane.		
				001	Quarter rate clock pattern (0x3333) is sent on clock lane.		
				010	A lone one clock pattern (0x0001) is sent on clock lane.		
				011	Static clock pattern (0x0000) is sent on clock lane.		

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
				100	Static clock pattern (0xFFFF) is sent on clock lane.		
				101	Programmable clock pattern is sent on clock lane.		
				110	Programmable clock pattern is sent on clock lane.		
				111	Programmable clock pattern is sent on clock lane.		
0x4A4	HSP_CLK_PAT_EXT_MSB	[7:0]	HSP_CLK_PAT_EXT_MSB		Bits[15:8] of Programmable Clock Pattern.	0x0	R/W
0x4A5	HSP_CLK_PAT_EXT_LSB	[7:0]	HSP_CLK_PAT_EXT_LSB		Bits[7:0] of Programmable Clock Pattern.	0x0	R/W
0x4A6	HSP_CLK_32B_ADD_PAT_EXT_MSB	[7:0]	HSP_CLK_32B_ADD_PAT_EXT_MSB		Bits[31:24] of Programmable Clock Pattern.	0x0	R/W
0x4A7	HSP_CLK_32B_ADD_PAT_EXT_LSB	[7:0]	HSP_CLK_32B_ADD_PAT_EXT_LSB		Bits[23:16] of Programmable 32-Bit Clock Pattern.	0x0	R/W
0x4B0	HSP_PARITY_REG	[7:1]	Reserved		Reserved.	0x0	R
		0	HSP_PARITY_TYPE		HSP Parity Type. Parity is determined for each 12-bit ADC sample and passed along with the data. Default parity for this application is defined as the number of ones in a 12-bit word. If the total number of ones is even, the parity bit = 0. If the total number of ones is odd, the parity bit = 1, 0 Even parity (default). 1 Odd parity (invert parity).	0x0	R/W
0x4B1	HSP_SCRAMBLER_REG	[7:1]	Reserved		Reserved.	0x0	R
		0	HSP_SCRAMBLER_EN		HSP Scrambler Enable. 0 Scrambler is disabled. 1 Scrambler is enabled.	0x0	R/W
0x4B2	HSP_CTRL_REG	[7:3]	Reserved		Reserved.	0x0	R
		2	HSP_2PIN_GPIO_PAT_SEL_MODE		HSP 2 Pin GPIO Pattern Select. This bit has an effect only when HSP_GPIO_PAT_SEL_MODE = 1. 0 GPIO[3:0] pins used for pattern selection. 1 GPIO[1:0] pins used for pattern selection.	0x0	R/W
		1	HSP_GPIO_PAT_SEL_MODE		HSP GPIO Pattern Select. Pattern selection based on the contents of Register 0x4A0, HSP_PAT_SEL[3:0]. Pattern selection based on GPIO[3:0] pins. 0 1	0x0	R/W
		0	SER_HSP_MODE		HSP Mode. 0 Chip is in JTX mode. 1 Chip is in HSP mode.	0x1	R/W
0x4B3	HSP_SER_PARITY_RESET_EN1	[7:0]	HSP_SER_PARITY_RESET_EN[7:0]		HSP Parity Reset Enable.	0x0	R/W
0x4B4	HSP_SER_PARITY_RESET_EN2	[7:0]	HSP_SER_PARITY_RESET_EN[15:8]		HSP Parity Reset Enable.	0x0	R/W
0x4B5	HSP_PARITY_RST_N1	[7:0]	HSP_SER_PARITY_RST_N[7:0]		HSP Parity Clear Bit. Each bit is a channel HSP_SER_PARITY_RST_N connected to serializer RSTB_PARITY_HSP pins	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x4B6	HSP_PARITY_RST_N2	[7:0]	HSP_SER_PARITY_RST_N[15:8]		HSP Parity Clear Bit. Each bit is a channel HSP_SER_PARITY_RST_N connected to serializer RSTB_PARITY_HSP pins	0x0	R/W
0x4B7	HSP_SER_PARITY_ERR1	[7:0]	HSP_SER_PARITY_ERR[7:0]		Parity Error. Parity error readback (status) register from SERDES.	0x0	R
0x4B8	HSP_SER_PARITY_ERR2	[7:0]	HSP_SER_PARITY_ERR[15:8]		Parity Error. Parity error read back (status) register from SERDES.	0x0	R
0x4B9	PWR_DN	[7:0]	HSP_PD_SER[7:0]	1	Power Down PHY Channel in HSP Mode. Channel off.	0x0	R/W
0x4BA	PWR_DN2	[7:0]	HSP_PD_SER[15:8]	1	Power Down PHY Channel in HSP Mode. Channel off.	0x0	R/W
0x4BB	HSP_LANE_PDWN	[7:0]	HSP_FORCE_LANE_PD[7:0]		Physical Lane Force Power-Down.	0x0	R/W
0x4BC	HSP_LANE_PDWN2	[7:0]	HSP_FORCE_LANE_PD[15:8]		Physical Lane Force Power-Down.	0x0	R/W
0x4BD	HSP_LINK_PD	[7:1]	Reserved		Reserved.	0x0	R
		0	HSP_LINK_PD	0 1	HSP Transmit Link Power-Down (Active High). Normal operation. Power-down.	0x0	R/W
0x4BE	PLL_CTRL	7	HSP_PLL_BYPASS_LOCK	0 1	Bypass PLL Lock Input. PLL lock signal used to generate the HSP_PLL_LOCKED status signal. PLL lock signal ignored. HSP_PLL_LOCKED status is '1'.	0x0	R/W
		[6:0]	Reserved		Reserved.	0x0	R
0x4BF	PLL_STATUS	7	HSP_PLL_LOCKED	0 1	PLL Locked Status Bit. How PLL locked status bit is generated depends on the HSP_PLL_BYPASS_LOCK bit setting. PLL lock signal from serializer is used to generate the HSP_PLL_LOCKED status signal PLL lock signal from serializer is ignored.	0x0	R
		[6:0]	Reserved		Reserved.	0x0	R
0x4C0	HSP_RSTB	[7:0]	HSP_RSTB_SER[7:0]	0 1	RESETB Signal for PHY Digital Logic. Channel 0. Channel 1.	0x0	R/W
				0 1	Channel 0. Channel 1.		
0x4C1	HSP_RSTB2	[7:0]	HSP_RSTB_SER[15:8]	0 1	RESETB Signal for PHY Digital Logic. Channel 0. Channel 1.	0x0	R/W
				0 1	Channel 0. Channel 1.		
0x4C2	HSP_32BIT_CTRL_REG	[7:4]	Reserved		Reserved.	0x0	R
		3	SER_32BIT_CLK_PAT_EN		HSP 32-Bit Clock Pattern Enable. This bit has an effect only when SER_32BIT_MODE = 1. Based on HSP_CLK_PAT_SEL,000: half rate clock pattern (0xAAAAAAAA) is sent on clock lane. 001: quarter rate clock pattern (0x33333333) is sent on clock lane. 010: a lone 32-bit one clock pattern (0x00000001) is sent on clock lane.	0x1	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
					011: static clock pattern (0x0000) is sent on clock lane. 100: static clock pattern (0xFFFFFFFF) is sent on clock lane. 101,110,111: programmable 32-bit clock pattern is sent on clock lane. 0 Same as 16-bit clock pattern selection. 1 Based on HSP_CLK_PAT_SEL (default).		
		2	SER_32BIT_BK_PAT_EN		HSP 32-Bit Break Pattern Enable. This bit has an effect only when SER_32BIT_MODE = 1. Single 16-bit break pattern indicates start of data. Single 32-bit break pattern indicates start of data (default). 0 1	0x1	R/W
		1	SER_32BIT_RPT_PAT_EN		HSP 32-Bit Repeat Pattern Enable. Effective only when SER_32BIT_MODE = 1. For Pattern Select 7 mode and Pattern Select 8 mode, the patterns used are 16-bit. Same as with 16-bit pattern mode. For Pattern Select 7 mode and Pattern Select 8 mode, the patterns used are 32-bit. Each 32 bit pattern is repeated (default). 0 1	0x1	R/W
		0	SER_32BIT_MODE		HSP 32-Bit Mode. 0 HSP in 16-bit pattern mode (default). 1 HSP in 32-bit pattern mode.	0x0	R/W
0x4C3	HSP_FORCE_LINK_RESET	[7:1]	Reserved		Reserved.	0x0	R
		0	HSP_FORCE_LINK_RESET		Force Link Reset from Register Map. This bit controls HSP_SER_SRST_N only, which is useful if the PD_SER delay is higher than the HSP_SER_SRST_N path delay. Provides control to deassert HSP_SER_SRST_N alone at the end of reset/power-down deassertion.	0x0	R/W
0x570	PLL_ENABLE_CTRL	[7:5]	Reserved		Reserved.	0x0	R
		4	LOLSTICKYCLEAR_FORCE_LCPLL_RC		Clears Out Loss of Lock Bit.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	LDSYNTH_FORCE_LCPLL_AD C		A Short 1 Pulse Starts VCO Calibration. The pulse width must be at least 1 reference clock period. Allows for user to perform a calibration at will.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	PWRUP_LCPLL		Output Interface PLL Power. Power off (0) before changing output interface PLL divide values. The power back on (1). 0 Output interface PLL powered off. 1 Output interface PLL powered on.	0x0	R/W
0x57A	PLL_REF_CLK_DIV1_REG	7	REFCK_DIV40BDIV120_LCPLL		Reference Clock Output. 1/40 or 1/120	0x0	R/W
		6	Reserved		Reserved.	0x0	R
		[5:4]	DIVM_LCPLL_RC		Selects Output Division Rate.	0x2	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
				0	Power down output divider.		
				1	No divider.		
				2	Divide by 2 (for 6.8 GSPS to 10.25 GSPS).		
				3	Divide by 4 (for 3.4 GSPS to <6.8 GSPS).		
		3	Reserved		Reserved.		
		[2:0]	REFDIV_LCPLL_RC		Sets Division Rate on Input.	0x2	R/W
				0	Divide by 1.		
				1	Divide by 2.		
				2	Divide by 4.		
				4	Divide by 8.		
		≥5	Divide by 16.				
0x57B	PLL_DIV2	[7:0]	B_LCPLL_RC		Sets Integer Division Rate as N = 8 × B_LCPLL_RC.	0x5	R/W
				5	For 6.8 GSPS to 10.25 GSPS.		
				8	For 3.4 GSPS to <6.8 GSPS.		
0x5AA	PLL_DIV_FORCE	[7:2]	Reserved		Reserved.	0x0	R
		1	FORCE_PREDIV3_LCPLL_RC		Force the Divide by 3 Option for LCPLL. Qualified with FORCEDIV.	0x0	R/W
		0	FORCEDIV_LCPLL_RC		Forces All the Pre, Post, and Feedback Dividers for the Output Interface PLL. Clear to 0 for 6.8 GSPS to 10.25 GSPS.	0x0	R/W
0x5B0	PWR_DN	[7:0]	PD_SER[7:0]		PHY Channel Power-Down. Active high.	0x00	R/W
				0	Channel 0.		
				1	Channel 1.		
				...	...		
0x5B1	PWR_DN2	[7:0]	PD_SER[15:8]		PHY Channel Power-Down. Active high.	0xFF	R/W
				0	Channel 0.		
				1	Channel 1.		
				...	...		
0x5B2	JTX_SWING1	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH1_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
3	RESERVED		Reserved.	0x0	R		
		[2:0]	DRVSWING_CH0_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
0x5B3	JTX_SWING2	7	Reserved		Reserved.		
		[6:4]	DRVSWING_CH3_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH2_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
0x5B4	JTX_SWING3			3	0.500 × JVTT.		
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH5_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH4_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
0x5B5	JTX_SWING4			1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH7_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
		3	Reserved		Reserved.	0x0	R
0x5B6	JTX_SWING5	[2:0]	DRVSWING_CH6_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH9_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
0x5B7	JTX_SWING6			3	0.500 × JVTT.		
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH11_SER_RC		Swing Level for Output Drivers.	0x1	R/W
				0	1.0 × JVTT.		
				1	0.850 × JVTT.		
				2	0.750 × JVTT.		
				3	0.500 × JVTT.		

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH10_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH13_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
0x5B8	JTX_SWING7	[2:0]	DRVSWING_CH12_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH15_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH14_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
0x5B9	JTX_SWING8	7	Reserved		Reserved.	0x0	R
		[6:4]	DRVSWING_CH15_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DRVSWING_CH14_SER_RC	0 1 2 3	Swing Level for Output Drivers. 1.0 × JVTT. 0.850 × JVTT. 0.750 × JVTT. 0.500 × JVTT.	0x1	R/W
		7	Reserved		Reserved.	0x0	R
0x5BA	DOUT0/DOUT1. de-emphasis select	[6:4]	DOUT1	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT0	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
		7	Reserved		Reserved.	0x0	R
0x5BB	DOUT2/DOUT3. de-emphasis select	7	Reserved		Reserved.	0x0	R

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
		[6:4]	DOUT3	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT2	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
0x5BC	DOUT4/DOUT5. de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	DOUT5	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT4	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
0x5BD	DOUT6/DOUT7. de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	DOUT7	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT6	0 1 2 3 4 5 to 7	Set Post Tap Level. 0 dB. 3 dB. 6 dB. 9 dB. 12 dB. Not applicable.	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x5BE	DOUT8/DOUT9. de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	DOUT9	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB. 4 12 dB. 5 to 7 Not applicable.	Set Post Tap Level.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT8	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB. 4 12 dB. 5 to 7 Not applicable.	Set Post Tap Level.	0x0	R/W
0x5BF	DOUT10/DOUT11. de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	DOUT11	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB. 4 12 dB. 5 to 7 Not applicable.	Set Post Tap Level.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT10	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB. 4 12 dB. 5 to 7 Not applicable.	Set Post Tap Level.	0x0	R/W
0x5C0	DOUT12/DOUT13. de-emphasis select	7	Reserved		Reserved.	0x0	R
		[6:4]	DOUT13	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB. 4 12 dB. 5 to 7 Not applicable.	Set Post Tap Level.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	DOUT12	0 0 dB. 1 3 dB. 2 6 dB. 3 9 dB.	Set Post Tap Level.	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x5C1	DOUT14/DOUT15. de-emphasis select	7	Reserved	4	12 dB.	0x0	R
				5 to 7	Not applicable.		
		[6:4]	DOUT15		Set Post Tap Level.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
				2	6 dB.		
0x5C2	PRE_TAP_LEVEL_CH0	7	Reserved	3	9 dB.	0x0	R
				4	12 dB.		
		[2:0]	DOUT14	5 to 7	Not applicable.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
0x5C3	PRE_TAP_LEVEL_CH01	7	Reserved	2	6 dB.	0x0	R/W
				3	9 dB.		
		[7:0]	DRVPREEM_CH0_SER_RC	4	12 dB.	0x0	R/W
				5 to 7	Not applicable.		
				0	0 dB.		
0x5C4	PRE_TAP_LEVEL_CH02	7	Reserved	1	3 dB.	0x0	R/W
				2	6 dB.		
		[7:0]	DRVPREEM_CH1_SER_RC	3	Not applicable.	0x0	R/W
				0	0 dB.		
				1	3 dB.		
0x5C5	PRE_TAP_LEVEL_CH03	7	Reserved	2	6 dB.	0x0	R/W
				3	Not applicable.		
		[7:0]	DRVPREEM_CH2_SER_RC	0	0 dB.	0x0	R/W
				1	3 dB.		
				2	6 dB.		
0x5C6	PRE_TAP_LEVEL_CH04	7	Reserved	3	Not applicable.	0x0	R/W
				0	0 dB.		
		[7:0]	DRVPREEM_CH3_SER_RC	1	3 dB.	0x0	R/W
				2	6 dB.		
				3	Not applicable.		
0x5C7	PRE_TAP_LEVEL_CH05	7	Reserved	0	0 dB.	0x0	R/W
				1	3 dB.		
		[7:0]	DRVPREEM_CH4_SER_RC	2	6 dB.	0x0	R/W
				3	Not applicable.		
				0	0 dB.		
0x5C8	PRE_TAP_LEVEL_CH06	7	Reserved	1	3 dB.	0x0	R/W
				2	6 dB.		
		[7:0]	DRVPREEM_CH5_SER_RC	3	Not applicable.	0x0	R/W
				0	0 dB.		
				1	3 dB.		

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x5C8	PRE_TAP_LEVEL_CH06	[7:0]	DRVPREEM_CH6_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5C9	PRE_TAP_LEVEL_CH07	[7:0]	DRVPREEM_CH7_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CA	PRE_TAP_LEVEL_CH08	[7:0]	DRVPREEM_CH8_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CB	PRE_TAP_LEVEL_CH09	[7:0]	DRVPREEM_CH9_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CC	PRE_TAP_LEVEL_CH010	[7:0]	DRVPREEM_CH10_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CD	PRE_TAP_LEVEL_CH011	[7:0]	DRVPREEM_CH11_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CE	PRE_TAP_LEVEL_CH012	[7:0]	DRVPREEM_CH12_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5CF	PRE_TAP_LEVEL_CH013	[7:0]	DRVPREEM_CH13_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5D0	PRE_TAP_LEVEL_CH014	[7:0]	DRVPREEM_CH14_SER_RC	0 0 dB. 1 3 dB. 2 6 dB. 3 Not applicable.	Sets Pre Tap Level.	0x0	R/W
0x5D1	PRE_TAP_LEVEL_CH015	[7:0]	DRVPREEM_CH15_SER_RC	0 0 dB. 1 3 dB. 2 6 dB.	Sets Pre Tap Level.	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
				3	Not applicable.		
0x5D2	RSTB	[7:0]	RSTB_SER[7:0]		RESETB Signal for Digital Logic. Bit 0 = Channel 0, Bit 1 = Channel 1.	0x0	R/W
				0	Reset.		
				1	Normal.		
0x5D3	RSTB2	[7:0]	RSTB_SER[15:8]		RESETB Signal for Digital Logic. Bit 0 = Channel 0, Bit 1 = Channel 1.	0x0	R/W
				0	Reset.		
				1	Normal.		
0x1507	RESET_CTRL	[7:5]	Reserved		Reserved.	0x2	R
		4	RESET_JTX		Reset JTX Block.	0x0	R/W
		3	Reserved		Reserved.	0x0	R/W
		2	RESET_DPATH		Reset Datapath. Apply to main digital.	0x0	R/W
		1	RESET_DIG_ANA		Reset Digital Blocks in the Analog Section. Reset all registers in analog section	0x0	R/W
		0	RESET_ANA		Reset Analog Section. Reset for the analog section.	0x0	R/W
0x150C	SPI_EN_DCS	[7:1]	Reserved		Reserved.	0x0	R
		0	SPI_EN_DCS		Duty Cycle Stabilizer.	0x0	R/W
				0	Disable.		
				1	Enable.		
0x150D	SPI_EN_FDLY	[7:2]	Reserved		Reserved.	0x0	R
		1	SPI_EN_SFDLY		Super Fine Delay Cell Enable Bit.	0x0	R/W
				0	Disabled.		
				1	Enabled (along with 1/2 fine delay cell).		
		0	SPI_EN_FDLY		Fine Delay Cell Enable Bit. Two halves fine delay cells in series. Each has 24 steps adjustments.	0x0	R/W
				0	Disabled.		
				1	Enabled (two halves fine delay cells).		
0x150E	SPI_TRM_FINE_DLY	[7:0]	SPI_TRM_FINE_DLY		Clock Fine Adjustment. Unsigned control to adjust sampling clock skew in 1.1 pS/step with 48 total steps. These bits are used only when Bit 1 or Bit 0 in Register 0x150D is set to 1. Minimum delay = 0, maximum delay = 48.	0x0	R/W
0x150F	SPI_TRM_SUPER_	[7:0]	SPI_TRM_SUPER_		Clock Super Fine Delay Adjustment. Unsigned control to adjust sampling clock skew in 16fS/step with 255 total steps. These bits are only used when Register h'150D, Bit[1] = 1, Register 'h1510, Bit[0] = 0. Minimum = 0, Maximum = 255.	0x0	R/W
	FINE_DLY		FINE_DLY				
0x1510	SPI_SFDC_BYPASS	[7:1]	Reserved		Reserved.	0x0	R
		0	SPI_SFDC_BYPASS		Super Fine Delay Cell Bypassed. This bit is working in conjunction with SPI_EN_SFDLY (super fine delay cell enable) bit. SPI_EN_SFDLY = 0, SPI_SFDC_BYPASS = 0 or 1 (don't care). SPI_EN_	0x0	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
					SFDLY = 1, SPI_SFDC_BYPASS = 1 (super fine delay cell bypassed).		
0x1511	BKEND_TOP_GAIN_ADJ	[7:1]	Reserved		Reserved.	0x0	R
		0	GAIN_2X		Setting this bit to 1 doubles the data at the output.	0x0	R/W
0x1512	SUPPLY_MON1 (register readback)	[7:6]	Reserved		Reserved.	0x0	R
		5	SUPMON_VTTPHY_SER_0P9		1 V Supply Monitor for Output Drivers.	0x0	R
		4	SUPMON_VDD-SYNTH_LCPLL_0P9		1 V Supply Monitor for Output Interface Synthesizer.	0x0	R
		3	SUPMON_VDDD_LCPLL_0P9		1 V Digital Supply Monitor for Output Interface PLL.	0x0	R
		2	SUPMON_VDDA_REFADC_1P0		1 V Analog Supply Monitor for reference ADC.	0x0	R
		1	SUPMON_VDDA_CLK_1P0		1 V Analog Supply Monitor for Clock.	0x0	R
		0	SUPMON_VDDA_1P0		1 V Analog Supply Monitor.	0x0	R
0x1513	SUPPLY_MON2 (register readback)	[7:5]	Reserved		Reserved.	0x0	R
		4	SUPMON_VDDA_TMU_1P8		2 V Analog Supply Monitor for TMU.	0x0	R
		3	SUPMON_VDDLDO_LCPLL_1P8		2 V Supply Monitor for Output Interface LDO.	0x0	R
		2	SUPMON_VDDD_SPI_1P8		2 V Digital Supply Monitor for SPI Pads.	0x0	R
		1	SUPMON_VDDA_REF_2P0		2 V Analog Supply Monitor for Reference.	0x0	R
		0	SUPMON_VDDA_BUF_2P0		2 V Analog Supply Monitor for Buffer.	0x0	R
0x1514	SUPPLY_MON3 (register readback)	[7:2]	Reserved		Reserved.	0x0	R
		1	SUPMON_VEEA_NEG1P0		1 V Analog Supply Monitor.	0x0	R
		0	SUPMON_VEEA_BUF_NEG1P0		1 V Analog Supply Monitor for Buffer.	0x0	R
0x1515	PDOWN_CTRL	[7:3]	PDB_REF_NOHCLK		Power-Down for Reference.	0x1F	R/W
		2	SPI_PDB_CLKBUF		Power-Down for CLK Buffer.	0x1	R/W
		1	STDBY_CHIP		Standby Chip.	0x0	R/W
		0	PD_CHIP		Power-Down Chip.	0x0	R/W
0x151A	EN_VCM_MODE	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	EN_VCM_MODE		VCM Enable Mode Control. Internal and external VCM control buffers disabled. Startup: internal VCM control buffer enabled. 01 External VCM control buffer enabled. 10 Internal and external VCM control buffers enabled. Auxiliary mode. 11	0x1	R/W
0x151B	SPI_NVG1	[7:3]	Reserved		Reserved.	0x0	R
		[2:1]	SPI_EN_SUM_NVG_1P0		There are several negative loops, and these bits control the loops enabled, which improves the efficiency at nominal mode. When the input buffer is at high performance mode, it is 11, and at nominal mode, it is 10.	0x2	R/W
		0	SPI_EN_NVG_1P0		-1 V Generator Enable Bit.	0x1	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
				0	Power-down.		
				1	Enable.		
0x151D	CLOCK_DETECT_CTRL	[7:1]	Reserved		Reserved.	0x0	R
		0	CLOCK_DETECT		Status of Clock Detect Locked. This bit indicates the instantaneous value of the clock detect circuit.	0x0	R
				0	Out of lock.		
				1	In lock.		
0x1523	GPIO_PDEB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	GPIO_PDEB		GPIO Pull-Down, Active Low.	0x1F	R/W
0x1600	USER_CTRL_TRANSFER	[7:1]	Reserved		Reserved.	0x0	R
		0	USER_CTRL_TRANSFER		If set to 1, apply the latest settings for Register 0x1601 through Register 0x1617.	0x0	R/W
					Self clearing.		
0x1601	CAL_CONTROL	[7:1]	Reserved		Reserved.	0x0	R
		0	CAL_FREEZE		Freeze Bit to Halt Background Calibrations.	0x0	R/W
0x1602	CLOCK_RATE	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	CLOCK_RATE		User to Specify Operating Clock Rate for Calibration Adaptation. Support for up to 4 clock rates. User can choose what those 4 clock rate values are.	0x0	R/W
				0	Clock Rate 0.		
				1	Clock Rate 1.		
				10	Clock Rate 2.		
				11	Clock Rate 3.		
0x1606	GPIO_CONTROL	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	GPIO_PROFILE		Define which GPIO profile to use	0x0	R/W
				0	Disabled. GPIO profiles disabled.		
				1	GPIO pins are used as control for HSP calibration		
0x1609	MAX_TEMPERATURE_LSB	[7:0]	MAX_TEMPERATURE[7:0]		Maximum Temperature of All Temperature Sensors. Q9.7 format.	0x0	R
0x160A	MAX_TEMPERATURE_MSB	[7:0]	MAX_TEMPERATURE[15:8]		Maximum Temperature of All Temperature Sensors. Q9.7 format.	0x0	R
0x160D	MIN_TEMPERATURE_LSB	[7:0]	MIN_TEMPERATURE[7:0]		Minimum Temperature of All Temperature Sensors. Q9.7 format.	0x0	R
0x160E	MIN_TEMPERATURE_MSB	[7:0]	MIN_TEMPERATURE[15:8]		Minimum Temperature of All Temperature Sensors. Q9.7 format.	0x0	R
0x160F	FD_OV_CONTROL	[7:2]	Reserved		Reserved.	0x0	R
		1	OV_EN		Overvoltage FD Pin Enable.	0x0	R/W
		0	FD_EN		Fast Detect FD Pin Enable.	0x0	R/W
0x1612	CHANNEL_GAIN_CONTROL_LSB	[7:0]	CHANNEL_GAIN_CONTROL[7:0]		Gain Adjustment Control for the Entire Channel. Value is represented as Q2.14 format.	0x0	R/W
0x1613	CHANNEL_GAIN_CONTROL_MSB	[7:0]	CHANNEL_GAIN_CONTROL[15:8]		Gain Adjustment Control for the Entire Channel. Value is represented as Q2.14 format.	0x40	R/W

MEMORY MAP

Table 13. Register Map (Continued)

Address	Name	Bits	Bit Name	Settings	Description	Default	Access
0x1614	ENCODE_CHANGE (only for changing sampling rate on the fly)	[7:3]	Reserved		Reserved.	0x0	R
		2	ACK_ENCODE_CHANGE_DONE		Acknowledge Encode Change Done.	0x0	R
		1	ENCODE_CHANGE_DONE		Bit for User to Indicate Encode Clock Rate is Changed	0x0	R/W
		0	READY_FOR_ENCODE_CHANGE		Bit to Indicate User Can Change Encode Clock Rate.	0x0	R
0x1617	DC_COUPLED_MODE_EN	[7:1]	Reserved		Reserved.	0x0	R
		0	DC_COUPLED_MODE_EN		Enable to Retain DC Content of Input Signal. AC-coupled mode. Actively null dc content of input signal. DC-coupled mode. Retain dc content of input signal.	0x0	R/W

APPLICATIONS INFORMATION

The following sections contain procedures necessary to properly operate the AD9217 within a given application.

START-UP SEQUENCE

To start the device, take the following steps:

1. Power up the AD9217. There is no supply sequencing requirement. The sample clock can be applied after power is applied. The sample clock must be applied before the write to Register 0x26 = 0x08 (see Step 5).
2. Assert a Pin Reset. Take the AD9217 RSTB pin from high (SVDD2 voltage) to low (0 V), then back to high (SVDD2 voltage).
3. Write Register 0x0 = 0x24 to set the SPI address ascension mode to increment.
4. Wait 100 ms before performing the next step.
5. Write Register 0x26 = 0x08 to configure the AD9217 to receive sample clock signal. Sample clock must be applied before this step is performed.
6. Wait 100 ms before performing the next step.
7. Write Register 0x570, Bit 0 = 0, powers down output interface PLL.
8. Write Register 0x570, Bit 0 = 1, powers up output interface PLL.
9. With Register 0x4BE Bit7 = 0 (default), read Register 0x4BF. Confirm if output interface PLL is locked, Bit 7 = 1 indicates lock.

TRANSFER BIT

Writes to Register 0x1601 through Register 0x1617 must be followed by writing Register 0x1600 = 0x01. Setting this transfer bit places previous writes to Register 0x1601 through Register 0x1617 into effect. An exception is writes to registers needed for changing sample clock frequency without power-down, Register 0x1602 and Register 0x1614. Writes to these registers do not need to be followed by setting the transfer bit.

CHANGING SAMPLE CLOCK FREQUENCY WITHOUT POWER DOWN

To change the sample clock frequency (encode clock rate) without powering-down the ADC, take the following steps:

1. Write Register 0x332 = 0x02 to alert the AD9217 that the user is changing the clock frequency.
2. Read Register 0x1614, Bit 0. Wait for this bit to go high, which indicates that the user can change the encode clock rate.
3. Write Register 0x1602 = 0x01. This selects the coefficient location for Clock Rate 1.
4. Change the frequency of the clock applied to the CLK_P and CLK_N pins.
 - a. Change any other necessary parameters due to the clock frequency change. For example, HSP output interface PLL divider settings related to clock rate changes.

5. Write Register 0x1614, Bit 1 = 1. This notifies the AD9217 that the sample clock frequency has been changed.
6. Read Register 0x1614, Bit 2. Wait for this bit to go high which indicates that the change is complete.

The AD9217 now functions at the new sample frequency.

The coefficients from Register 0x1602 = 0x01 are now for the new, user selected clock frequency. At this point, coefficients are stored for two clock frequencies: Register 0x1602 = 0x00, coefficients for Clock Rate 0 (the original sample rate), and Register 0x1602 = 0x01, coefficients for Clock Rate 1 (the new sample rate).

To return to the original sample rate (Clock Rate 0), perform the procedure outlined in this section and set the Register 0x1602 clock rate parameter to Clock Rate 0.

The AD9217 now functions at the selected sample frequency, and the ADC is ready for operation at Clock Rate 0 within a few microseconds.

The procedure described in this section can be performed for four sample clock frequencies, including the original frequency used by the AD9217 at power-up. The coefficients for different clock frequencies are accessed by the different writes to Register 0x1602.

The following are examples of write operations to access the coefficients for various clock frequencies:

- Write Register 0x1602 = 0x00. This is the default value and contains coefficients for the original sample clock frequency (Clock Rate 0).
- Write Register 0x1602 = 0x01. This is points to Clock Rate 1 and contains coefficients for the user selected clock frequency (Clock Rate 1).
- Write Register 0x1602 = 0x02. This is points to Clock Rate 2 and contains coefficients for the user selected clock frequency (Clock Rate 2).
- Write Register 0x1602 = 0x03. This is points to Clock Rate 3 and contains coefficients for the user selected clock frequency (Clock Rate 3).

The coefficients for 10 GSPS are initially stored in all four locations by default.

The first time a sample clock frequency is used, a few seconds are required for the coefficients to converge and store as Clock Rate 0, Clock Rate 1, Clock Rate 2, or Clock Rate 3. In the next instance a specific clock rate is used with its associated set of stored coefficients, only a few microseconds are required to make the change. Note that additional time is required for the device to perform the SPI writes described in this section.

This procedure must be performed from the beginning if the AD9217 is powered down.

APPLICATIONS INFORMATION

CONFIGURING THE AD9217 TO OPERATE IN JESD204B MODE

The high speed parallel output interface of the AD9217 can be configured to operate as a JESD204B interface. When configured in this way, the operation is identical to the JESD204B interface of the [AD9213](#). Refer to the AD9213 data sheet for information on how to configure and operate the AD9217 after it is placed in JESD204B mode.

After the AD9217 enters JESD204B mode, signals and balls that are not used for the device in default parallel output mode become necessary. The pin assignments of the AD9217 in JESD204B mode are the same as for AD9213. Refer to the Pin Configuration diagram and Pin Function Descriptions table in the AD9213 data sheet for pin definitions of the AD9217 in JESD204B mode.

What follows is an example register sequence that places the AD9217 in JESD204B mode. The registers designated as AD9213 register are described in the AD9213 data sheet register map table.

1. Write Register 0x4BD, Bit 0 = 1 to power down the HSP interface.
2. Write Register 0x4B2, Bit 0 = 0 to enable JESD204B mode.
3. Write Register 0x570, Bit 0 = 0 to power down the output interface PLL.
4. Write Register 0x503, Bit 0 = 1 to power down the JESD204B transmit link (AD9213 register).
5. Write Register 0x53B, Bits[7:0] = 0xFF to power down Physical Lane 0 through Physical Lane 7 (AD9213 register).
6. Write Register 0x53C, Bits[7:0] = 0xFF to power down Physical Lane 8 through Physical Lane 15 (AD9213 register).
7. Write Register 0x524, Bits[4:0] = 0x0B to select JESD204B N = 12 (AD9213 register).
8. Write Register 0x525, Bits[7:5] = 0x00 to select JESD204B Subclass 0 (AD9213 register).
9. Write Register 0x504, Bit 4 = 1 to select the SYNC pin to be LVDS (AD9213 register).
10. Write Register 0x509, Bits[1:0] = 0x02 to set the JESD204B control bits to be undefined (default) (AD9213 register).
11. Write Register 0x524, Bits[7:6] = 0x03 to select JESD204B CS = 3 (all control bits enabled) (AD9213 register).
12. Write Register 0x570, Bit 0 = 1 to power up the output interface PLL (AD9213 register).
13. Write Register 0x503, Bit 0 = 0 to power up the JESD204B transmit link (AD9213 register).
14. Write Register 0x5D2, Bits[7:0] = 0xFF to take the Lane 0 through Lane 7 digital logic out of reset and into normal operation.
15. Write Register 0x5D3, Bits[7:0] = 0xFF to take the Lane 8 through Lane 15 digital logic out of reset and into normal operation.

16. Write Register 0x5B0, Bits[7:0] = 0x00 to power up the PHY for Lane 0 through Lane 7.
17. Write Register 0x5B1, Bits[7:0] = 0x00 to power up the PHY for Lane 8 through Lane 15.
18. Write Register 0x53B, Bits[7:0] = 0x00 to power up Physical Lane 0 through Physical Lane 7 (AD9213 register).
19. Write Register 0x53C, Bits[7:0] = 0x00 to power up Physical Lane 8 through Physical Lane 15 (AD9213 register).
20. Write Register 0x681, Bit 4 = 1 to enable the DDC and JTX clocks (AD9213 register).
21. Wait 1 sec.
22. Read Register 0x501, Bit 7. When Bit 7 = 1, this indicates JESD204B PLL lock (AD9213 register).

POWER SUPPLY RECOMMENDATIONS

Several of the AD9217 supply domains can be combined and powered by the supply configuration shown in [Figure 90](#) if desired. This is an example configuration for minimizing power supply components and power domains. This approach can increase the risk of switching regulator artifacts being injected into the power supply domains of the ADC. Initial evaluations using this configuration suggest the noise impact is minimal and is typically outweighed by its simplicity and use of fewer power supply components. Use of linear regulators and isolating specific supply pins can result in less noise.

Among the supplies that share a regulator, there is a benefit to decoupling the sensitive supplies from others at the board level by dedicating a power plane to the sensitive supply. For example, although CLKVDD_LF is grouped together with other 1 V digital supplies (see [Figure 90](#)), dedicating a power plane exclusively to CLKVDD_LF reduces noise from the digital supplies coupling to affect the clock power domain. A separate supply branch allows CLKVDD_LF to be routed to its own bypass capacitor, placed close to the package on the PCB top layer or directly underneath (adjacent to the ground pin) when connected through a PCB via. For further decoupling, a series ferrite can be inserted at the branch point shared with the other 1V supply feeds.

An effective way to add power supply bypass capacitance to the AD9217 PCB is to use through vias on the AD9217 BGA power pads. Use 0201 (0603 Metric), 0.1 μ F surface mount capacitors directly below the BGA footprint on the opposite side of the board, connecting the supply pins to the adjacent ground pins. Surface mount solder pads are required to accommodate the capacitors.

All ground pins can be connected to the same planes and combined into one domain at the board level

APPLICATIONS INFORMATION

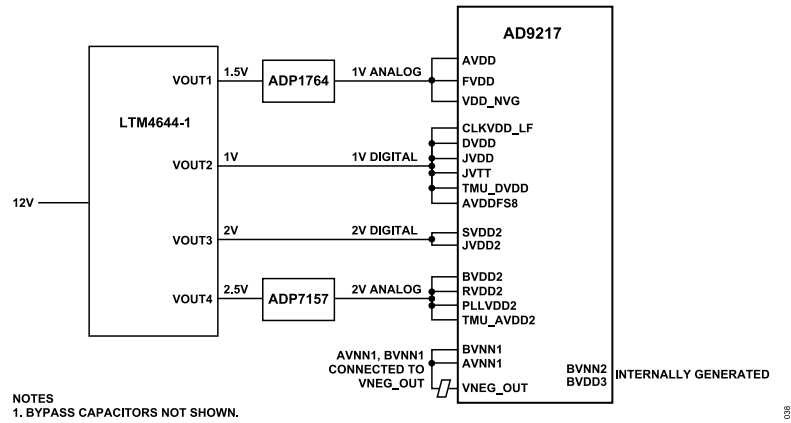


Figure 90. Alternate Simplified Power Supply Configuration

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
BP-192-1	BGA_ED	192-Ball Ball Grid Array, Thermally Enhanced

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range ²	Package Description	Package Option
AD9217BBPZ-6G	-20°C to +115°C	192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-192-1
AD9217BBPZ-10G	-20°C to +115°C	192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-192-1

¹ Z = RoHS Compliant Part.

² Specified operating junction temperature (T_J). Startup at T_J = -40°C is guaranteed.

EVALUATION BOARDS

Model ¹	Description
AD9217-6GEBZ	Evaluation Board
AD9217-10GEBZ	Evaluation Board

¹ Z = RoHS Compliant Part.

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