SBVS101–DECEMBER 2007

16-Channel, 16-Bit PWM LED Driver with 7-Bit Global Brightness Control

FEATURES

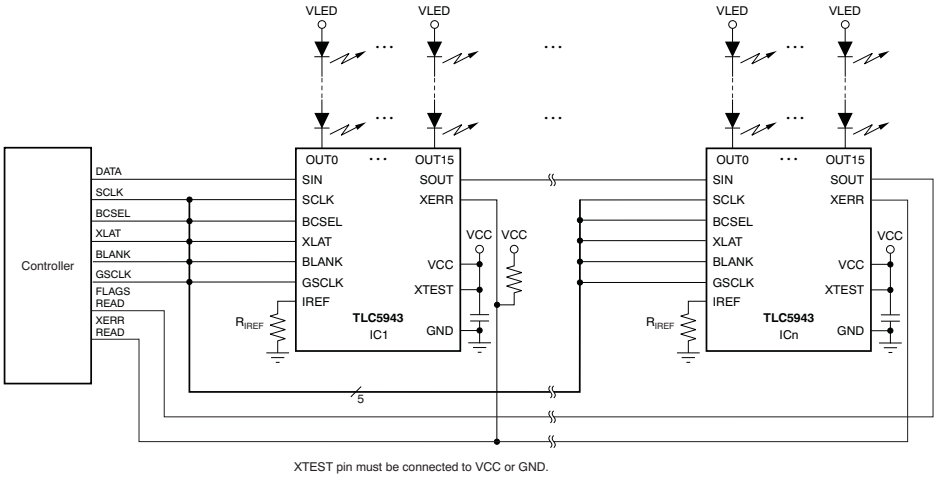
- 16 Channels, Constant Current Sink Output
- 50-mA Capability (Constant Current Sink)
- 16-Bit (65,536 Steps) Grayscale Control with Enhanced Spectrum (ES) PWM
- 7-Bit (128 Steps) Global Brightness Control for All Channels with Sink Current
- LED Power-Supply Voltage up to 17 V
- V_{CC} = 3.0 V to 5.5 V
- Constant Current Accuracy:
  - Channel-to-Channel = ±1.5%
  - Device-to-Device = ±3%
- CMOS Level I/O
- 30-MHz Data Transfer Rate
- 33-MHz Grayscale Control Clock
- Auto Display Repeat
- Auto Data Refresh
- Continuous Base LED Open Detection (LOD):
  - Detect LED opening and LED short to GND during display
- Thermal Shutdown (TSD):
  - Automatic shutdown at high temperature conditions
  - Restart under normal temperature
- Readable Error Information:
  - LED Open Detection (LOD)
  - Thermal Error Flag (TEF)
- Noise Reduction:
  - 4-channel grouped delay to prevent inrush current
- Operating Temperature: –40°C to +85°C

APPLICATIONS

- Monochrome, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting

DESCRIPTION

The TLC5943 is a 16-channel, constant current sink driver. Each channel is individually adjustable with 65,536 enhanced spectrum pulse-width modulated (PWM) steps controlled by grayscale (GS) data. All output drivers are adjustable with 128 constant sink current steps at same value controlled by brightness control (BC) data. Both GS data and BC data are writable via a serial interface port. The maximum current value of all 16 channels can be set by a single external resistor.



Typical Application Circuit (Multiple Daisy-Chained TLC5943s)

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DESCRIPTION, CONTINUED

The TLC5943 has two error detection circuits for LED open detection (LOD) and a thermal error flag (TEF). LOD detects a broken or disconnected LED and shorted LED to GND during the display period. TEF indicates an over-temperature condition; when a TEF is set, all output drivers are turned off. When the TEF is cleared, all output drivers are restarted.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5943	HTSSOP-28 PowerPAD™	TLC5943PWPR	Tape and Reel, 2000
		TLC5943PWP	Tube, 50
TLC5943	5 mm × 5 mm QFN-32	TLC5943RHBR	Tape and Reel, 3000
		TLC5943RHBT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5943	UNIT
V_{CC}	Supply voltage, V_{CC}		–0.3 to +6.0	V
I_{OUT}	Output current (dc): OUT0 to OUT15		60	mA
V_{IN}	Input voltage range: SIN, SCLK, XLAT, BLANK, GSCLK, BCSEL, IREF		–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT, XERR	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to +18	V
$T_{J(max)}$	Maximum operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
	ESD rating	Human body model (HBM)	2	kV
		Charged device model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

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RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5943			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			17	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
		XERR			5	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15			50	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (sclk)}$	Data shift clock frequency	SCLK			30	MHz
$f_{CLK\ (gsclk)}$	Grayscale control clock frequency	GSCLK			33	MHz
T_{WH0} / T_{WL0}	Pulse duration	SCLK, GSCLK	10			ns
T_{WH1}		XLAT, BLANK	30			ns
T_{SU0}	Setup time	SIN–SCLK↑	6			ns
T_{SU1}		XLAT↑–SCLK↑	100			ns
T_{SU2}		BLANK↓–GSCLK↑	10			ns
T_{SU3}		BCSEL–SCLK↑	10			ns
T_{SU4}		BCSEL–XLAT↑	30			ns
T_{SU5}		XLAT↓–SCLK↑	15			ns
T_{SU6}		XLAT↑–BLANK↓	20			ns
T_{H0}	Hold time	SIN–SCLK↑	3			ns
T_{H1}		XLAT↑–SCLK↑	30			ns
T_{H2}		BCSEL–SCLK↓	10			ns
T_{H3}		BCSEL–XLAT↑	100			ns

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
HTSSOP-28 with PowerPAD soldered (1)	31.67 mW/°C	3958 mW	2533 mW	2058 mW
HTSSOP-28 with PowerPAD not soldered (2)	16.21 mW/°C	2026 mW	1296 mW	1053 mW
QFN-32 (3)	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

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ELECTRICAL CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5943			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT	0		0.4	V
		I_{OL} = 5 mA at XERR			0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, SCLK, GSCLK, XLAT, BLANK, BCSEL	–1		1	µA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/GSCLK/XLAT/BCSEL = low, BLANK = high, GSn = FFFFh, BCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 10 kΩ		1	3	mA
I_{CC2}		SIN/SCLK/GSCLK/XLAT/BCSEL = low, BLANK = high, GSn = FFFFh, BCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 2 kΩ		4	8	mA
I_{CC3}		SCLK/GSCLK = 30 MHz, SIN = 15MHz, XLAT/BCSEL/BLANK = low, GSn = FFFFh, BCn = 7Fh, Auto Repeat on, V_{OUTn} = 1 V, R_{IREF} = 2 kΩ (1)		14	30	mA
I_{CC4}		SCLK/GSCLK = 30 MHz, SIN = 15MHz, XLAT/BCSEL/BLANK = low, GSn = FFFFh, BCn = 7Fh, Auto Repeat on, V_{OUTn} = 1 V, R_{IREF} = 1 kΩ (1)		27	50	mA
$I_{O(LC)}$	Constant output current	All OUTn = ON, BCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ	43	49	55	mA
$I_{O(LKG1)}$	Leakage output current	BLANK = high, R_{IREF} = 1 kΩ, V_{OUTn} = 17 V, At OUT0 to OUT15			0.1	µA
$I_{O(LKG2)}$	Leakage output current	No error condition, V_{XERR} = 5.5 V, at XERR			1	µA
$\Delta I_{O(LC)}$	Constant current error (pin-to-pin) (1)	All OUTn = ON, BCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ, at OUT0 to OUT15		±1.5	±4	%
$\Delta I_{O(LC1)}$	Constant current error (device-to-device) (2)	All OUTn = ON, BCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ		±3	±9	%
$\Delta I_{O(LC2)}$	Line regulation (3)	All OUTn = ON, BCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ, at OUT0 to OUT15		±1	±4	%/V
$\Delta I_{O(LC3)}$	Load regulation (4)	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ, at OUT0 to OUT15		±1	±3	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature (5)	+150	+162	+175	°C
$T_{(HYS)}$	Thermal error hysteresis	Junction temperature (5)	+5	+10	+20	°C
V_{LOD}	LED open detection threshold	All OUTn = ON	0.2	0.3	0.4	V
V_{IREF}	Reference voltage output	R_{IREF} = 1 kΩ	1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT15 constant current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT15 constant current average from the ideal constant current value. Deviation is calculated by the following formula:

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 41 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5 \text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})} \right) \times \frac{100}{5.5 \text{ V} - 3 \text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3 \text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})} \right) \times \frac{100}{3 \text{ V} - 1 \text{ V}}$$

(5) Not tested. Specified by design.

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SWITCHING CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 82 Ω, R_{IREF} = 1 kΩ, and V_{LED} = 5.0 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5943			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT			16	ns
t_{R1}		OUTn, BC = 7Fh		10	30	
t_{F0}	Fall time	SOUT			16	ns
t_{F1}		OUTn, BC = 7Fh		10	30	
t_{F2}		XERR, C_L = 100 pF, R_L = 1 kΩ, V_{XERR} = 5 V			100	ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT			25	ns
t_{D1}		BLANK↑ to OUT0 sink current off		20	40	ns
t_{D2}		GSCLK↑ to OUT0/4/8/12	5	18	40	ns
t_{D3}		GSCLK↑ to OUT1/5/9/13	20	42	73	ns
t_{D4}		GSCLK↑ to OUT2/6/10/14	35	66	106	ns
t_{D5}		GSCLK↑ to OUT3/7/11/15	50	90	140	ns
t_{ON_ERR}	Output on-time error(1)	GSn = 0001h, GSCLK = 33 MHz	–20		10	ns

(1) Output on-time error is calculated by the following formula: T_{ON_ERR} (ns) = t_{OUTON} – T_{GSCLK}. t_{OUTON} is the actual on-time of the constant current driver. T_{GSCLK} is the period of GSCLK.

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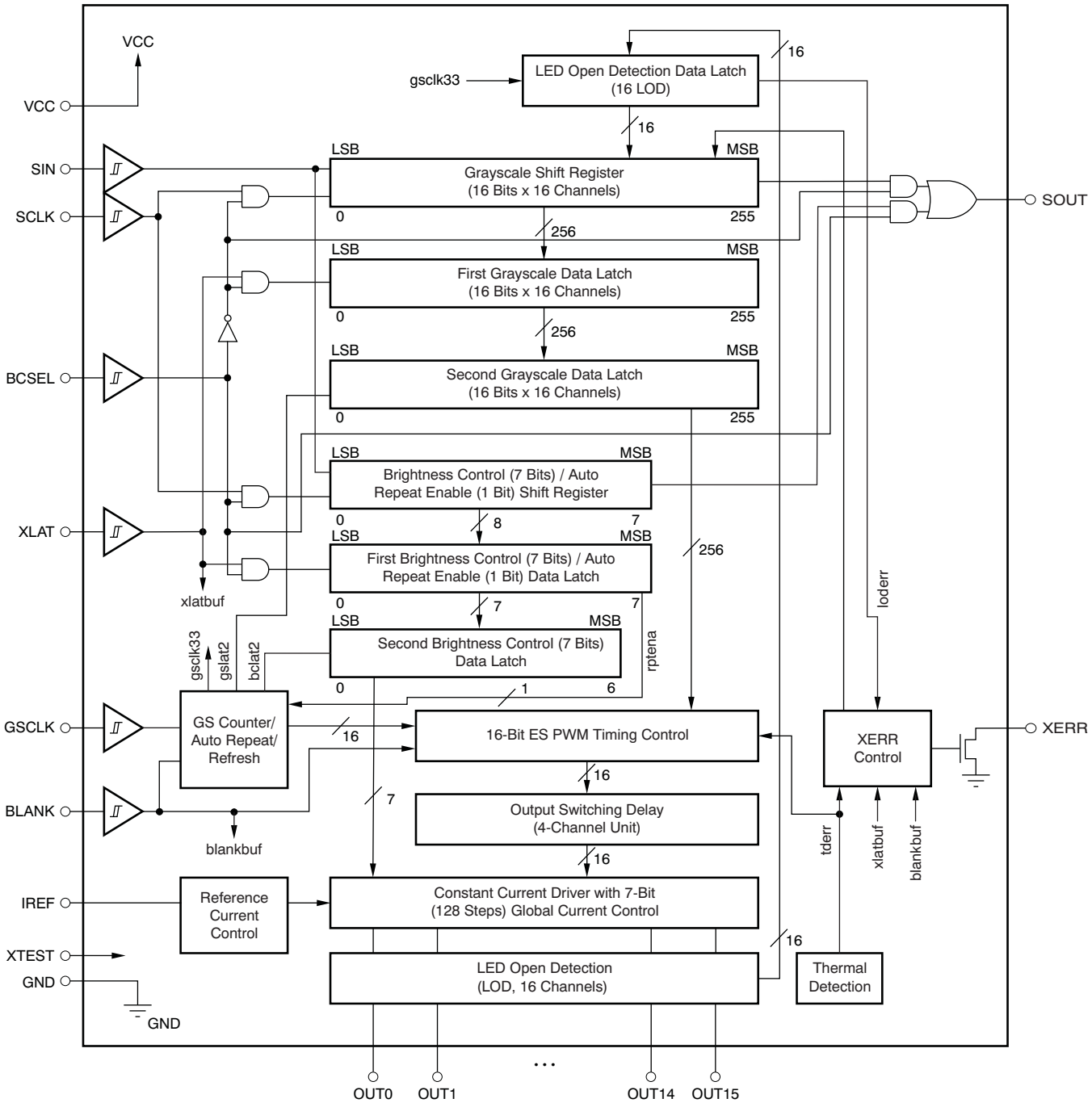
FUNCTIONAL BLOCK DIAGRAM



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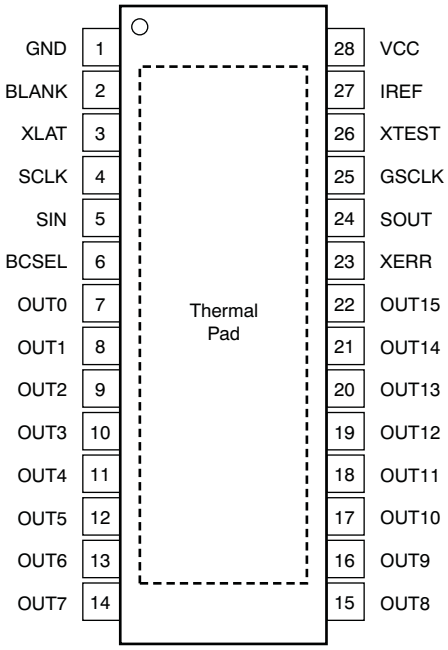
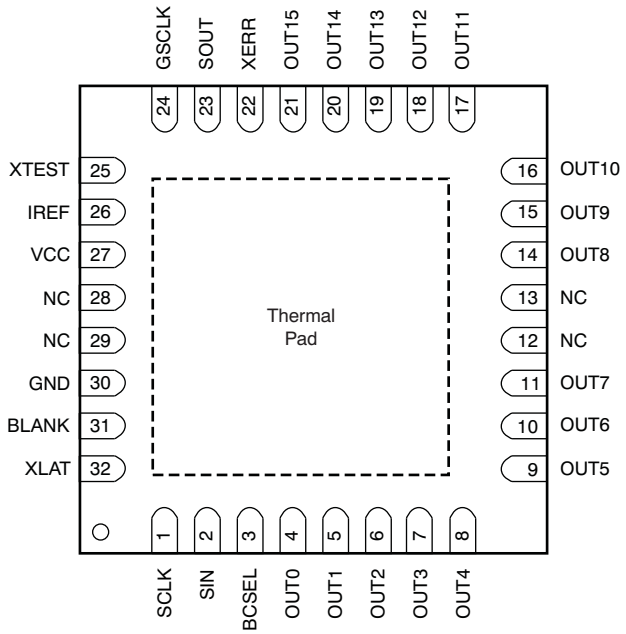
DEVICE INFORMATION

PWP PACKAGE
(Top View)



RHB PACKAGE
(Top View)



NC = No internal connection.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	PWP	RHB		
SIN	5	2	I	Serial data input for grayscale and brightness control data. Schmitt buffer input.
SCLK	4	1	I	Serial data shift clock for GS shift register and BC shift register. Schmitt buffer input. The shift register is selected by BCSEL. Data present on the SIN pin are shifted into the shift register selected by BCSEL with the rising edge of the SCLK pin. Data in the selected shift register are shifted to the MSB side by 1-bit synchronizing to the rising edge of SCLK. The MSB data of the selected register appears on SOUT.
XLAT	3	32	I	Data in the Grayscale and Brightness shift register are moved to the respective first data latch with a low-to-high transition of this pin.
BCSEL	6	3	I	Shift register and data latch select. Schmitt buffer input. When BCSEL is low, Grayscale shift register and first data latch are selected. When BCSEL is high, Brightness Control shift register and first data latch are selected. BCSEL should not be changed while SCLK is high.
GSCLK	25	24	I	Reference clock for Grayscale PWM control. Schmitt buffer input. If BLANK is low, then each rising edge of GSCLK increments the grayscale counter for PWM control.
BLANK	2	31	I	Blank (all constant current outputs off). Schmitt buffer input. When BLANK is high, all constant current outputs (OUT0 through OUT15) are forced off, the Grayscale counter is reset to '0', and the Grayscale PWM timing controller is initialized. When BLANK is low, all constant current outputs are controlled by the Grayscale PWM timing controller.
IREF	27	26	I/O	Constant current value setting. OUT0 through OUT15 sink constant current is set to desired value by connecting an external resistor between IREF and GND.
SOUT	24	23	O	Serial data output. This output is connected to Grayscale/Status Information shift register or Brightness Control shift register. The connected register is selected by BCSEL.
XERR	23	22	O	Error output. Open-drain output. XERR goes low when LOD or TEF is detected.
OUT0	7	4	O	Constant current output.
OUT1	8	5	O	Constant current output
OUT2	9	6	O	Constant current output
OUT3	10	7	O	Constant current output
OUT4	11	8	O	Constant current output
OUT5	12	9	O	Constant current output
OUT6	13	10	O	Constant current output
OUT7	14	11	O	Constant current output
OUT8	15	14	O	Constant current output
OUT9	16	15	O	Constant current output
OUT10	17	16	O	Constant current output
OUT11	18	17	O	Constant current output
OUT12	19	18	O	Constant current output
OUT13	20	19	O	Constant current output
OUT14	21	20	O	Constant current output
OUT15	22	21	O	Constant current output
VCC	28	27	—	Power-supply voltage
GND	1	30	—	Power ground
XTEST	26	25	I	Factory test pin. XTEST must be connected to VCC or GND.
NC	—	12, 13, 28, 29	—	No internal connection

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PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

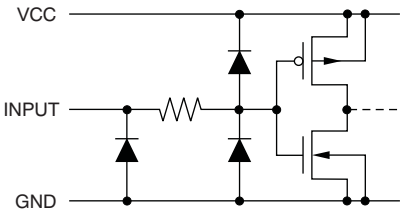


Figure 1. SIN, SCLK, XLAT, BCSEL, BLANK, GSCLK

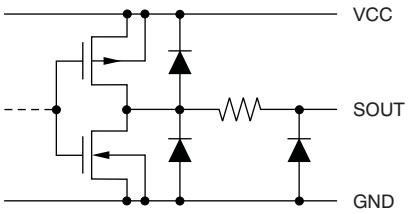


Figure 2. SOUT

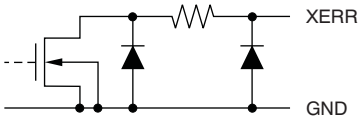


Figure 3. XERR

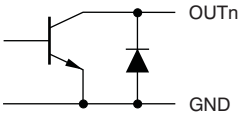
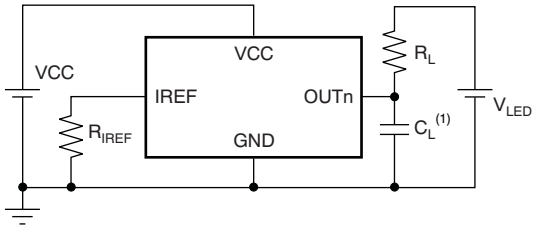


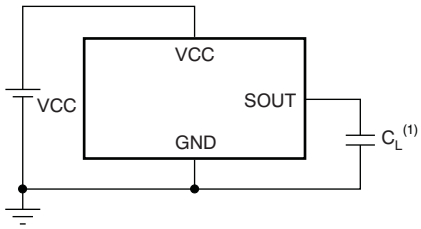
Figure 4. OUT0 Through OUT15

TEST CIRCUITS



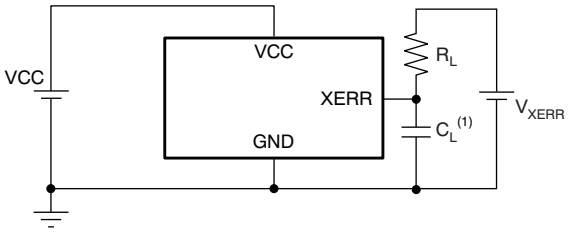
(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 6. Rise Time and Fall Time Test Circuit for SOUT



(1) C_L includes measurement probe and jig capacitance.

Figure 7. Rise Time and Fall Time Test Circuit for XERR

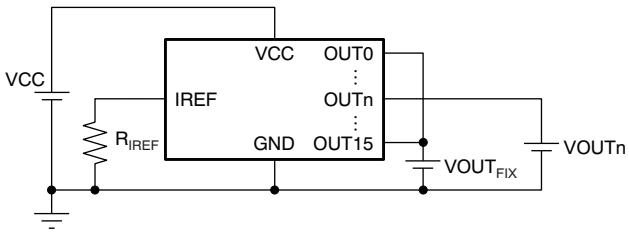
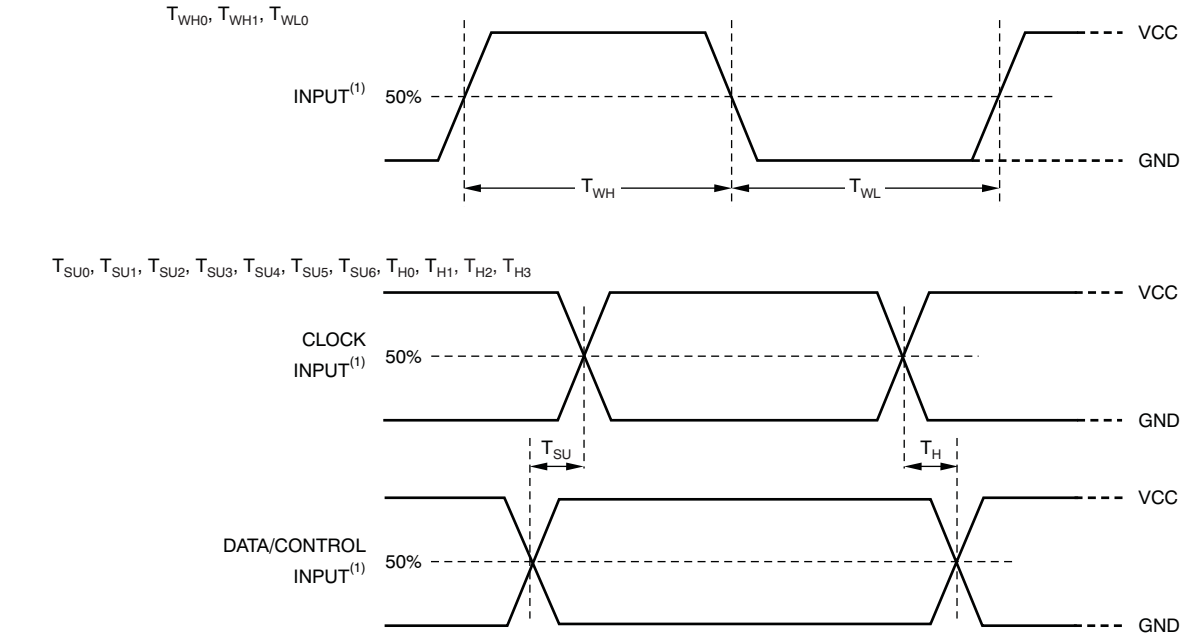


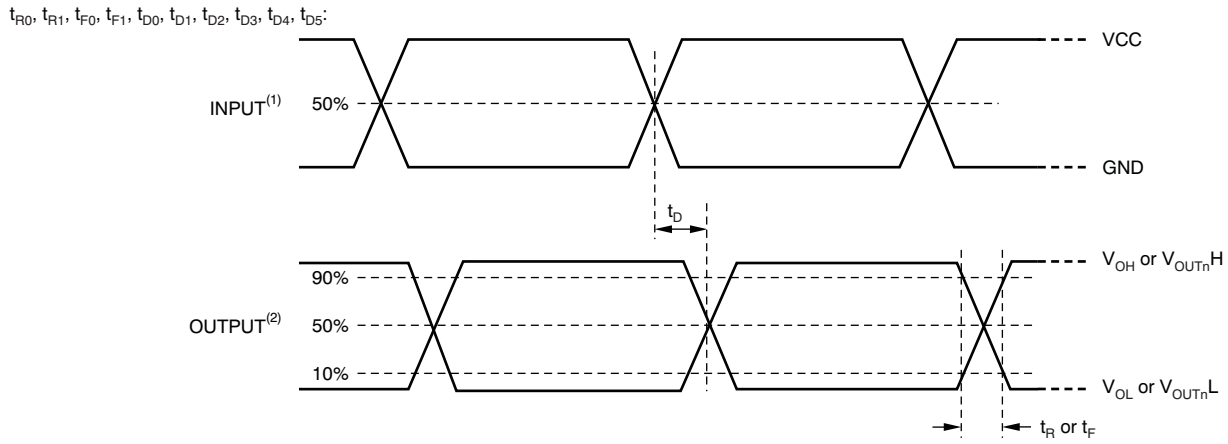
Figure 8. Constant Current Test Circuit for OUTn

TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 9. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

(2) Input pulse high level is V_{CC} and low level is GND.

Figure 10. Output Timing

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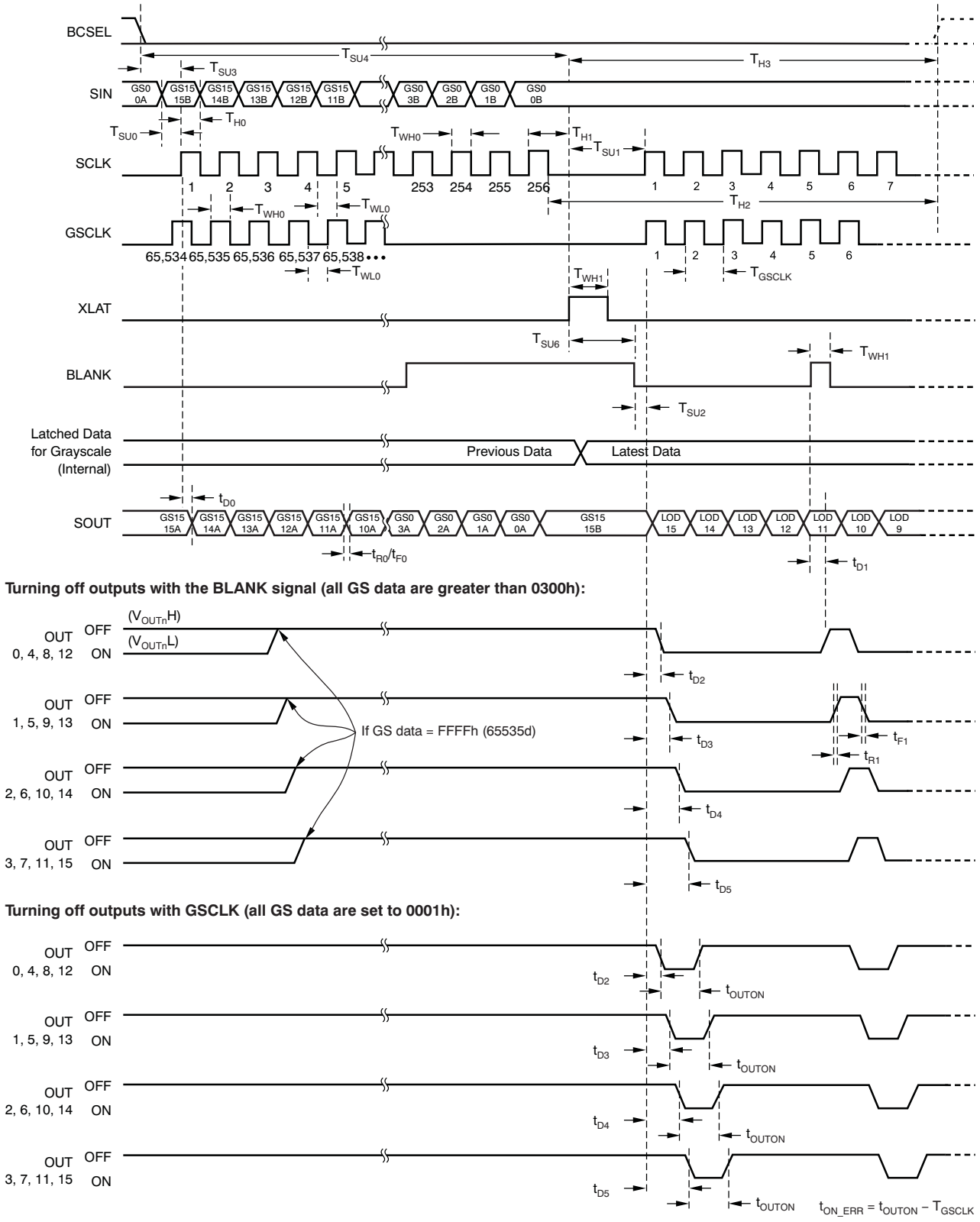


Figure 11. Grayscale Data Write and Constant Current Output Timing

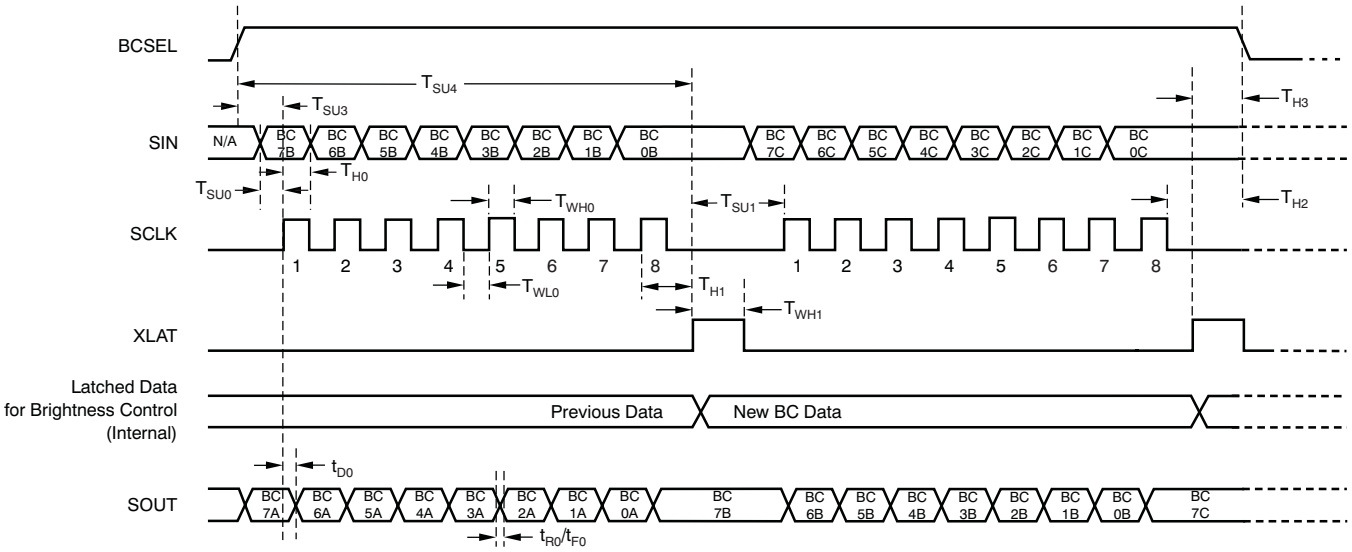
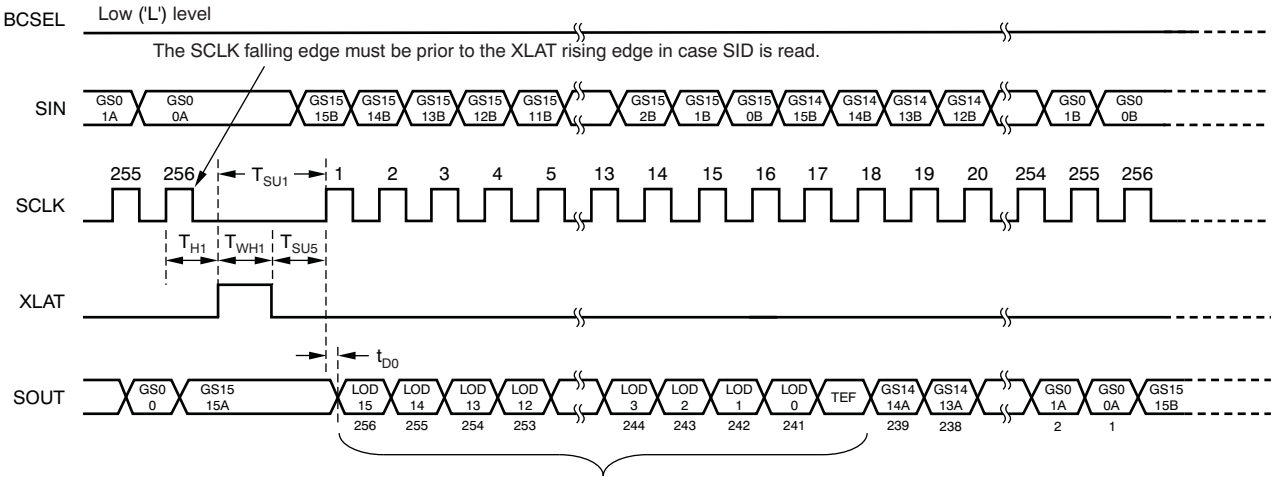


Figure 12. Brightness Control Data Write Timing



SID are entered in the GS shift register at the first rising edge of SCLK after XLAT goes low.
The SID readout consists of the saved LOD result at the 33rd GSCLK rising edge in the previous display period and the TEF data after the previous TEF data readout.

Figure 13. Status Information Data Read Timing

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TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

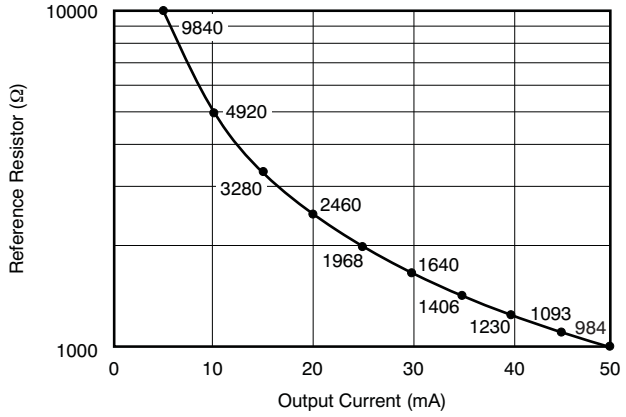

Figure 14.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

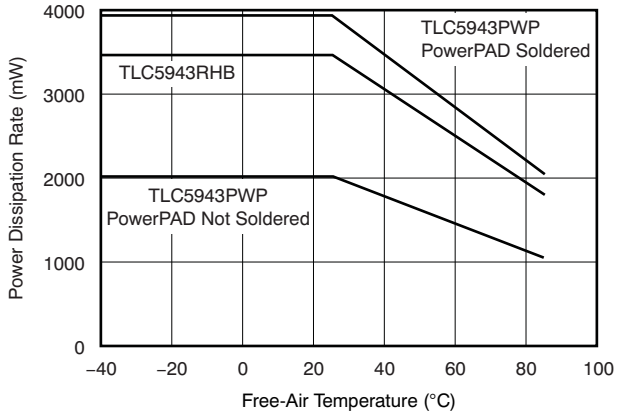

Figure 15.

OUTPUT CURRENT vs OUTPUT VOLTAGE

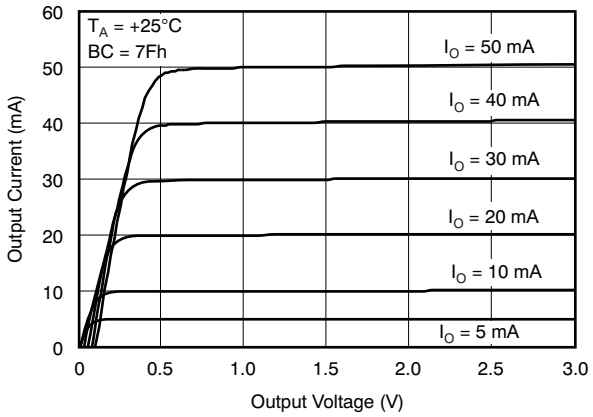

Figure 16.

OUTPUT CURRENT vs OUTPUT VOLTAGE

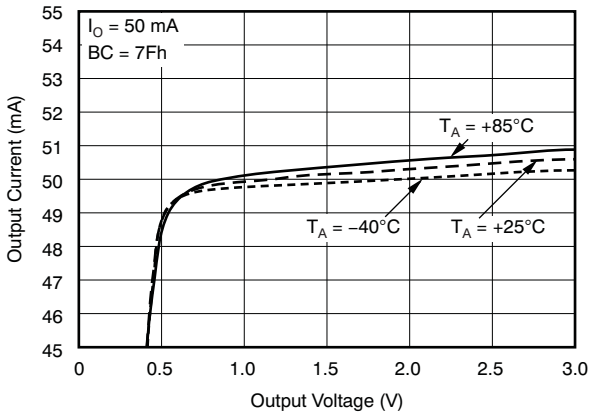

Figure 17.

ΔI_{OLC} vs AMBIENT TEMPERATURE

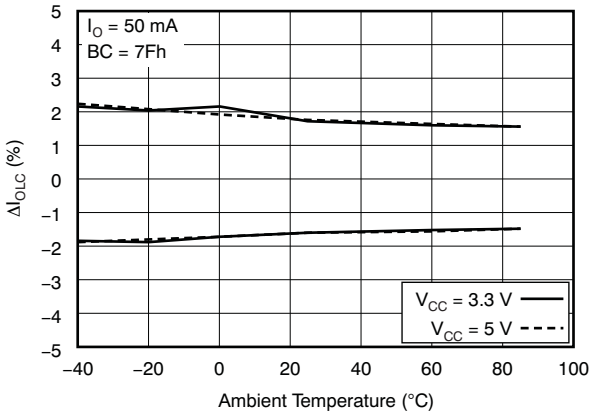

Figure 18.

ΔI_{OLC} vs OUTPUT CURRENT

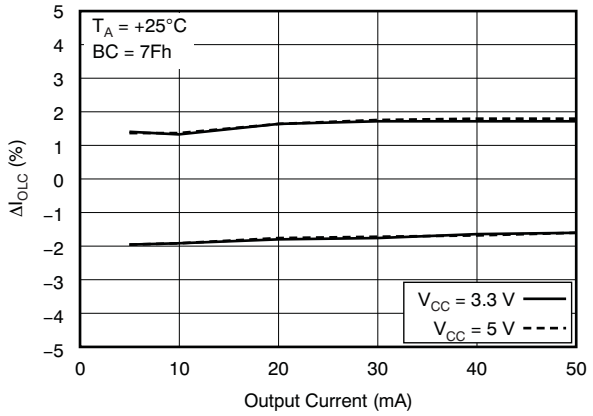

Figure 19.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

BRIGHTNESS CONTROL LINEARITY

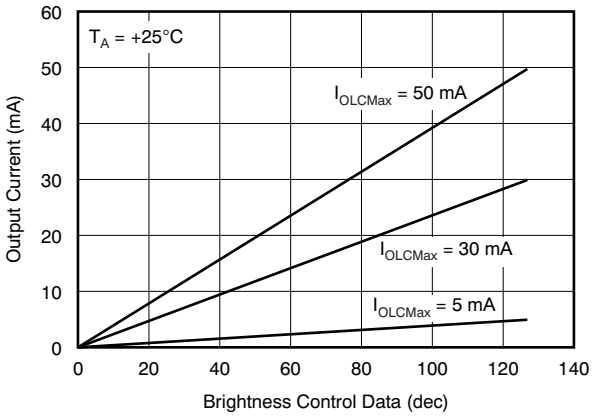

Figure 20.

BRIGHTNESS CONTROL LINEARITY

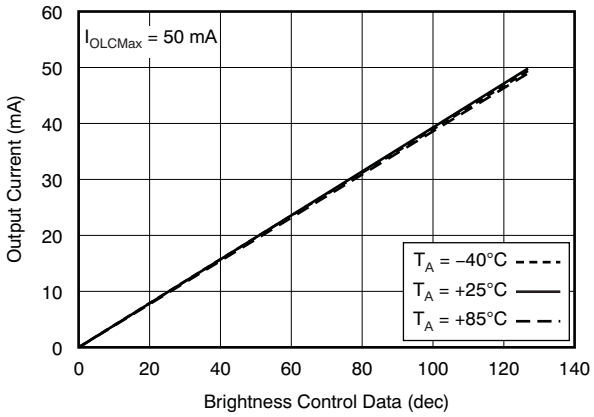

Figure 21.

CONSTANT CURRENT OUTPUT VOLTAGE WAVEFORM

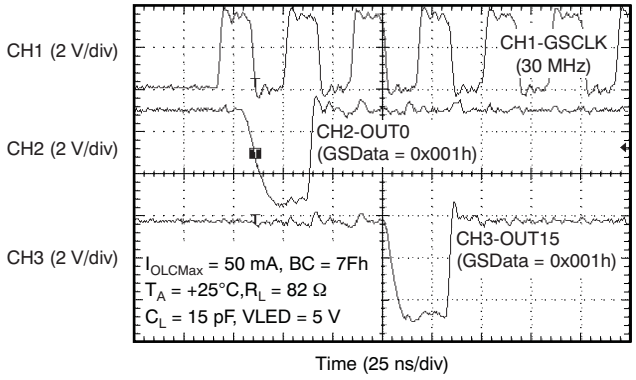

Figure 22.

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DETAILED DESCRIPTION

Setting for the Maximum Constant Sink Current Value

On the TLC5943, the maximum constant current sink value for each channel, I_{OLCMax}, is determined by an external resistor, R_{IREF}, placed between the IREF and GND pins. The R_{IREF} resistor value is calculated with Equation 1:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 41 \quad (1)$$

Where:

- V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V)

I_{OLCMax} is the largest current for all outputs. Each output sinks the I_{OLCMax} current when it is turned on and the brightness control data are set to the maximum value of 7Fh (127d). The sink current for each output can be reduced by lowering the brightness control data.

R_{IREF} must be between 984 Ω (typ) and 9.84 kΩ (typ) in order to keep I_{OLCMax} between 5 mA and 50 mA. The output may become unstable when I_{OLCMax} is set lower than 5 mA. However, output currents lower than 5 mA can be achieved by setting I_{OLCMax} to 5 mA or higher, and then using brightness control to lower the output current.

Figure 14 in the Typical Characteristics and Table 1 show the characteristics of the constant sink current versus the external resistor, R_{IREF}.

Table 1. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA, Typical)	R_{IREF} (Ω)
50	984
45	1093
40	1230
35	1406
30	1640
25	1968
20	2460
15	3280
10	4920
5	9840

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Brightness Control (BC) Function

The TLC5943 is able to adjust the output current of all channels (OUT0 to OUT15). This function is called *brightness control* (BC). The BC function allows users to adjust the global brightness of LEDs connected to the outputs OUT0 to OUT15. All channel output currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The brightness control data are entered into the TLC5943 via the serial interface.

Equation 2 determines the sink current for each output (OUTn):

$$I_{OUTn}\ (mA) = I_{OLCMax}\ (mA) \times \left(\frac{BCn}{127d}\right) \quad (2)$$

Where:

- I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}
- BCn = the programmed brightness control value for OUTn (BCn = 0 to 127d)

When the IC is powered on, the data in the Brightness Control Shift Register and data latch 1 and 2 are not set to any default values. Therefore, BC data must be written to the BC latch 1 and 2 before turning on the constant current output.

Table 2 summarizes the BC data versus current ratio and set current value.

Table 2. BC Data versus Current Ratio and Set Current Value

BC DATA (Binary)	BC DATA (Decimal)	BC DATA (Hex)	SET CURRENT RATIO TO MAX CURRENT (%)	OUTPUT CURRENT (mA, Typical) AT I_{OLCMax} = 50 mA	OUTPUT CURRENT (mA, Typical) AT I_{OLCMax} = 5 mA
000 0000	0	00	0.0	0.0	0.00
000 0001	1	01	0.8	0.4	0.04
000 0010	2	02	1.6	0.8	0.08
... ...	... ...	... ...	... ...	... ...	... ...
111 1101	125	7D	98.4	49.2	4.92
111 1110	126	7E	99.2	49.6	4.96
111 1111	127	7F	100.0	50.0	5.00

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Grayscale (GS) Function (Enhanced Spectrum PWM Operation)

The TLC5943 has an enhanced spectrum pulse-width modulation (ES PWM) function. In this PWM control, the total display period is divided to 128 display segments. *Total display period* means the timing from the first grayscale clock (GSCLK) input to the 65,536th grayscale clock input after BLANK goes low. Each display period has 512 grayscale as a maximum. The driver (OUTn) on time changes depending on the 16-bit grayscale data. Refer to Table 3 for sequence information and Figure 23 for timing information.

Table 3. ES PWM Drive Turn-On Time Length

GS DATA (Dec)	GS DATA (Hex)	OUTn DRIVER OPERATION
0	0000h	No turn on
1	0001h	Turns on during 1GSCLK period in first display period
2	0002h	Turns on during 1GSCLK period in first and 65th display periods
3	0003h	Turns on during 1GSCLK period in first, 65th, and 33rd display periods
4	0004h	Turns on during 1GSCLK period in first, 65th, 33rd, and 97th display periods
5	0005h	Turns on during 1GSCLK period in first, 65th, 33rd, 97th, and 17th display periods
6	0006h	Turns on during 1GSCLK period in first, 65th, 33rd, 97th, 17th, and 81st display periods
---	---	The number of display periods in which OUTn turns on during 1GSCLK is increased by GS data increasing in the following order. The display period order in which OUTn turns on : 1>65>33>97>17>81>49>113>9>73>41>105>25>89>57>121>5>69>37>101>21> 85>53>117>13>77>45>109>29>93>61>125>3>67>35>99>19>83>51>115>11> 75>43>107>27>91>59>123>7>71>39>103>23>87>55>119>15>79>47>111>31> 95>63>127>2>66>34>98>18>82>50>114>10>74>42>106>26>90>58>122>6>70> 38>102>22>86>54>118>14>78>46>110>30>94>62>126>4>68>36>100>20>84> 52>116>12>76>44>108>28>92>60>124>8>72>40>104>24>88>56>120>16>80> 48>112>32>96>64>128.
127	007Fh	Turns on during 1GSCLK period in first through 127th display period. No turn on in 128th display period only.
128	0080h	Turns on during 1GSCLK period in all (1 through 128th) display periods.
129	0081h	Turns on during 2GSCLK periods in first display period and 1GSCLK period in other display periods.
---	---	The number of display periods in which OUTn turns on during 2GSCLKs increases by GS data as when GS is 130 through 254.
255	00FFh	Turns on during 2GSCLKs period in 1 through 127th display period and turns on 1GSCLK period in 128th display period only.
256	0100h	Turns on during 2GSCLK periods in all (1 through 128th) display periods.
257	0101h	Turns on during 3GSCLK periods in first display period and 2GSCLK periods in other display periods.
---	---	Display period in which OUTn turn-on time increases by GS data, increasing as does above operation
65478	FEFFh	Turns on during 511 GSCLK period in 1 through 127th display period and turns on 510 GSCLK period in 128th display period only.
65279	FF00h	Turns on during 511 GSCLK period in all (1 through 128th) display periods.
65280	FF01h	Turns on during 512 GSCLK period in first display period + 511 GSCLK period in second through 128th display period.
---	---	Display period in which OUTn turn-on time increases by GS data, increasing as does above operation
65534	FFFEh	Turns on during 512 GSCLK period in first through 63rd and 65th through 127th display period, and turns on 511 GSCLK period in 64th and 128th display periods.
65535	FFFFh	Turns on during 512 GSCLK period in first through 127th display periods, and turns on 511 GSCLK period in 128th display period only.

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Constant Current Driver ON/OFF Tming in ES-PWM

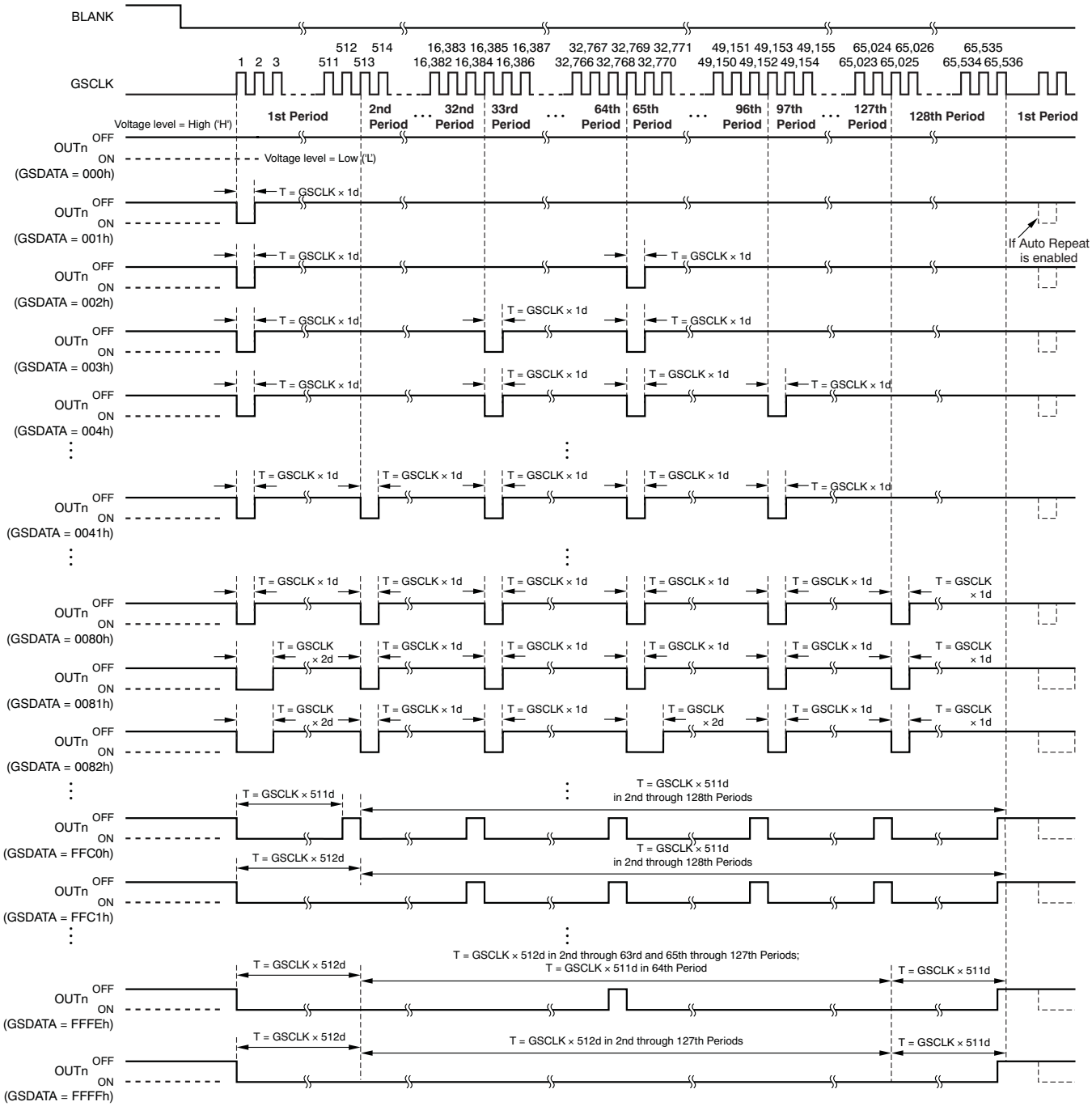

Figure 23. PWM Operation Timing

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When the IC powers on, the data in the Grayscale Shift Register and latch 1/2 are not set to any default value. Therefore, grayscale data must be written to the Grayscale latch before turning on the constant current output. Additionally, BLANK should be high when the device turns on, to prevent the outputs from turning on before the proper grayscale and brightness control values can be written. All constant current outputs are always off when BLANK is high. Equation 3 determines each output (OUTn) total on time (t_{OUTON}):

$$t_{OUTON}\ (ns) = T_{GSCLK}\ (ns) \times GSn \quad (3)$$

Where:

- T_{GSCLK} = the period of GSCLK
- GSn = the programmed grayscale value for OUTn (GSn = 0 to 65,535d)

Table 4 summarizes the GS data versus OUTn on duty and on time.

Table 4. GS Data versus OUTn Total On Duty

GS DATA (Decimal)	GS DATA (Hex)	ON-TIME DUTY (%)	GS DATA (Decimal)	GS DATA (Hex)	ON-TIME DUTY (%)
0	0	0	32768	8000	50.001
1	1	0.002	32769	8001	50.002
2	2	0.003	32770	8002	50.004
3	3	0.005	32771	8003	50.005
---	---	---	---	---	---
8191	1FFF	12.499	40959	9FFF	62.499
8192	2000	12.5	40960	A000	62.501
8193	2001	12.502	40961	A001	62.502
---	---	---	---	---	---
16381	3FFD	24.996	49149	BFFD	74.997
16382	3FFE	24.997	49150	C000	74.998
16383	3FFF	24.999	49151	C001	75
16384	4000	25	49152	C002	75.001
16385	4001	25.002	49153	C003	75.003
16386	4002	25.003	49154	C004	75.004
16387	4003	25.005	49155	C005	75.006
---	---	---	---	---	---
24575	5FFF	37.499	57343	DFFF	87.5
24576	6000	37.501	57344	E000	87.501
24577	6001	37.502	57345	E001	87.503
---		---	---		---
32765	7FFD	49.996	65533	FFFD	99.997
32766	7FFE	49.998	65534	FFFE	99.998
32767	7FFF	49.999	65535	FFFF	100

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Auto Display Repeat Function

This function can repeat the total display period without a BLANK signal as long as GSCLK is input as Figure 24 shows. This function can be switched on or off by the data of bit 7 in the first latch of the Brightness Control. When bit 7 is '1', Auto Repeat is enabled and the entire display period repeats without a BLANK signal. When bit 7 is '0', Auto Repeat is disabled and the entire display period executes only one time after the falling edge of BLANK.

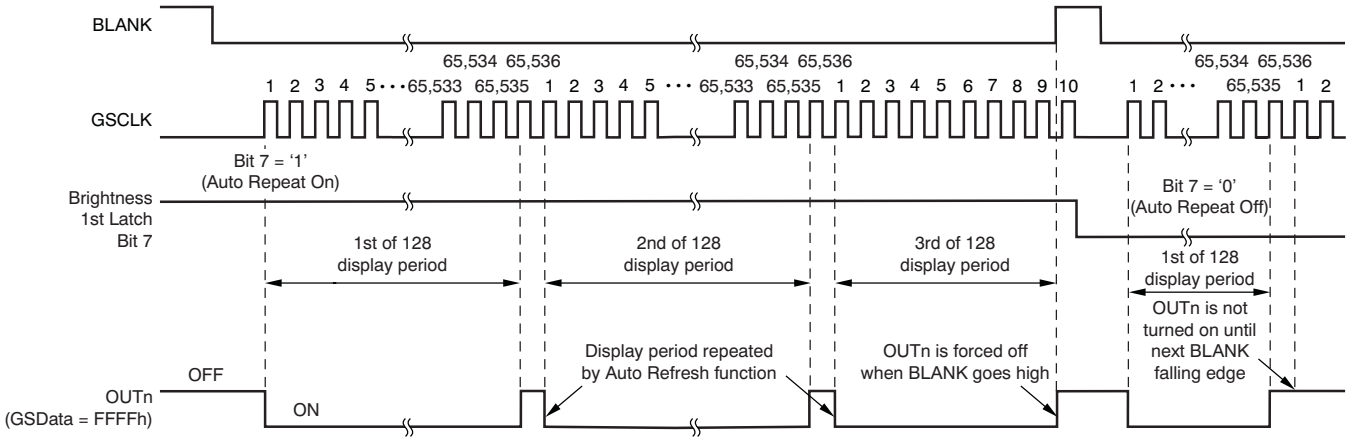

Figure 24. Auto Repeat Display Function Timing

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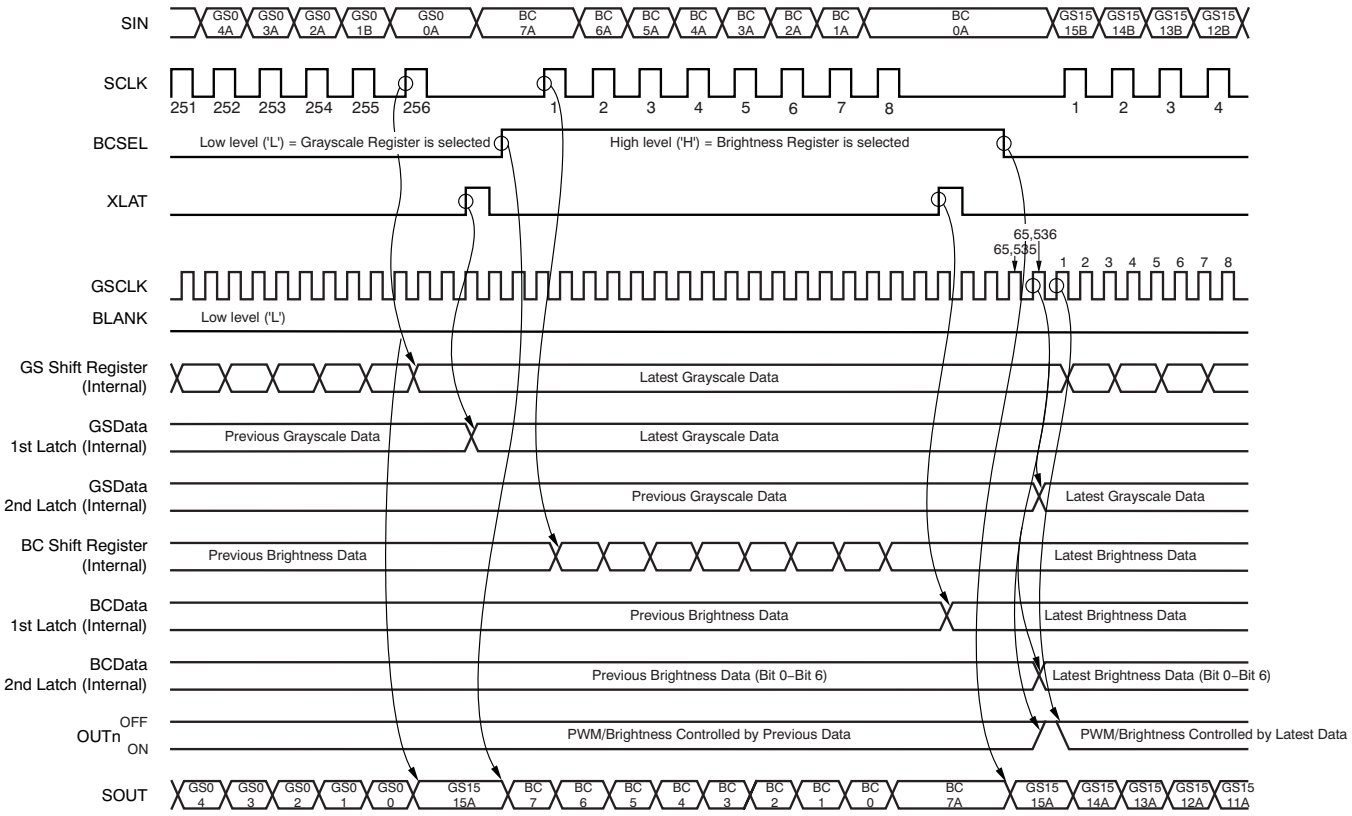
Auto Data Refresh Function

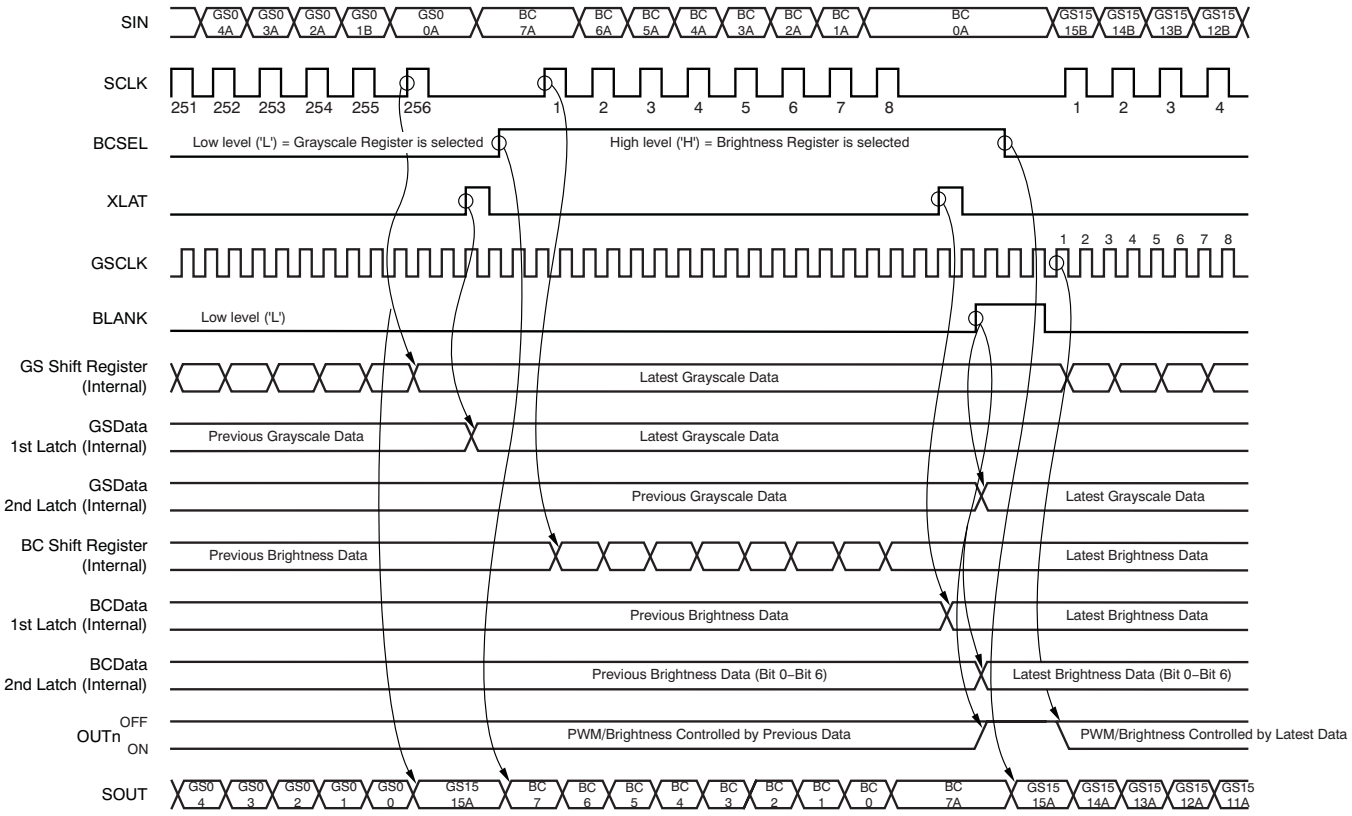
This function allows users to input Grayscale (GS) data or Brightness Control (BC) data any time without synchronizing the input to the BLANK signal. If GS data or BC data are input during a display period, the input data are held in the first latch for each data register. Data are then transferred to the second latch when the 65,536th GSCLK occurs. The second latch data are used for the next display period. Figure 25 through Figure 27 show the timing.

However, when the high level signal of BLANK occurs before the 65,536th GSCLK, then the first latch data upload to the second latch immediately. Also, when the XLAT rising edge inputs while BLANK is at a high level, then the selected shift register data are transferred to the first and second latch at the same time. Bit 7 data of BC update immediately whenever the data are written into the first latch.



If there is no BLANK input when Auto Repeat is enabled.

Figure 25. Auto Refresh Data Function Timing 1



When the BLANK input occurs after XLAT.

Figure 26. Auto Refresh Data Function Timing 2

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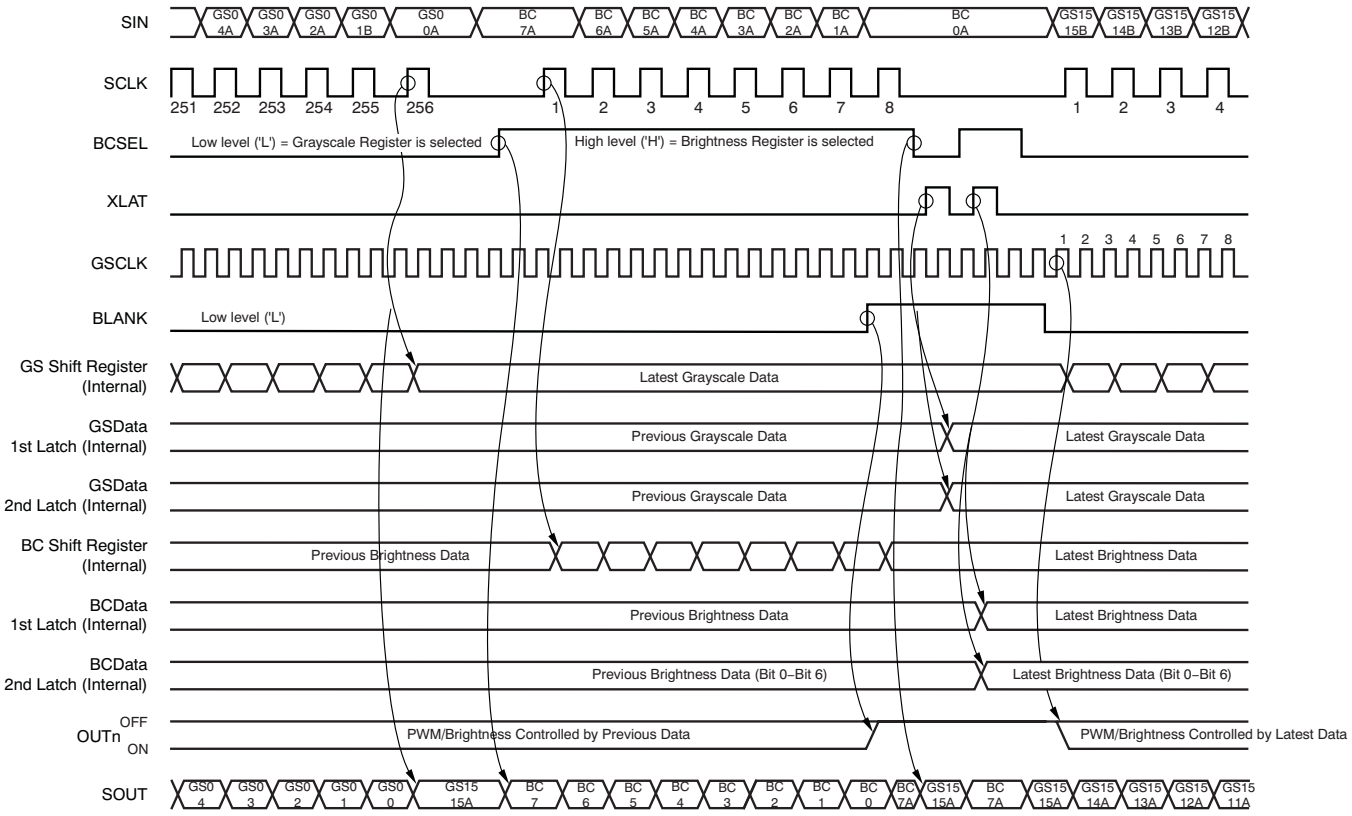

When the BLANK input occurs with XLAT.

Figure 27. Auto Refresh Data Function Timing 3

Grayscale (GS) Shift Register and Data Latch

The Grayscale (GS) Shift Register and data latch 1 and 2 are each 256 bits in length, and set the PWM timing for each constant current driver. See Table 4 for the ON time duty of each GS data bit. Figure 28 shows the shift register and latch configuration. Refer to Figure 11 for the timing diagram for writing data into the GS shift register and latch.

The driver on time is controlled by the data in the GS second data latch. GS data can be set into the latch by the rising edge of XLAT with BCSEL = low after writing data into the GS shift register with SIN and GSCLK with BCSEL = low. A BCSEL level change occurs during SCLK = low, and after 100 ns from the rising edge of XLAT. When the device powers up, the data in the GS shift register and latches are not set to any default value. Therefore, GS data must be written to the GS latch before turning on the constant current output. Also, BLANK should be at a high level when powering on the device, because the constant current may be turned on as well. All constant current output is off when BLANK is at a high level.

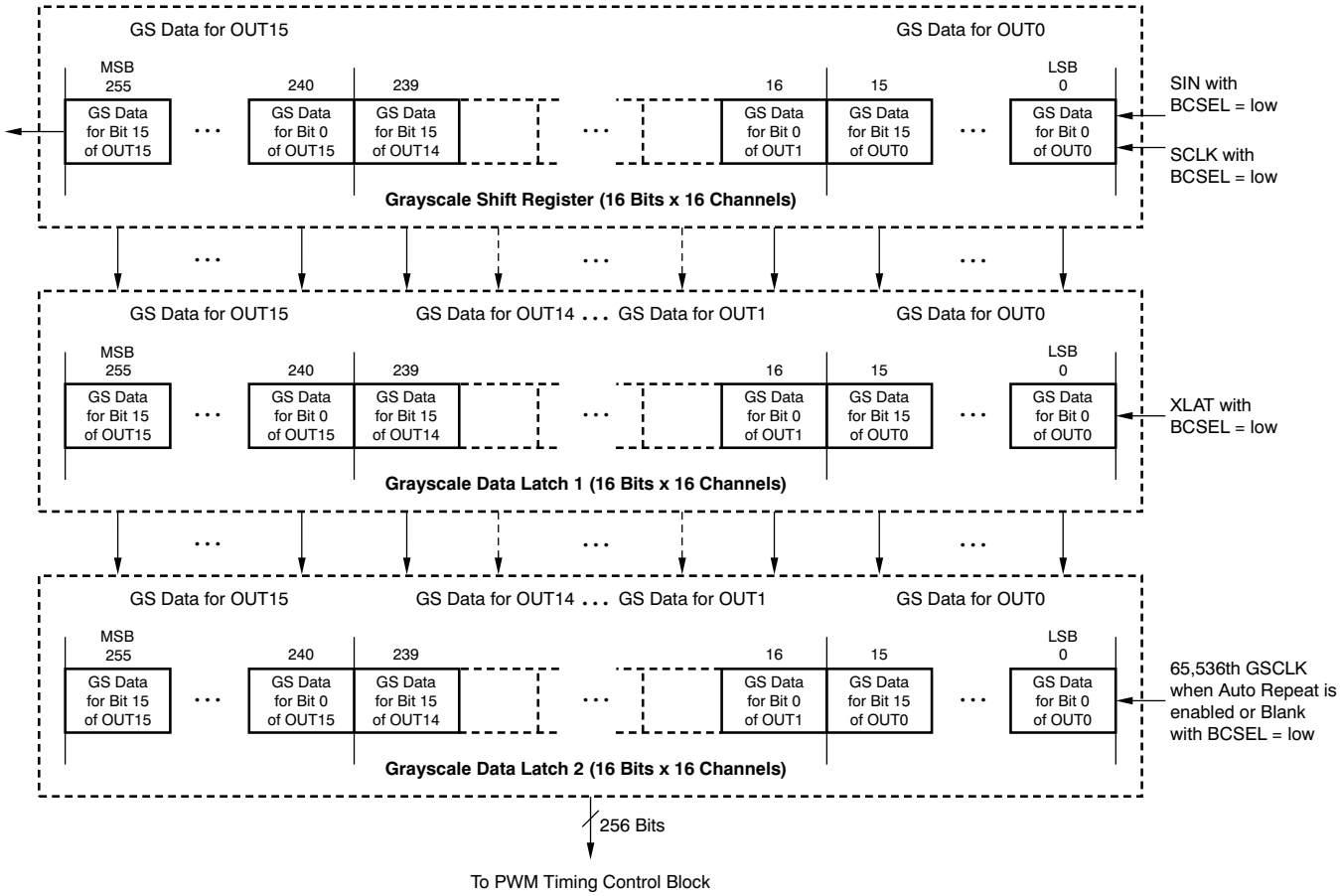

Figure 28. Grayscale Shift Register and Data Latch Configuration

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Brightness Control (BC) Shift Register and Data Latch

The Brightness Control (BC) data shift register and the first latch are each 8 bits long; the second latch is 7 bits long. The lower 7 bits in the latch are used to adjust the constant current value for all channels of the constant current driver. The MSB of the first latch is used for the auto repeat mode setting. Table 5 shows the ratio of setting the current value against the maximum current value for each BC data point. Figure 29 shows the shift register and latch configuration for BC data. Figure 12 shows the timing for writing data.

The driver constant current value is controlled by the data in the second BC data latch. BC data can be set into the latch at the rising edge of XLAT with BCSEL = high after writing the data into the BC Shift Register by SIN and SCLK with BCSEL = high. A BCSEL level change occurs during SCLK = low and after 100 ns from the rising edge of XLAT. When powered up, the data in the BC Shift Register and latches are not set to any default value. Therefore, brightness data must be written to the BC latch before turning on the constant current output.

Table 5. BC Data vs Current Ratio

BC Data (Dec)	BC Data (Lower 7 Bits; Hex)	Ratio of Setting Current Value Against MAX Value (%)
0	0	0
1	1	0.8
2	2	1.6
3	3	2.4
---	---	---
125	7D	98.4
126	7E	99.2
127	7F	100

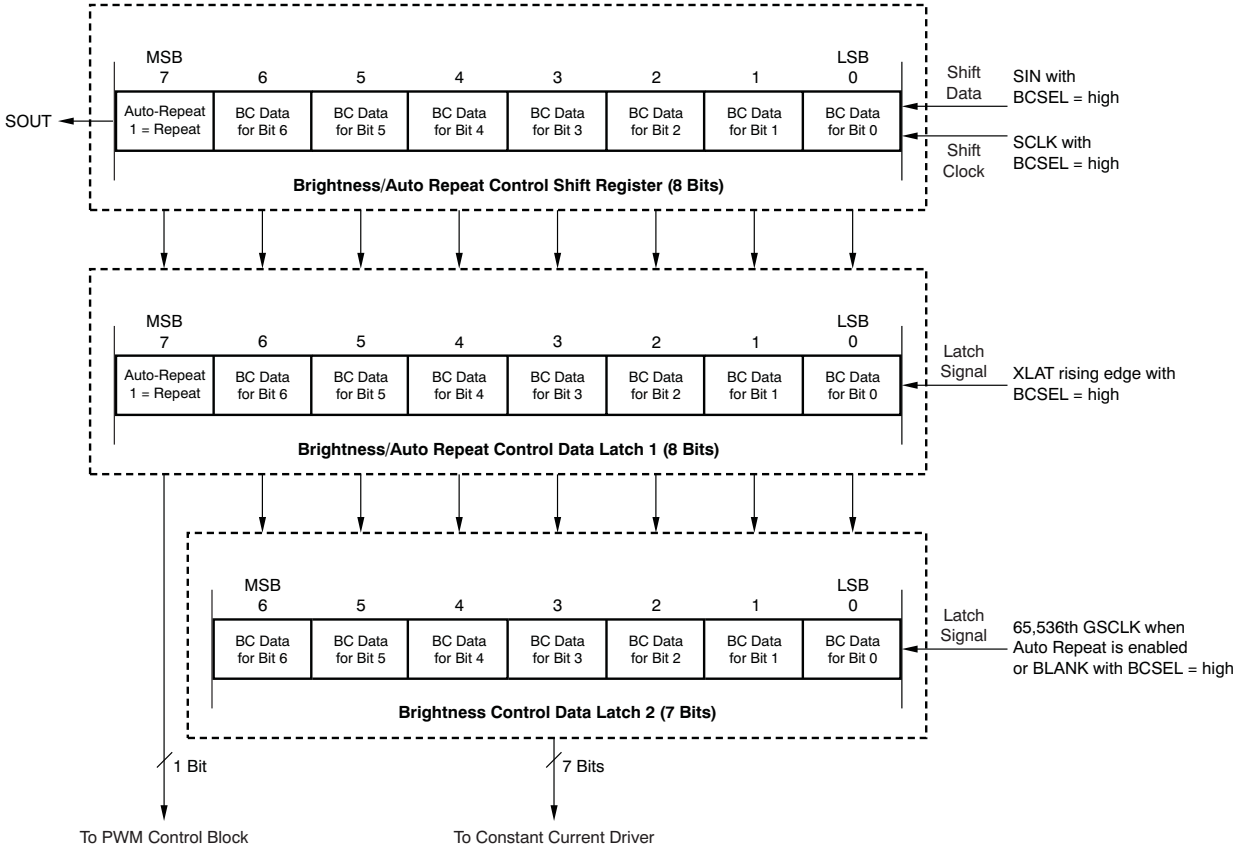

Figure 29. Brightness Control Shift Register and Latch Configuration

Status Information Data (SID)

Status information data (SID) are 17-bit, read-only data. Both the LED open detection (LOD) error and the thermal error flag (TEF) are shifted out onto the SOUT pin with each rising edge of the shift clock, SCLK. The 16 LOD bits for each channel and the TEF bit are written into the 17 most significant bits of the Grayscale Shift Register at the rising edge of the first SCLK after XLAT goes low. As a result, the previous data in the 17 most significant bits are lost at the same time. No data are loaded into the other 175 bits. Figure 30 shows the bit assignments. Figure 13 illustrates the read timing for the status information data.

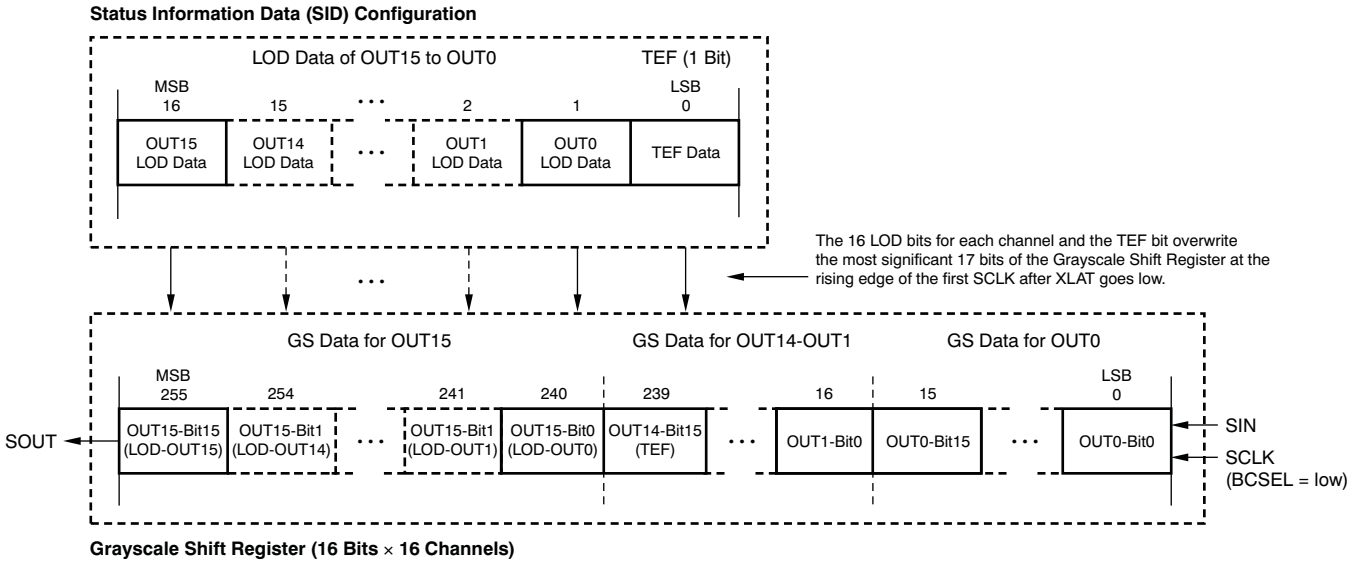

Figure 30. Status Information Data Configuration

The LOD data update at the rising edge of the 33rd GSCLK pulse after BLANK goes low; the LOD data are retained until the next 33rd GSCLK. LOD data are only checked for outputs that are turned on during the rising edge of the 33rd GSCLK pulse. A '1' in an LOD bit indicates an open LED or short LED to GND condition for the corresponding channel. A '0' indicates normal operation. LOD shows a '0' even if the LED is open or shorted to GND when the grayscale data are less than 1000h (4096d). Therefore, grayscale data must be greater than 1001h (4097d) to correctly receive LOD data.

The TEF bit indicates that the IC temperature is too high. The flag also indicates that the IC has turned off all drivers to avoid damage by overheating the device. A '1' in the TEF bit means that the IC temperature has exceeded the detect temperature threshold ($T_{(TEF)}$) and the driver is turned off. A '0' in the TEF bit indicates normal operating temperature conditions. The IC automatically turns the drivers back on when the IC temperature decreases to less than $T_{(TEF)} - T_{(HYS)}$. When the IC powers on, LOD data do not show correct values. Therefore, LOD data must be read from the 33rd GSCLK pulse input after BLANK goes low. Table 6 shows a truth table for both LOD and TEF.

Table 6. LOD and TEF Truth Table

SID DATA	CONDITION	
	LED OPEN DETECTION (LODn)	THERMAL ERROR FLAG (TEF)
0	LED is connected ($V_{OUTn} > V_{LOD}$)	Device temperature is low (temp ≤ $T_{(TEF)} - T_{(HYS)}$)
1	LED is open or shorted to GND ($V_{OUTn} \le V_{LOD}$)	Device temperature is high (temp > $T_{(TEF)}$)

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Noise Reduction

Large surge currents may flow through the IC and the printed circuit board (PCB) on which the device is mounted if all 16 LED channels turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5943 turns on the LED channels in a series delay to provide a circuit soft-start feature. The output current sinks are grouped into four groups of four channels each. The first group is OUT0,4,8,12; the second group is OUT1,5,9,13; the third group is OUT2,6,10,14; and the fourth group is OUT3,7,11,15. Each group is turns on sequentially with a small delay between groups; see Figure 11. Both turn-on and turn-off are delayed.

Continuous Base LED Open Detection

When the 33rd GSCLK goes high in the first display period after a BLANK falling edge, the LED open detection (LOD) circuit checks the voltage of each constant current output (OUT0 through OUT15 = OUTn) that is turned on to detect open LEDs and short LEDs to GND. Then, if the voltage of OUTn is less than the LED open detection threshold (V_{LOD} = 0.3 V_{TYP}), it sets '1' as the error flag to the LOD error bit that corresponds with the error channel in the Status Information Data (SID) register. Also, the XERR pin level moves from Hi-Z at the same time. As a result, GS data should be over 1001h (4097d) to get the LOD result. The OUTn channel that has the detected LOD error is forced off to avoid an increase in the V_{CC} supply current. OUTn turns on at the first GSCLK after a BLANK falling edge again. LOD data are kept until the next 33rd rising edge of GSCLK in the first display period after a BLANK falling edge. LOD is always '0' when grayscale data are less than 1001h (4097d). XERR is forced to a Hi-Z state while BLANK is high. When powered up, LOD data are not set to any default value. Therefore, SID data must be used after OUTn turns on with over 1001h GS data. Figure 31 shows the LED Open Detection timing.

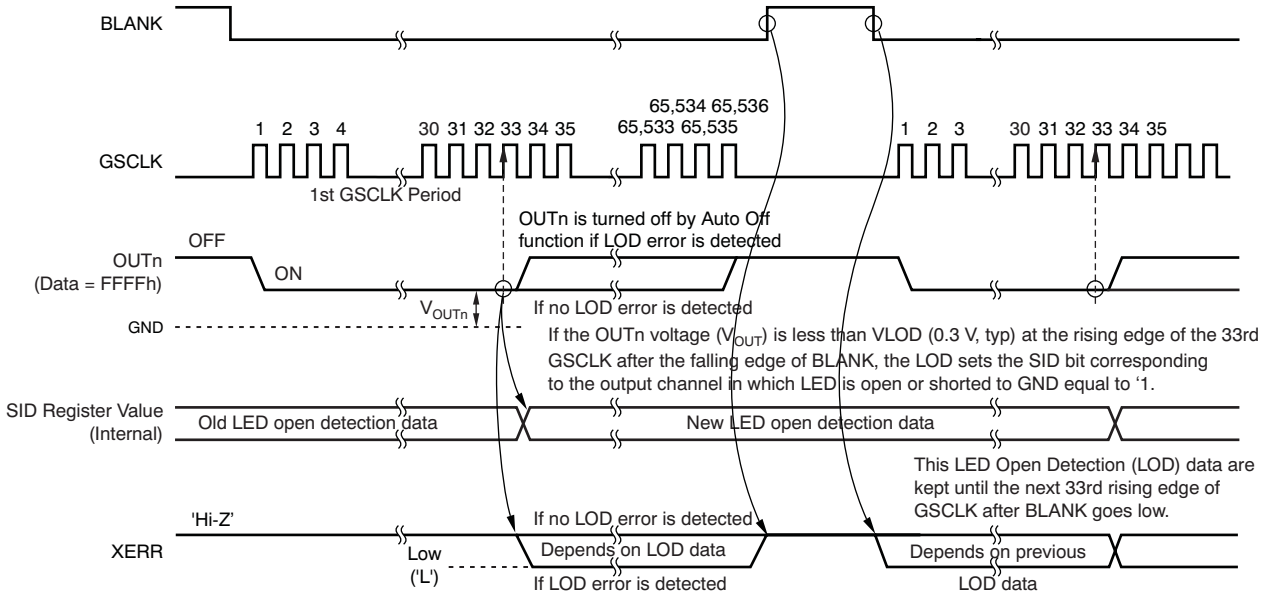

Figure 31. LED Open Detection (LOD) Timing

Auto Output Off

If the active OUTn channel is not connected to an LED or if LED is shorted to GND, then V_{CC} consumption current increases. In order to avoid this event, the device has an auto output off function. This function turns off channel OUTn with a detected LED opening or LED shorting to GND at the 33rd GSCLK after BLANK goes low automatically. V_{CC} current can be saved by this function. OUTn is controlled normally again after BLANK goes low. Figure 32 illustrates the auto output off function.

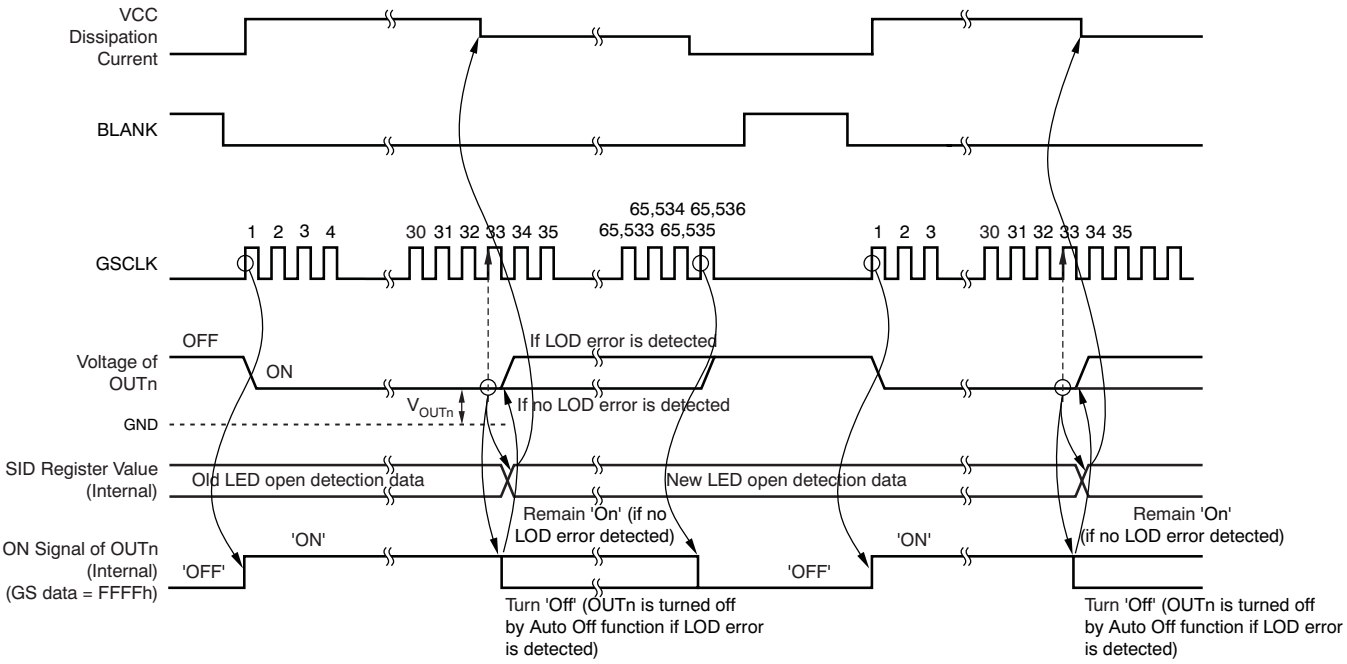

Figure 32. Auto Output Off Function

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Thermal Shutdown and Thermal Error Flag

The Thermal Shutdown (TSD) function turns off all of the constant current outputs on the IC immediately when the junction temperature (T_J) exceeds the threshold ($T_{(TEF)}$ = +162°C, typ) and sets the thermal error flag (TEF) to '1'. The XERR pin goes low at the same time. The XERR pin level and the TEF level are kept until the first SCLK falling edge after an XLAT falling edge of grayscale data. Then if T_J is still greater than $T_{(TEF)}$, TEF continues at '1' while XERR remains low. If T_J becomes less than $T_{(TEF)} - T_{(HYS)}$, TEF is set to '0' and XERR becomes Hi-Z. XERR is not forced to a Hi-Z state while BLANK is high. Therefore, the error type TEF or LOD can be distinguished from the BLANK signal control. OUTn is turned on at the first GSCLK after the BLANK falling edge if T_J becomes less than $T_{(TEF)} - T_{(HYS)}$ at the BLANK rising edge.

When the IC powers on, TEF may be set and all output is forced off. Therefore, an XLAT pulse and a BLANK rising edge should be input once to turn on the output. Figure 33 illustrates the TEF/TSD/XERR timing sequence.

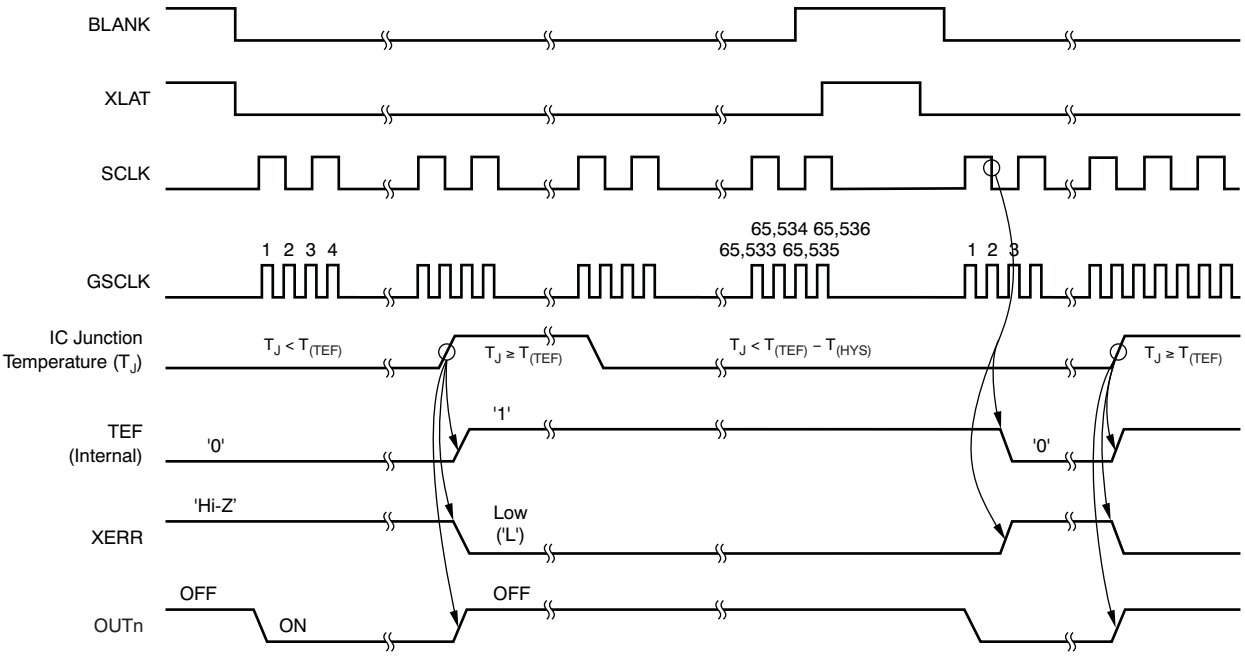

Figure 33. TEF/TSD/XERR timing

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package (illustrated in Figure 15) to ensure correct operation. Equation 4 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{BCn}{127d} \times d_{PWM} \right) \quad (4)$$

Where:

- V_{CC} = device supply voltage
- I_{CC} = device supply current
- V_{OUT} = OUTn voltage when driving LED current
- I_{MAX} = LED current adjusted by $R_{(IREF)}$ resistor
- BCn = maximum BC value for OUTn
- N = number of OUTn driving LED at the same time
- d_{PWM} = duty ratio defined by BLANK pin or GS PWM value

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5943PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943PWP.B	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5943
TLC5943RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943
TLC5943RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943
TLC5943RHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943
TLC5943RHBRG4.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943
TLC5943RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943
TLC5943RHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5943

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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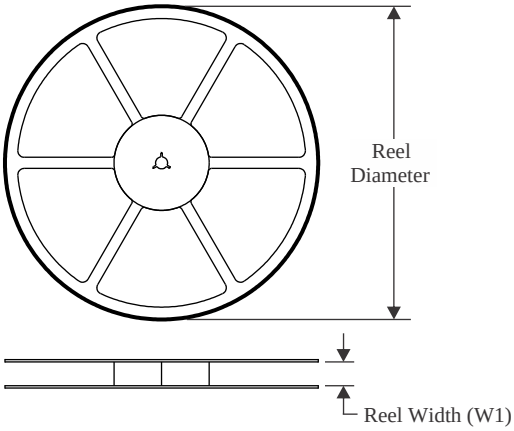
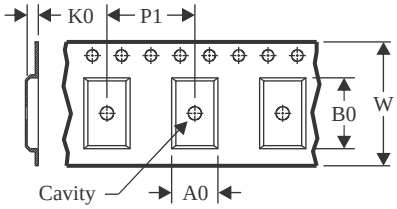
TAPE AND REEL INFORMATION

REEL DIMENSIONS

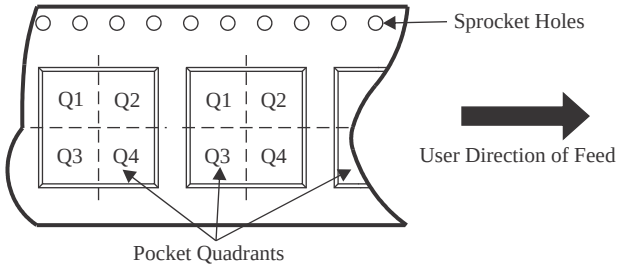


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

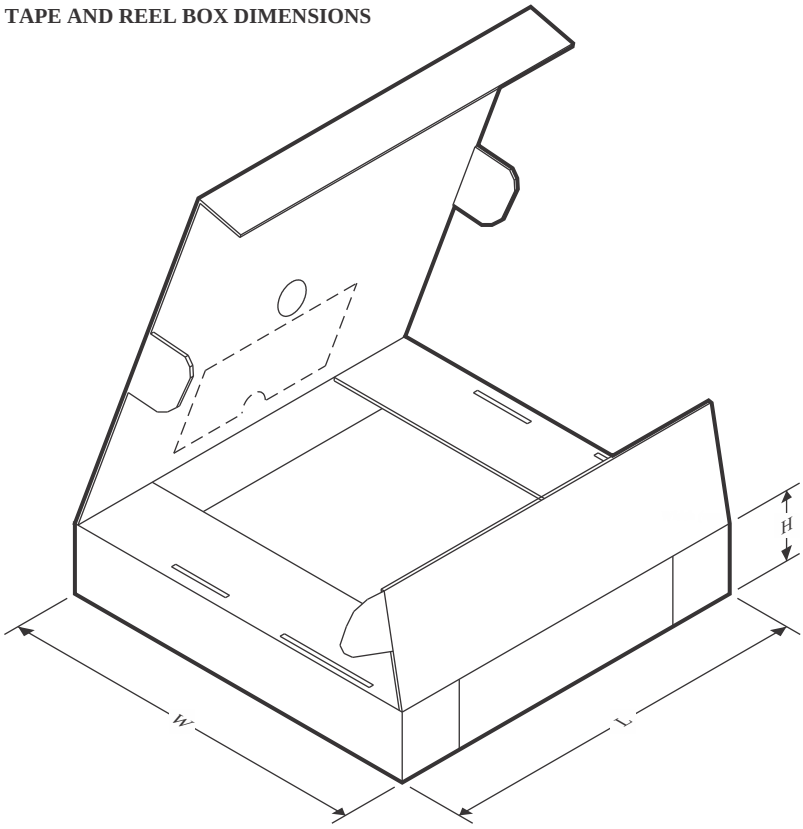
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5943PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TLC5943RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5943RHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC5943RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

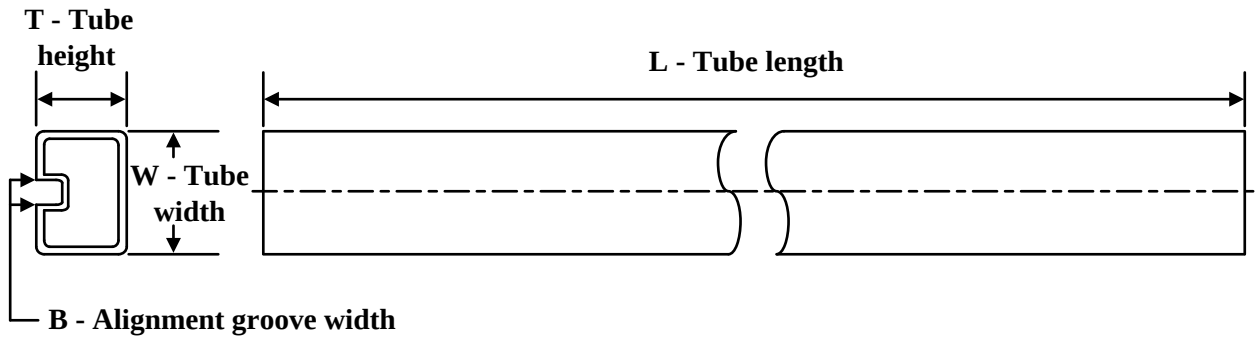
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5943PWPR	HTSSOP	PWP	28	2000	353.0	353.0	32.0
TLC5943RHBR	VQFN	RHB	32	3000	353.0	353.0	32.0
TLC5943RHBRG4	VQFN	RHB	32	3000	353.0	353.0	32.0
TLC5943RHBT	VQFN	RHB	32	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5943PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TLC5943PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TLC5943PWP.B	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

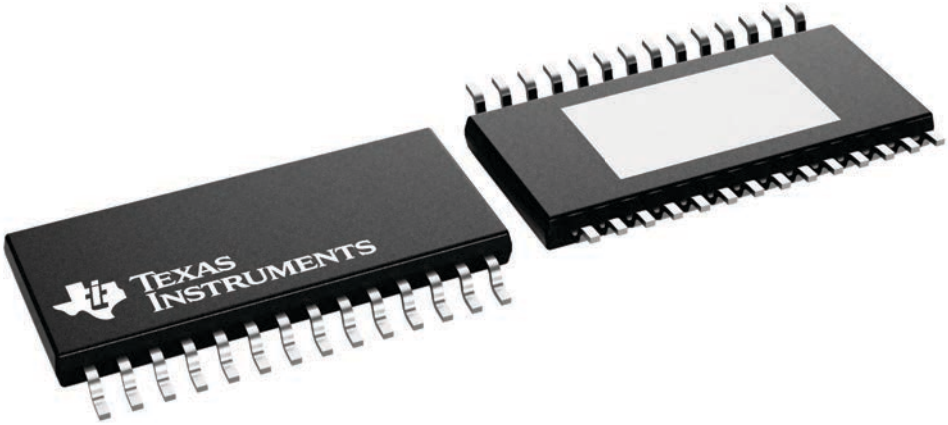
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

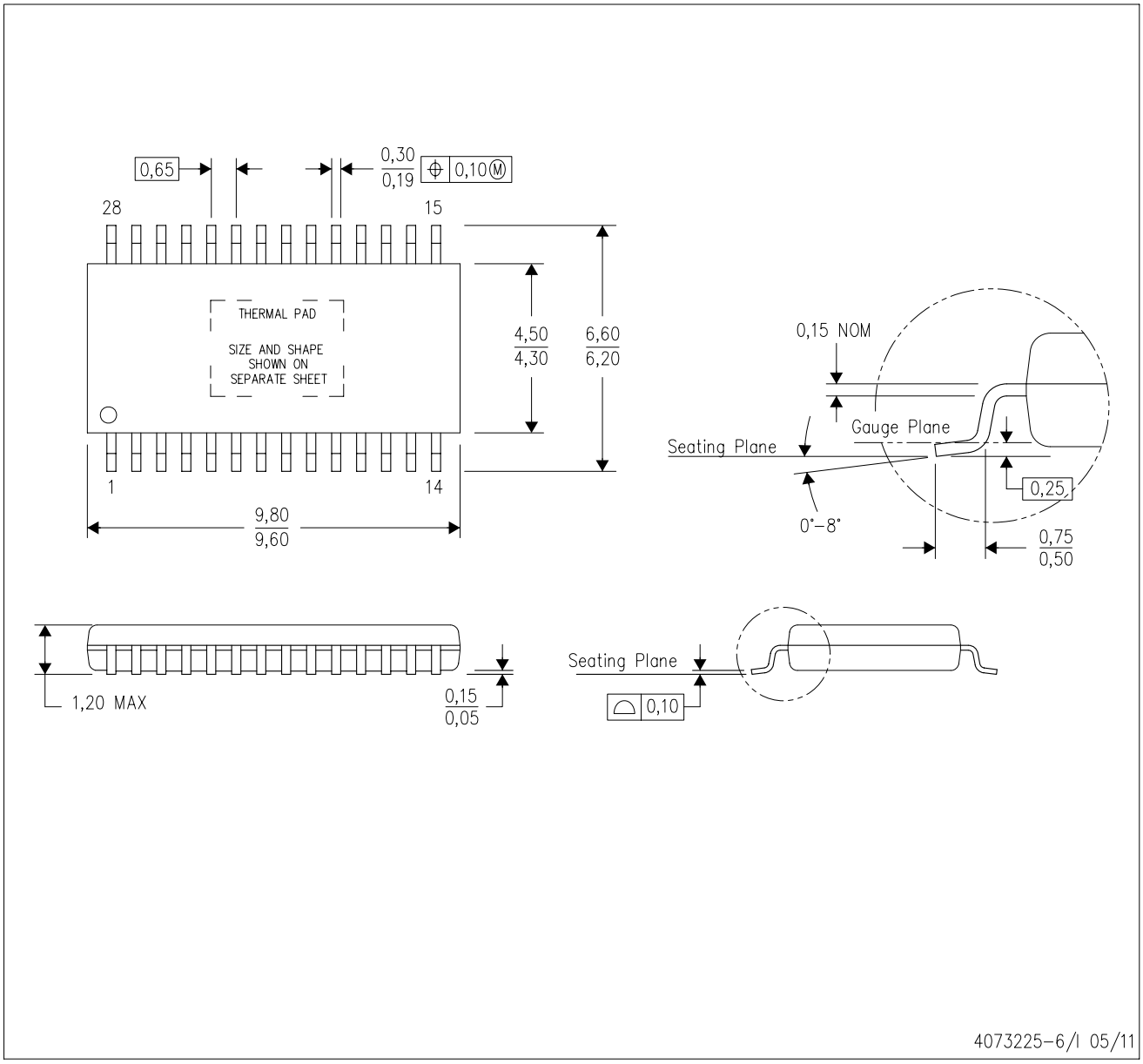
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

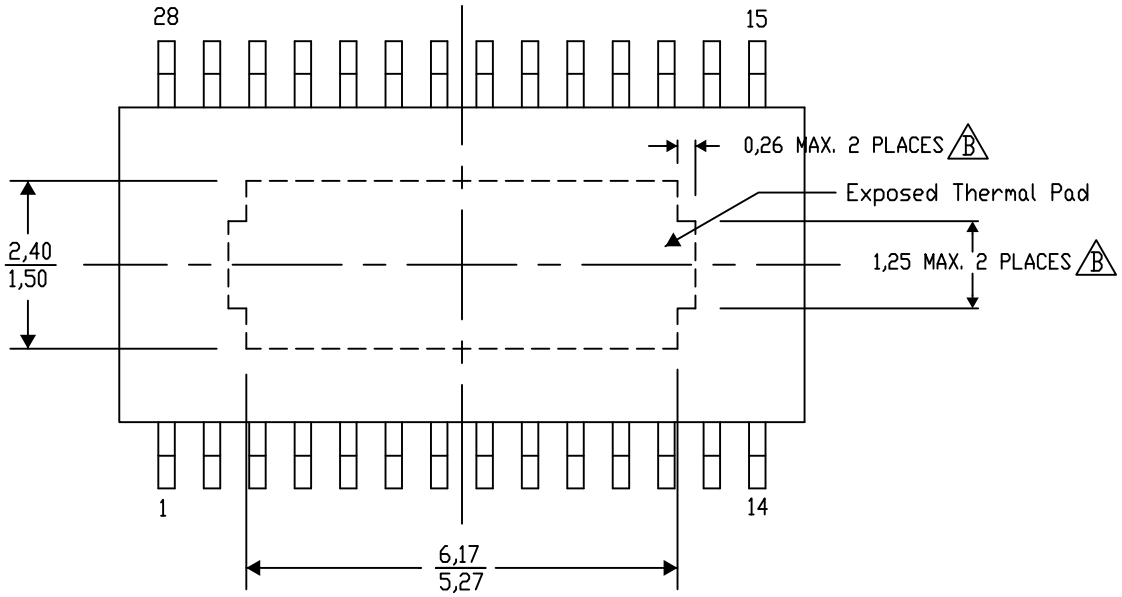
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

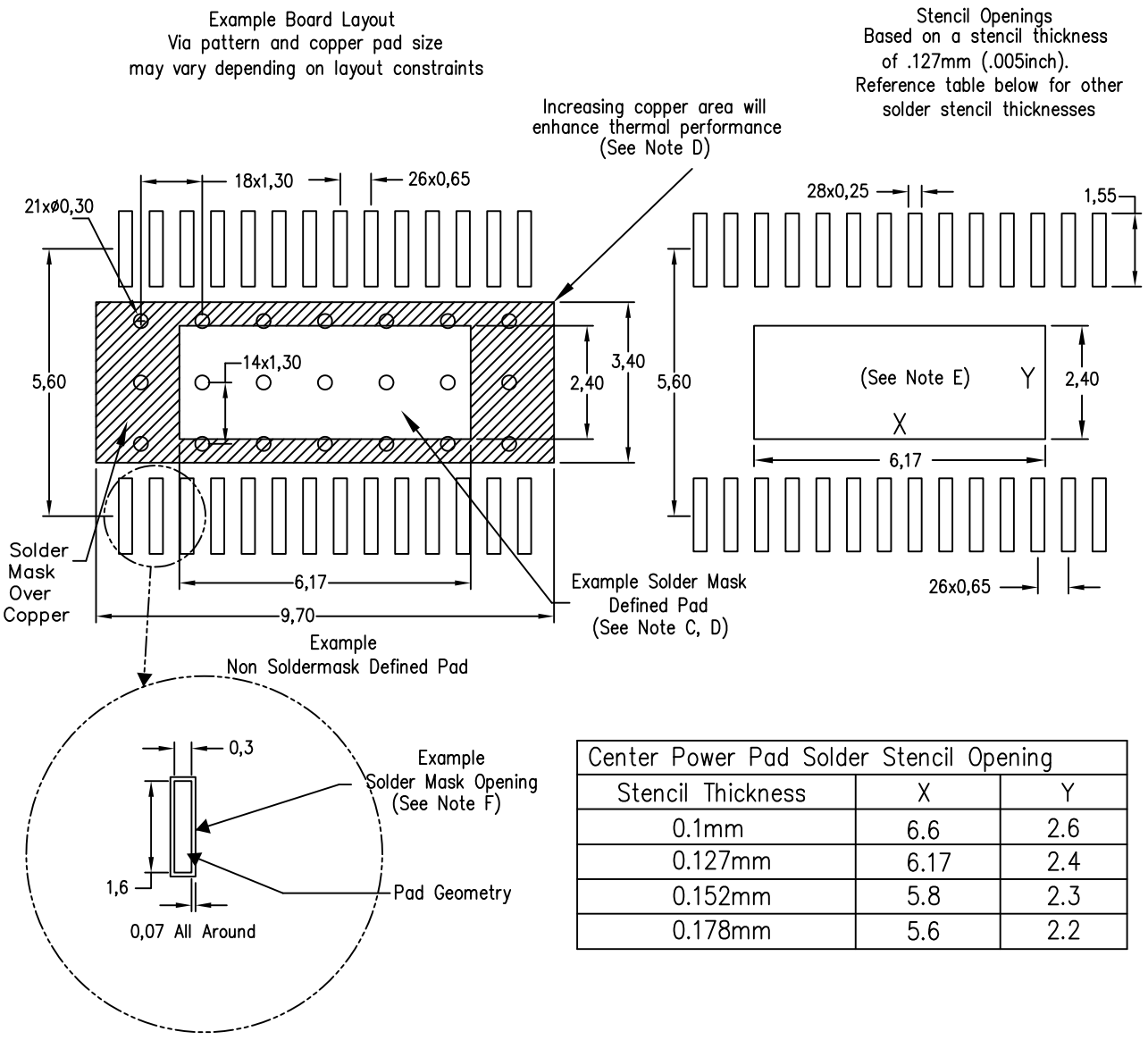
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

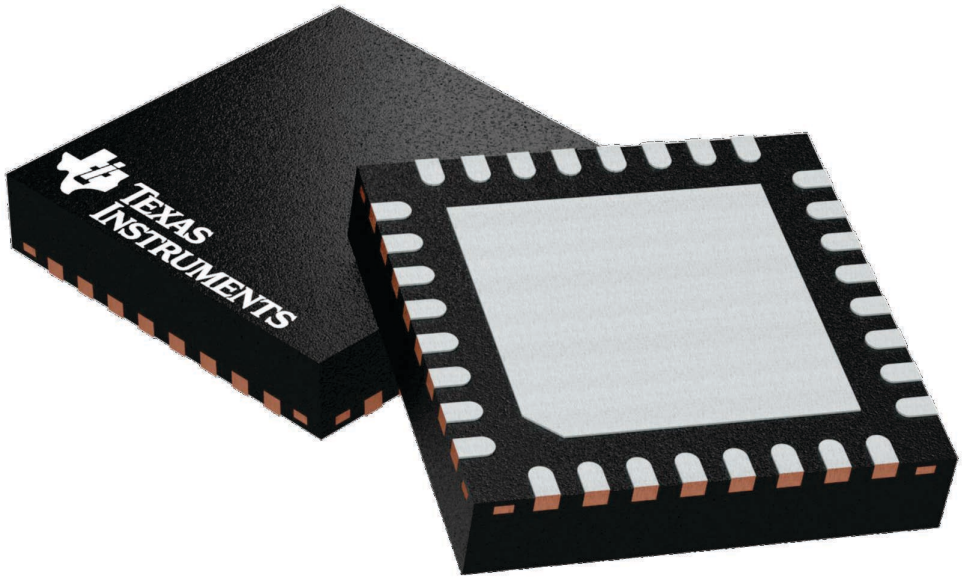
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

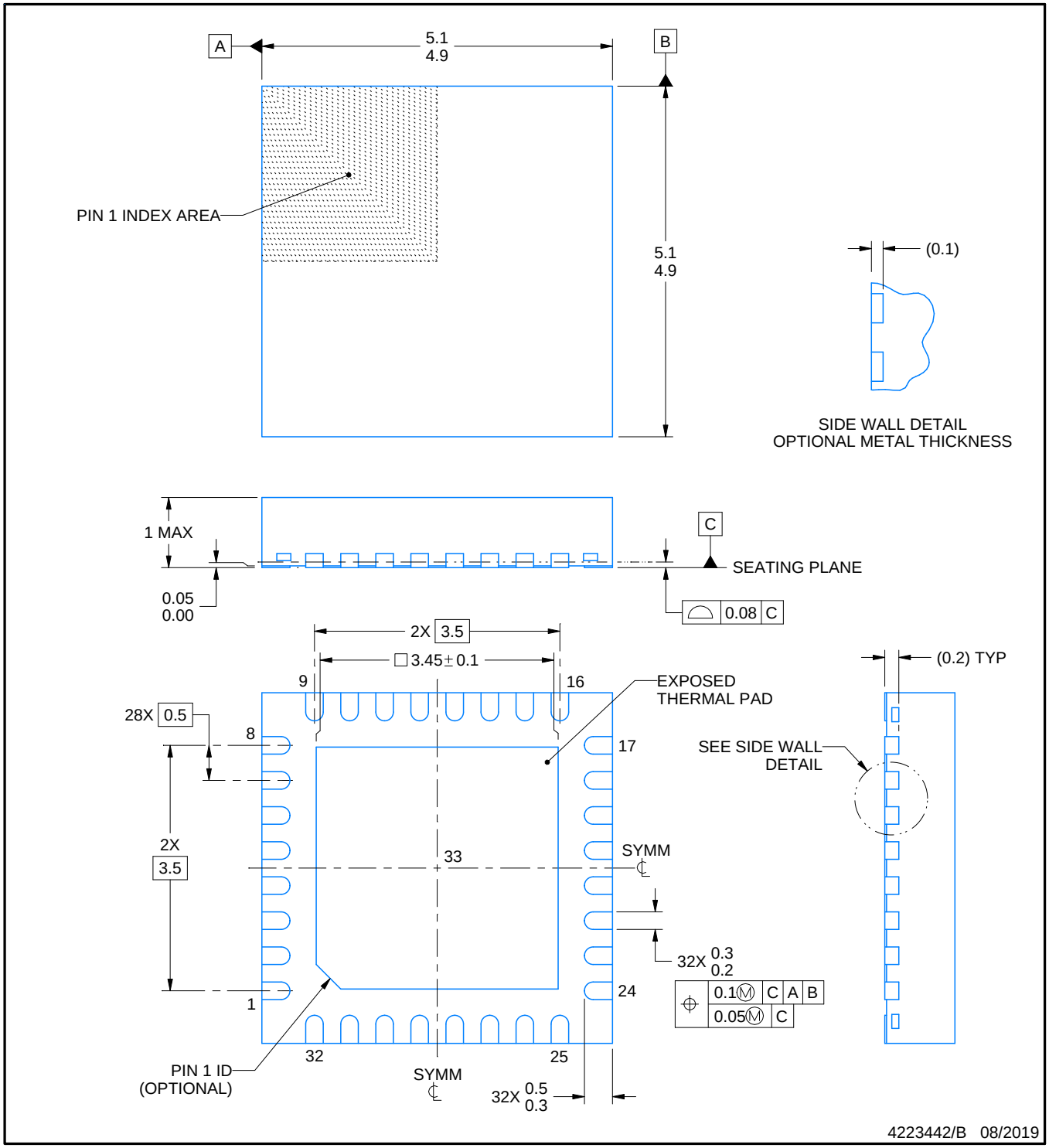
4224745/A

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

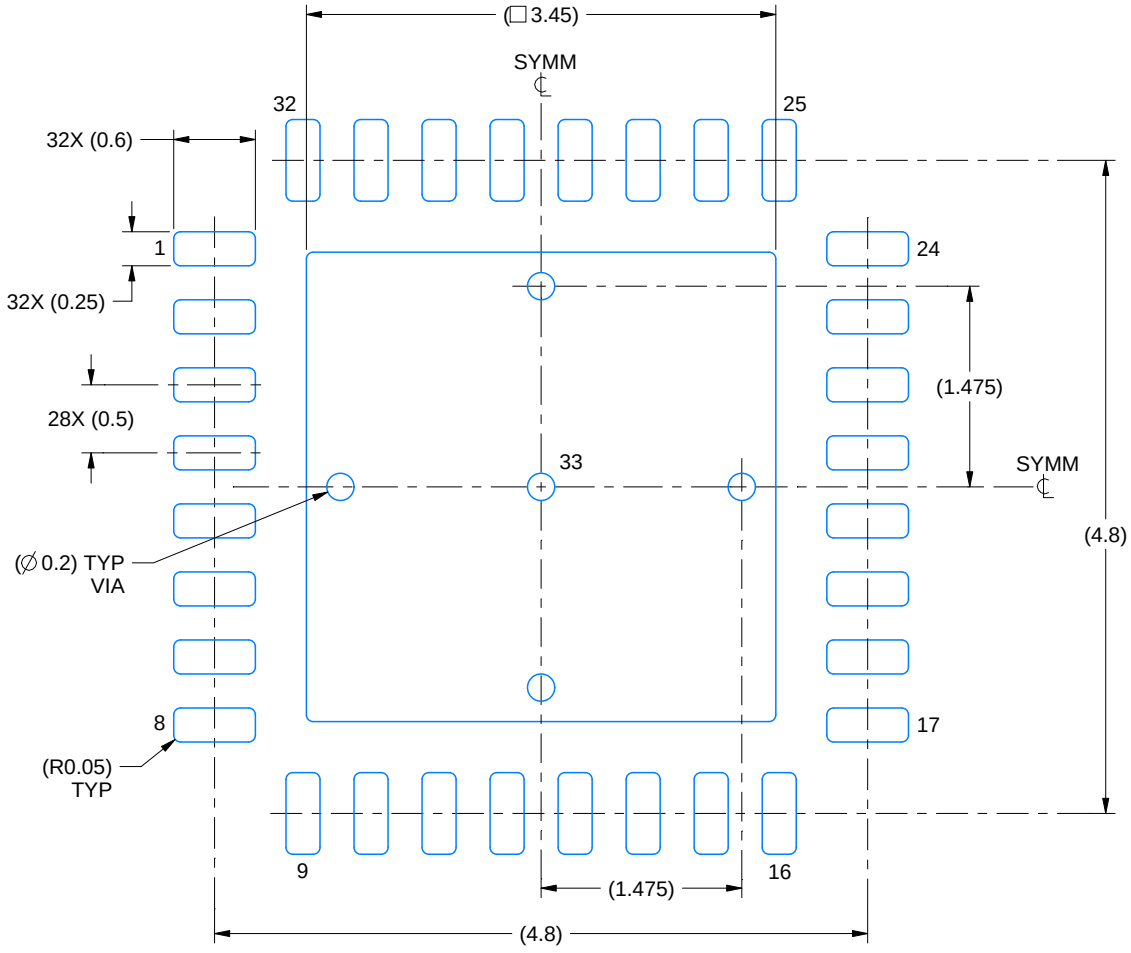
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

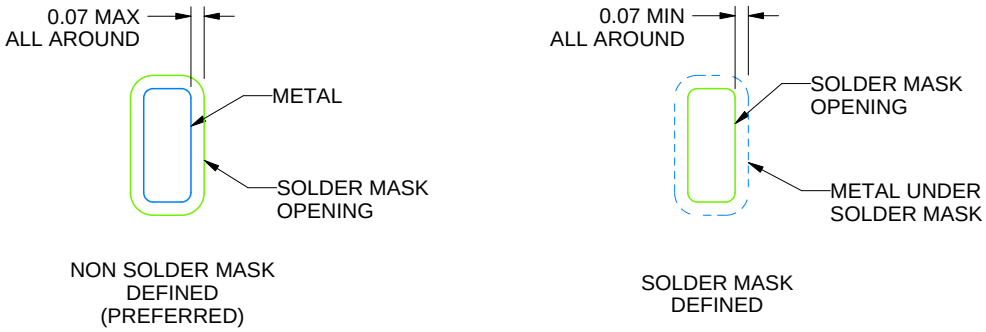
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X

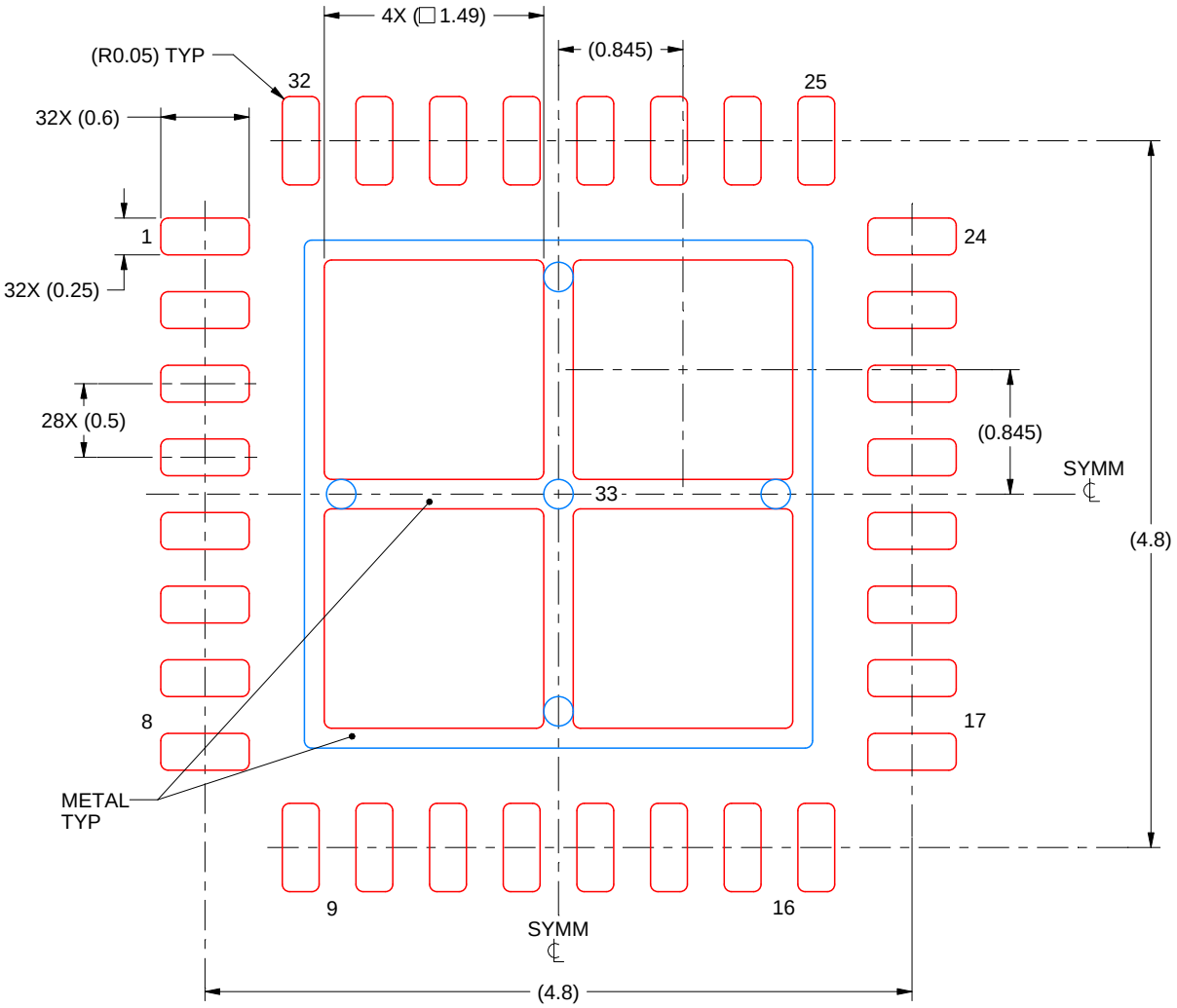


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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