

Dual N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Dual N-channel Devices – 2V Maximum Low Threshold
- High Input Impedance – 125 pF Maximum Low Input Capacitance
- Fast Switching Speeds
- Low On-resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-level Interfaces (Ideal for TTL and CMOS)
- Solid-state Relays
- Battery-operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

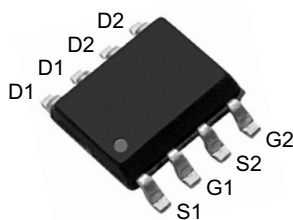
General Description

The TD9944 is a low-threshold Enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors as well as the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

8-lead SOIC
(Top view)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = 25^{\circ}C$. (Note 1)						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	240	—	—	V	$V_{GS} = 0V, I_D = 2\text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	0.6	—	2	V	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	-5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$ (Note 2)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	$V_{GS} = 0V, V_{DS} = \text{Maximum rating}$
		—	—	1	mA	$V_{DS} = 0.8\text{ Maximum rating}, V_{GS} = 0V, T_A = 125^{\circ}C$ (Note 2)
On-State Drain Current	$I_{D(ON)}$	0.5	1.9	—	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		1	2.8	—		$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	4	6	Ω	$V_{GS} = 4.5V, I_D = 250\text{ mA}$
		—	4	6		$V_{GS} = 10V, I_D = 0.5A$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.4	%/ $^{\circ}C$	$V_{GS} = 10V, I_D = 0.5A$ (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at $+25^{\circ}C$. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T _A = 25°C. (Note 2)						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G _{FS}	300	600	—	mmho	V _{DS} = 20V, I _D = 0.5A
Input Capacitance	C _{ISS}	—	65	125	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C _{OSS}	—	35	70	pF	
Reverse Transfer Capacitance	C _{RSS}	—	10	25	pF	
Turn-on Delay Time	t _{d(ON)}	—	—	10	ns	V _{DD} = 25V, I _D = 1A, R _{GEN} = 25Ω
Rise Time	t _r	—	—	10	ns	
Turn-off Delay Time	t _{d(OFF)}	—	—	20	ns	
Fall Time	t _f	—	—	20	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	—	1.8	V	V _{GS} = 0V, I _{SD} = 1A (Note 1)
Reverse Recovery Time	t _{rr}	—	300	—	ns	V _{GS} = 0V, I _{SD} = 1A

Note 1: Unless otherwise stated, all DC parameters are 100% tested at $+25^\circ\text{C}$. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, for all specifications $T_A = T_J = +25^\circ\text{C}$.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC	θ_{JA}	—	133	—	$^\circ\text{C/W}$	

Note 1: Mounted on an FR5 board 25 mm x 25 mm x 1.57 mm.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

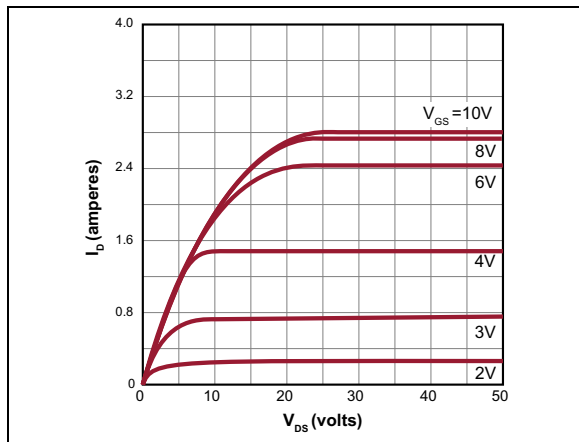


FIGURE 2-1: Output Characteristics.

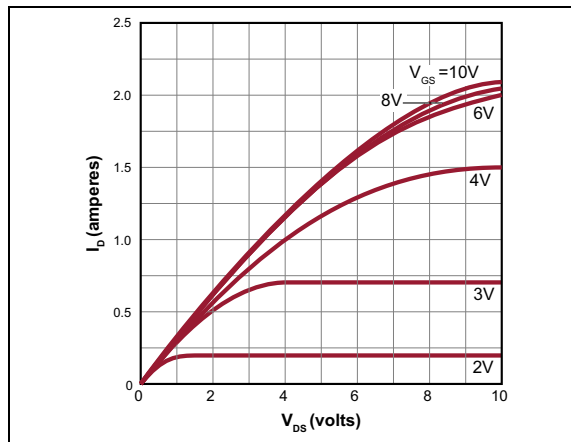


FIGURE 2-4: Saturation Characteristics.

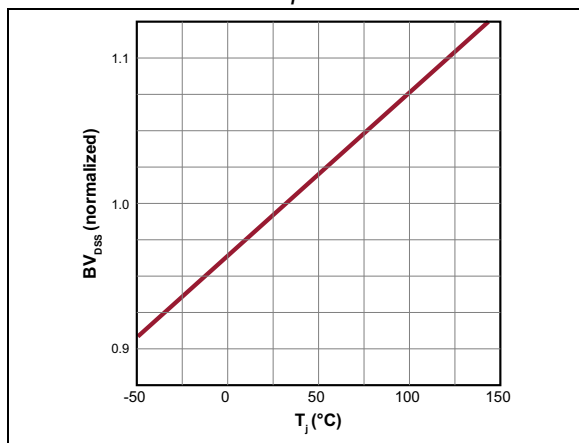


FIGURE 2-2: BV_{DS} Variation with Temperature.

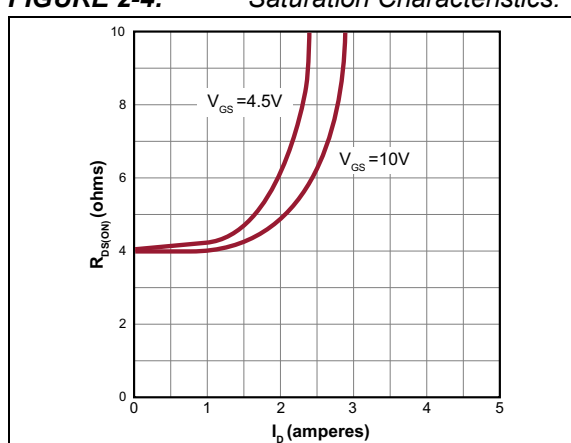


FIGURE 2-5: On-Resistance vs. Drain Current.

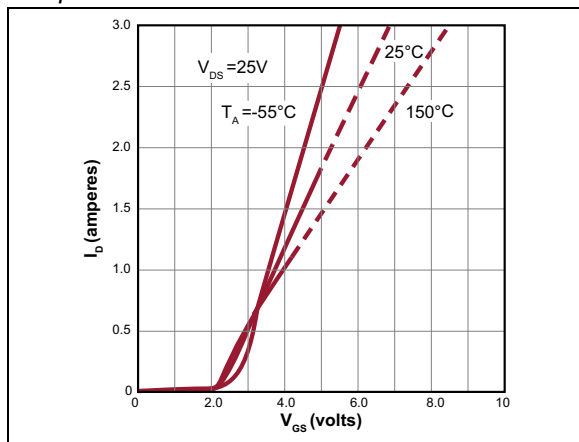


FIGURE 2-3: Transfer Characteristics.

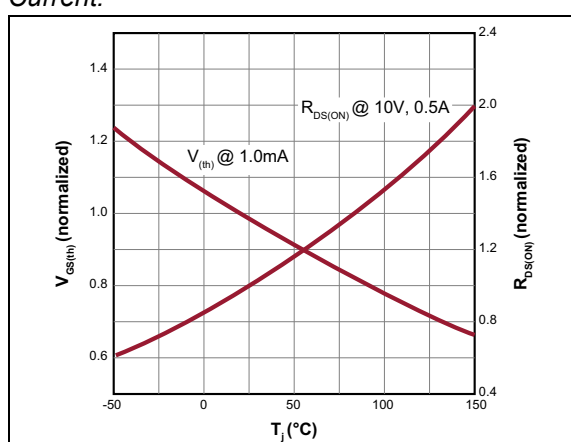


FIGURE 2-6: V_{th} and R_{DS} Variation with Temperature.

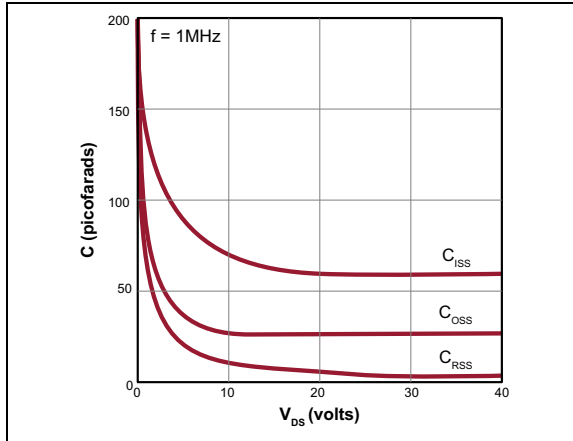


FIGURE 2-7: Capacitance vs. Drain-to-source Voltage.

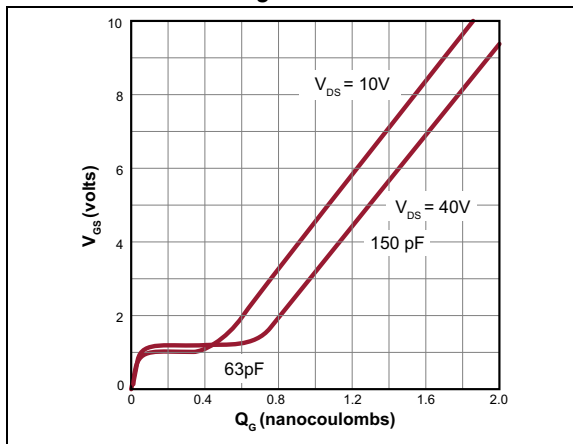


FIGURE 2-8: Gate Drive Dynamic Characteristics.

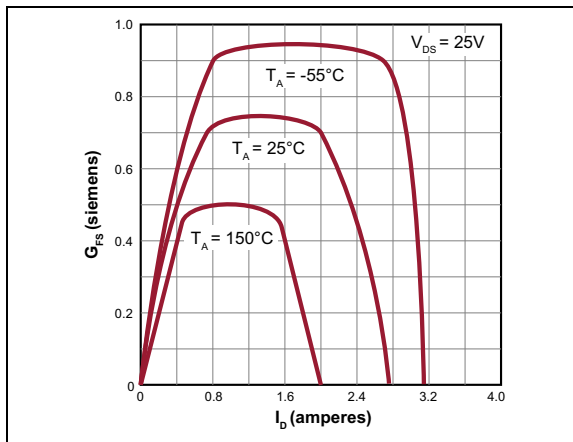


FIGURE 2-9: Transconductance vs. Drain Current.

3.0 PIN DESCRIPTION

Table 3-1 shows the description of pins in TD9944.
Refer to [Package Type](#) for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	S1	Source N-Channel 1
2	G1	Gate N-Channel 1
3	S2	Source N-Channel 2
4	G2	Gate N-Channel 2
5	D2	Drain N-Channel 2
6	D2	Drain N-Channel 2
7	D1	Drain N-Channel 1
8	D1	Drain N-Channel 1

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TD9944.

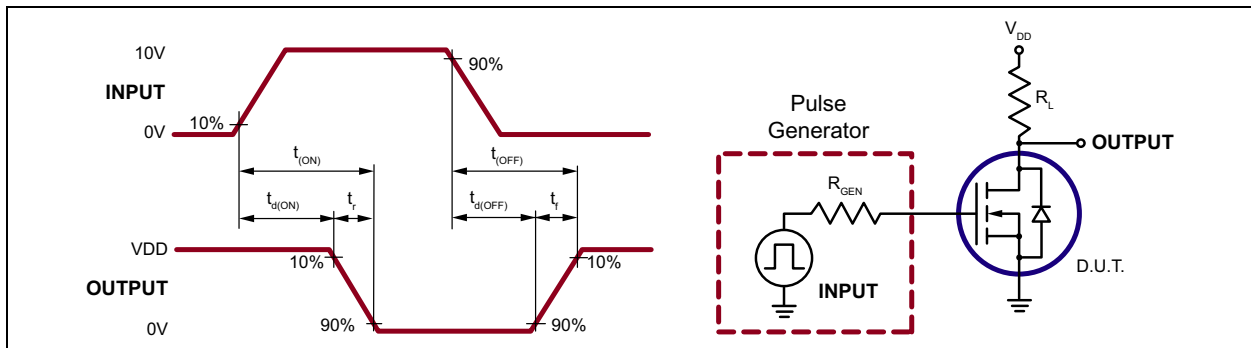


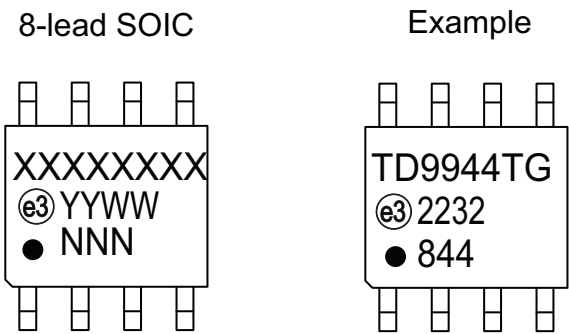
FIGURE 4-1: Switching Waveforms and Test Circuit.

TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (A)	$V_{GS(th)}$ (Maximum) (V)
240	6	1	2

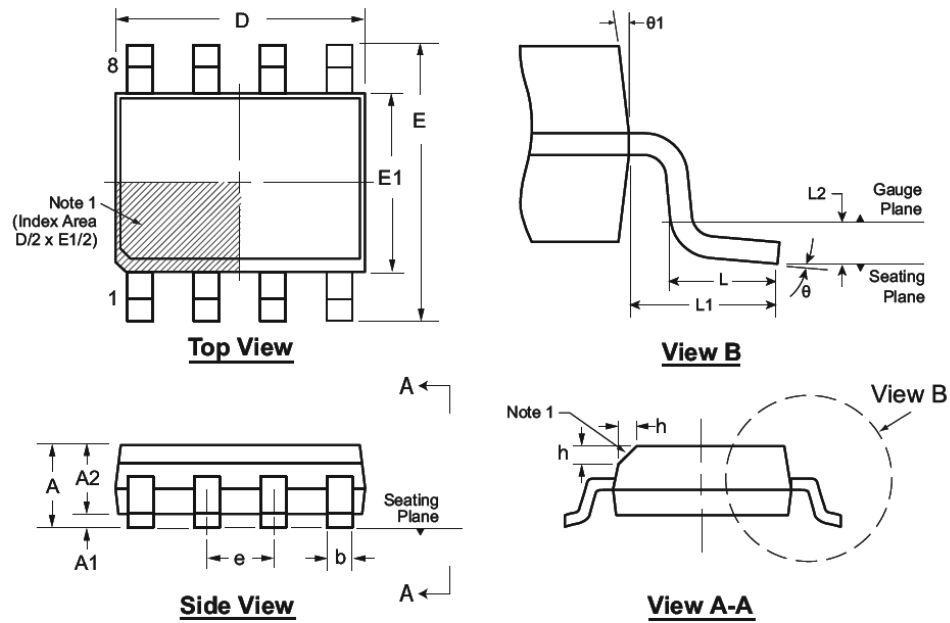
5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	Ⓔ3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (Ⓔ3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

8-Lead SOIC (Narrow Body) Package Outline (LG/TG) **4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch**



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier, an embedded metal marker, or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2022)

- Converted Supertex Doc# DSFP-TD9944 to Microchip DS20005787A
- Changed the package marking format
- Changed the quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel
- Made minor text changes throughout the document

TD9944

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.			XX	-	X	-	X
Device			Package Options		Environmental		Media Type
Device:	TD9944	=	Dual N-Channel Enhancement-Mode Vertical DMOS FET				
Package:	TG	=	8-lead SOIC				
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package				
Media Type:	(blank)	=	3300/Reel for a TG Package				

Example:

a) TD9944TG-G: Dual N-Channel Enhancement-Mode Vertical DMOS FET, 8-lead SOIC, 3300/Reel

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