LM5070 Integrated Power Over Ethernet PD Interface and PWM Controller

Check for Samples: LM5070

FEATURES

- **Fully Compliant 802.3af Power Interface Port**
- **80V, 1Ω, 400 mA Internal MOSFET**
- **Programmable Inrush Current Limit**
- **Detection Resistor Disconnect Function**
- **Programmable Classification Current**
- **Programmable Under-voltage Lockout with Programmable Hysteresis**
- **Thermal Shutdown Protection**
- **Current Mode Pulse Width Modulator**
- **Supports Both Isolated and Non-Isolated Applications**
- **Error Amplifier and Reference for Non-Isolated Applications**
- **Programmable Oscillator Frequency**
- **Programmable Soft-Start**
- **80% Maximum Duty Cycle Limiter, Slope Compensation (-80 device)**
- **50% Maximum Duty Cycle Limiter, No Slope Compensation (-50 device)**
- **800 mA Peak Gate Driver**

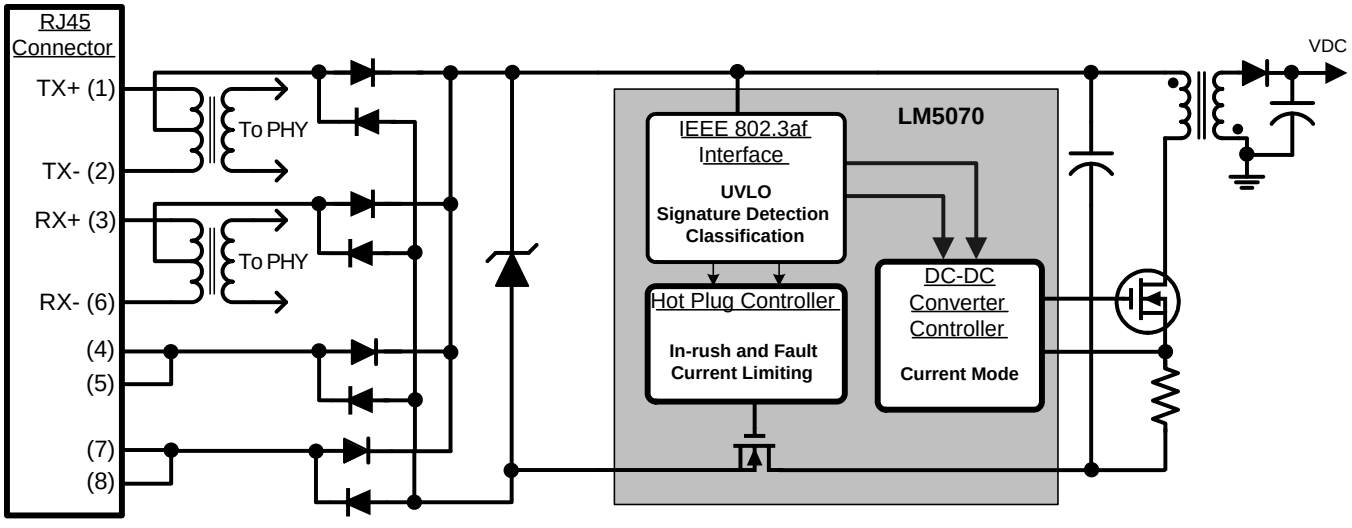
DESCRIPTION

The LM5070 power interface port and pulse width modulation (PWM) controller provides a complete integrated solution for Powered Devices (PD) that connect into Power over Ethernet (PoE) systems. The LM5070 integrates an 80V, 400mA line connection switch and associated control for a fully IEEE 802.3af compliant interface with a full featured current mode pulse width modulator dc-dc converter. All power sequencing requirements between the controller interface and switch mode power supply (SMPS) are integrated into the IC. Two options are available providing either an 80% maximum duty cycle limit with slope compensation (on the –80 suffix) device or a 50% maximum duty cycle limit and no slope compensation on the (–50 suffix) device.

PACKAGES

- **TSSOP-16**
- **WSON-16 (5 mm x 5 mm)**

Block Diagrams



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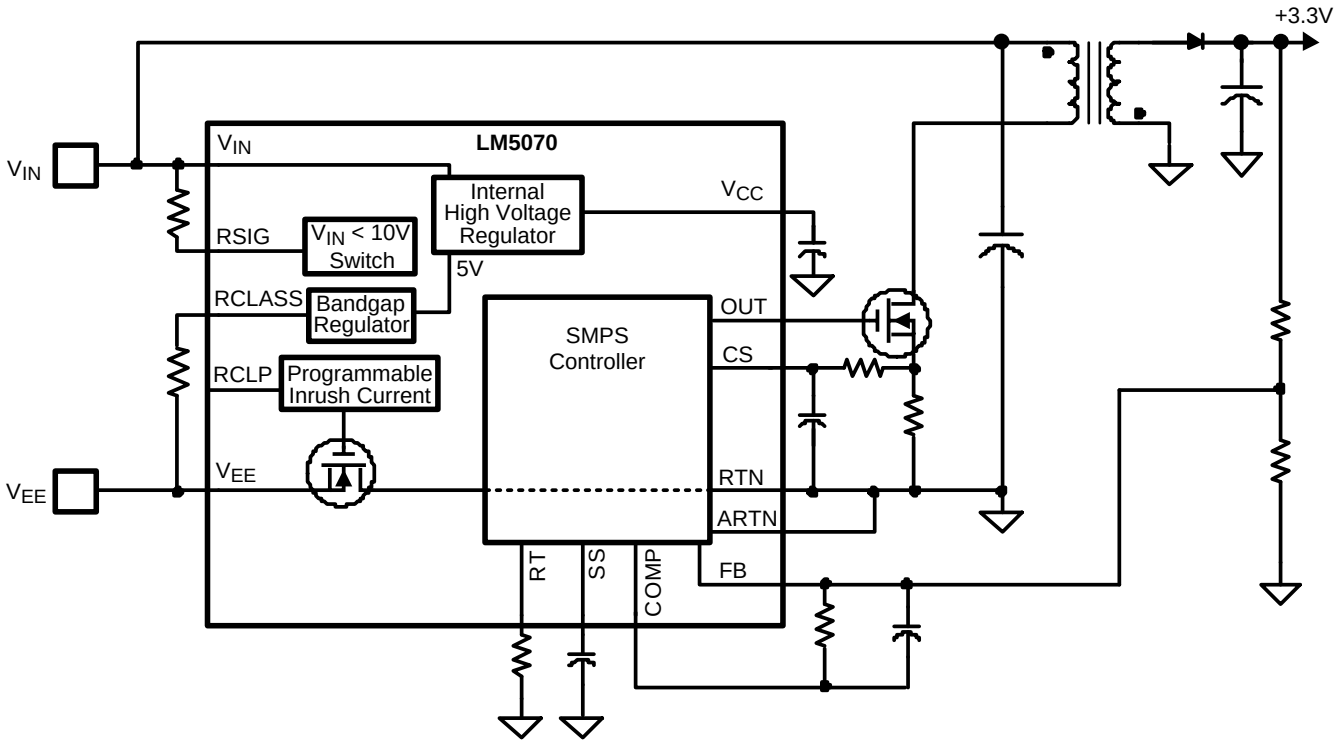

Figure 1. Simplified Block Diagram and Application

Connection Diagram

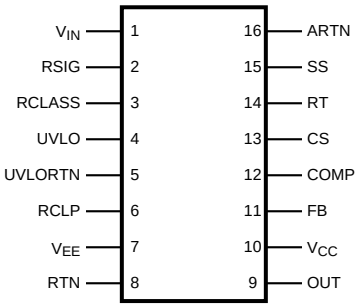

Figure 2. 16 Lead TSSOP/WSON
See Package Number PW or NHQ0016A

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PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	V_{IN}	System high potential input.	The diode “OR” of several lines entering the PD, it is the more positive input potential.
2	RSIG	Signature resistor pin.	Connect a 25kΩ signature resistor from V_{IN} to this pin for signature detection.
3	RCLASS	Classification resistor pin.	Connect the classification programming resistor from this pin to V_{EE}.
4	UVLO	Line under-voltage lockout.	An external resistor divider from V_{IN} to UVLORTN programs the shutdown levels with a 2.00V threshold at the UVLO pin. Hysteresis is set by a switched internal 10uA current source that forces additional current into the resistor divider.
5	UVLORTN	Return for the external UVLO resistors.	Connect the bottom resistor of the resistor divider between the UVLO pin and this pin.
6	RCLP	Current limit programming pin.	Programs the inrush current limit for the device. If left open, the inrush current limit will default to 400mA max.
7	V_{EE}	System low potential input.	Diode “OR’d” to the RJ45 connector and PSE’s –48V supply, it is the more negative input potential.
8	RTN	System return for the PWM converter.	The drain of the internal current limiting power MOSFET which connects V_{EE} to the return path of the dc-dc converter.
9	OUT	Output of the PWM controller.	DC-DC converter gate driver output with 800mA peak sink current capability.
10	V_{CC}	Output of the internal high voltage series pass regulator. Regulated output voltage is nominally 7.8V.	When the auxiliary transformer winding (if used) raises the voltage on this pin above the regulation set point, the internal series pass regulator will shutdown, reducing the controller power dissipation.
11	FB	Feedback signal.	Inverting input of the internal error amplifier. The non-inverting input is internally connected to a 1.25V reference.
12	COMP	The output of the error amplifier and input to the Pulse Width Modulator.	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
13	CS	Current sense input.	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5V the OUT pin switches low for cycle-by-cycle current limiting. CS is held low for 50ns after OUT switches high to blank leading edge current spikes.
14	RT / SYNC	Oscillator timing resistor pin and synchronization input.	An external resistor connected from RT to ARTN sets the oscillator frequency. This pin will also accept narrow ac-coupled synchronization pulses from an external clock.
15	SS	Soft-start input.	An external capacitor and an internal 10uA current source set the soft-start ramp rate.
16	ARTN	Analog PWM supply return.	RTN for sensitive analog circuitry including the SMPS current limit amplifier.
—	EP	Exposed PAD, underside of the WSON package option.	Internally bonded to the die substrate. Connect to V_{EE} potential for low thermal impedance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

V_{IN} ,RTN to V_{EE}		-0.3V to 80V
RSIG to V_{IN}		-12V to 0V
UVLO to V_{EE}		-0.3V to 57V
UVLORTN		-0.3V to 13V
RCLASS, RCLP to V_{EE}		-0.3V to 7V
ARTN to RTN		-0.3V to 0.3V
V_{CC}, OUT to ARTN		-0.3V to 16V
All other inputs to ARTN		-0.3V to 7V
ESD Rating	Human Body Model	2000V
Storage Temperature		-65°C to +150°C
Junction Temperature		150°C
Lead Temperature[3]	Wave (4 seconds)	260°C
	Infrared (10 seconds)	240°C
	Vapor Phase (75 seconds)	219°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics. The absolute maximum rating of V_{IN}, RTN to V_{EE} is derated to (-0.3V to 76V) at -40°C.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For detailed information on soldering plastic TSSOP and WSON packages, see the Packaging Databook available from TI.

Operating Ratings

V_{IN} voltage	1.8V to 75V
External voltage applied to V_{CC}	8.1V to 15V
Operating Junction Temperature	-40°C to +125°C

Electrical Characteristics[1]

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, V_{CC} = 10V, RT = 30.3kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Powered Interface						
IOS	Offset Current	V_{IN} < 10.0V			**10**	uA
VCLSS(ON)	Signature Resistor Disable / Classification Current Turn On	V_{IN} with respect to V_{EE}	**10.0**	11.5	**12.5**	V
VCLSS(OFF)	Classification Current Turn Off	V_{IN} with respect to V_{EE}	**20.5**	22.0	**23.0**	V
	Classification Voltage	With respect to V_{EE}	**1.43**	1.5	**1.57**	V
ICLASS	Supply Current During Classification	V_{IN} =17V		0.5	**1.0**	mA
IDC	Supply Current During Normal Operation	OUT floating		1	**1.9**	mA
	UVLO Pin Reference Voltage	V_{IN} > 12V	**1.95**	2.00	**2.05**	V
	UVLO Hysteresis Current	V_{IN} > UVLO	**8.0**	10	**11.5**	uA
	Softstart Release	RTN falling with respect to V_{EE}	**1.2**	1.45	**1.7**	V
	Softstart Release Hysteresis	RTN rising with respect to V_{EE}	**0.8**	1.1	**1.3**	V
RDS(ON)	PowerFET Resistance	I = 350mA, V_{IN} = 48V		1	**2.2**	Ω
ILEAK	SMPS Bias Current	V_{EE} = 0V, V_{IN} = RTN = 57V			**100**	uA
ILIM	Default Current Limit	V_{EE} = 0V, RTN = 3.0V, Temp = 0°C to 85°C	**350**	390	**420**	mA

(1) Min and Max limits are 100% production tested at 25 °C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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Electrical Characteristics[1] (continued)

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, V_{CC} = 10V, RT = 30.3kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILIM	Default Current Limit	V_{EE} = 0V, RTN = 3.0V, Temp = -40°C to 125°C	**325**	390	**420**	mA
	Current Limit Programming Accuracy	V_{EE} = 0V, RTN = 3.0V, RCLP = 80.6kΩ	**-20**		**+20**	%
Startup Regulator						
VccReg	V_{CC} Regulation	Open ckt	**7.5**	7.8	**8.1**	V
	V_{CC} Current Limit	See[2]	**15**	20		mA
V_{CC} Supply						
	V_{CC} UVLO (Rising)		**VccReg – 300mV**	VccReg – 100mV		
	V_{CC} UVLO (Falling)		**5.9**	6.25	**6.6**	V
	Supply Current (Icc)	Cload = 0		1.5	**3**	mA
Error Amplifier						
GBW	Gain Bandwidth			4		MHz
	DC Gain			75		dB
	Input Voltage	FB = COMP	1.219 **1.212**		1.281 **1.288**	V
	COMP Sink Capability	FB=1.5V COMP=1V	**5**	20		mA
Current Limit						
	ILIM Delay to Output	CS step from 0 to 0.6V, time to onset of OUT transition (90%)		20		ns
	Cycle by Cycle Current Limit Threshold Voltage		**0.44**	0.5	**0.56**	V
	Leading Edge Blanking Time			55		ns
	CS Sink Impedance (clocked)			25	**55**	Ω
Softstart						
	Softstart Current Source		**7**	10	**13**	uA
Oscillator[3]						
	Frequency1 (RT = 30.3K)		**175**	200	**225**	KHz
	Frequency2 (RT = 10.5K)		**505**	580	**665**	KHz
	Sync threshold			3.1	**3.8**	V
PWM Comparator						
	Delay to Output	COMP set to 2V CS stepped 0 to 0.4V, time to onset of OUT transition low		25		ns
	Min Duty Cycle	COMP=0V			**0**	%
	Max Duty Cycle (-80 Device)			80		%
	Max Duty Cycle (-50 Device)			50		%
	COMP to PWM Comparator Gain			0.33		
	COMP Open Circuit Voltage		**4.5**	5.4	**6.3**	V
	COMP Short Circuit Current	COMP= 0V	**0.6**	1.1	**1.5**	mA
Slope Compensation						
	Slope Comp Amplitude (LM5070-80 Device Only)	Delta increase at PWM Comparator to CS		105		mV

(2) Device thermal limitations may limit usable range.
(3) Specification applies to the oscillator frequency. The operational frequency of the LM5070-50 devices is divided by two.

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Electrical Characteristics[1] (continued)

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V_{IN} = 48V, V_{CC} = 10V, RT = 30.3kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Section						
	Output High Saturation	I_{out} = 50mA, V_{CC} - V_{OUT}		0.25	**0.75**	V
	Output Low Saturation	I_{out} = 100mA		0.25	**0.75**	V
	Rise time	Cload = 1nF		15		ns
	Fall time	Cload = 1nF		15		ns
Thermal Shutdown						
Tsd	Thermal Shutdown Temp.			165		°C
Thermal Shutdown Hysteresis				25		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	PW Package		125		°C/W
		NHQ0016A Package		32		°C/W

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Typical Performance Characteristics

Default Current Limit vs Temperature

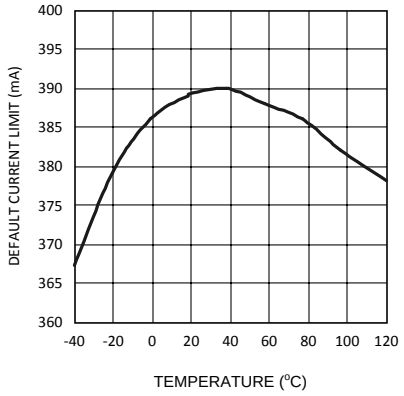

Figure 3.

Inrush Current Limit vs RCLP Resistor

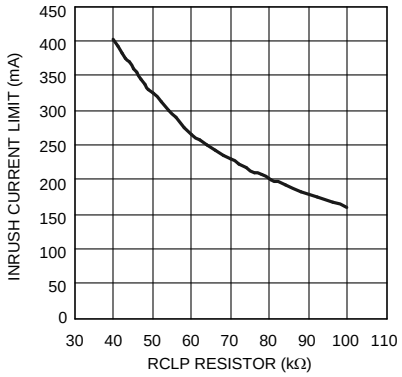

Figure 4.

Oscillator Frequency vs RT Resistance

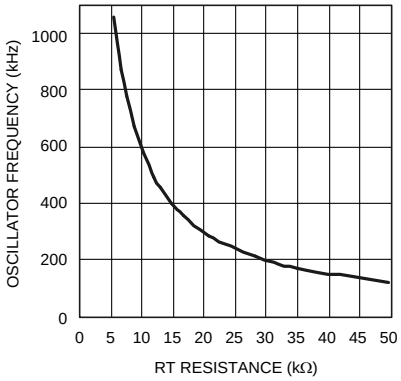

Figure 5.

UVLO Hysteresis Current vs Temperature

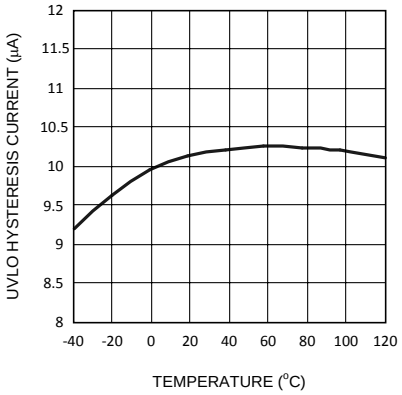

Figure 6.

Softstart Current vs Temperature

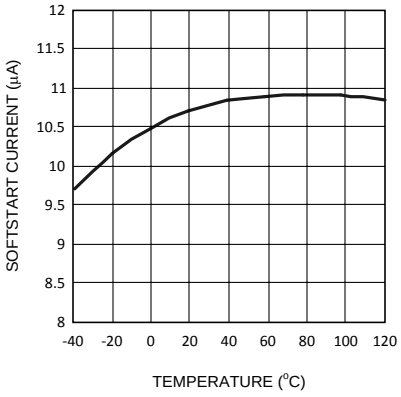

Figure 7.

Error Amp Input Voltage vs temperature

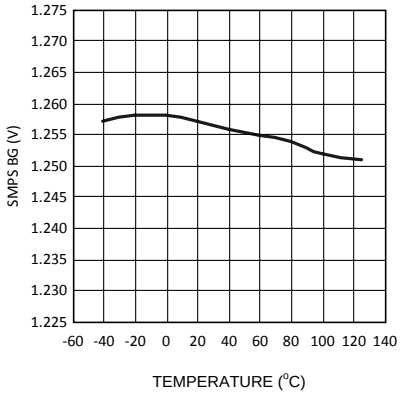

Figure 8.

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Typical Performance Characteristics (continued)

Oscillator Frequency vs Temperature RT = 15.2 kΩ

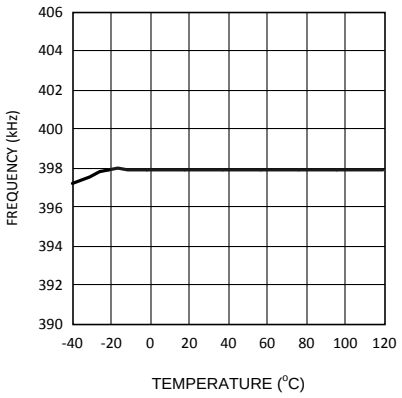

Figure 9.

V_{CC} vs I_{CC}

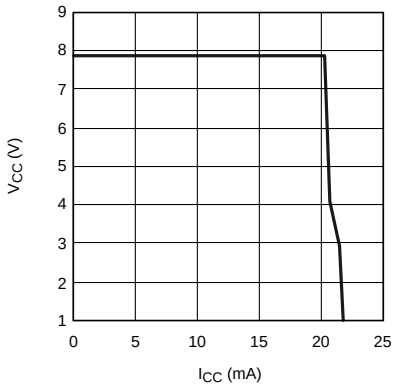

Figure 10.

Input Current vs Input Voltage

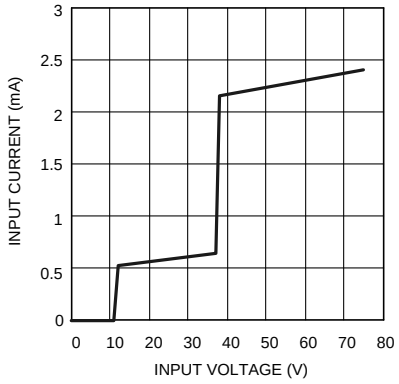

Figure 11.

UVLO Threshold vs Temperature

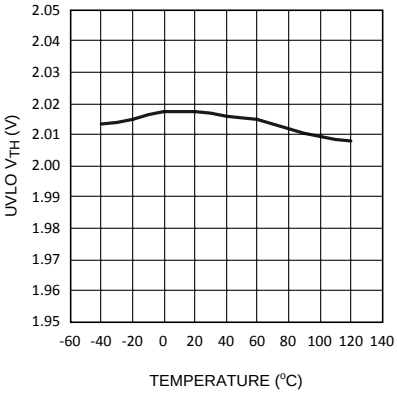

Figure 12.

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BLOCK DIAGRAMS

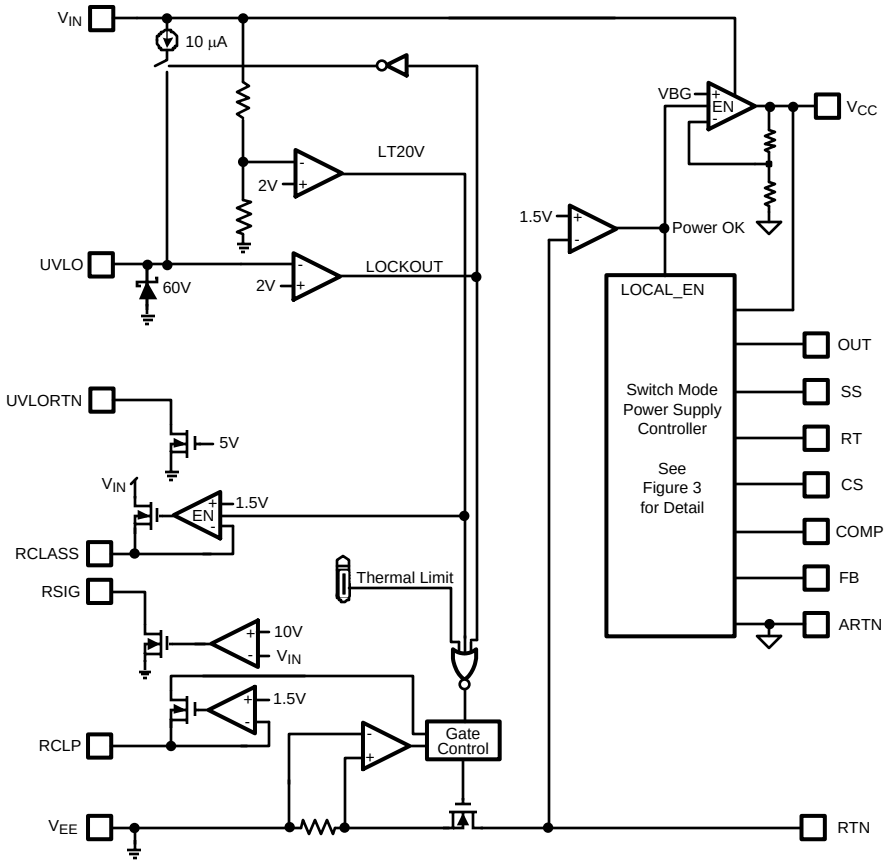

Figure 13. Top Level Block Diagram

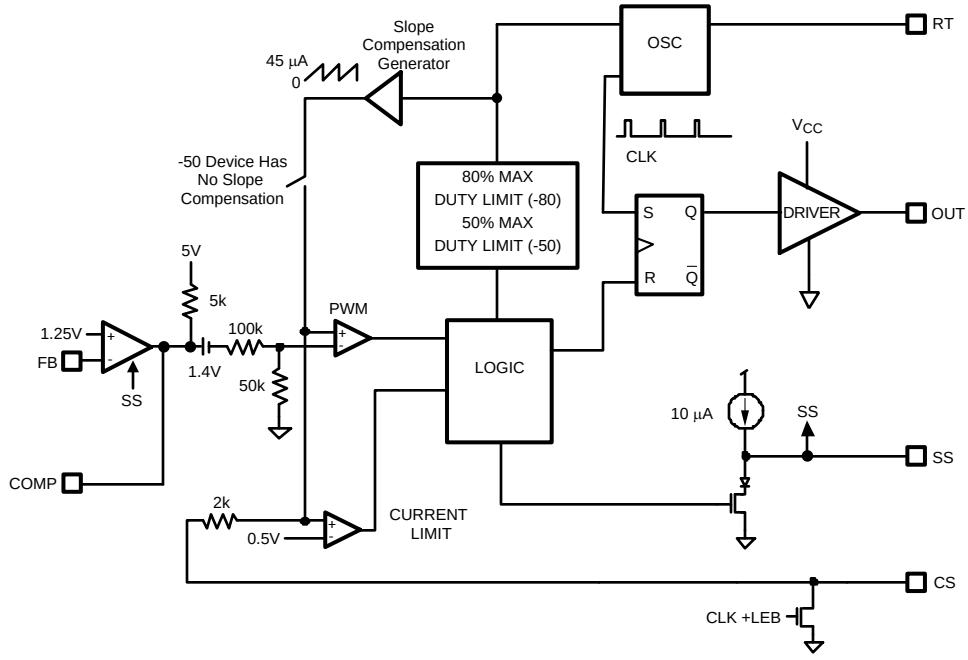

Figure 14. PWM Controller Block Diagram

Detailed Operating Description

The LM5070 power interface port and pulse width modulation (PWM) controller provides a complete integrated solution for Powered Devices (PD) that connect into Power over Ethernet (PoE) systems. Major features of the PD interface portion of the IC include detection, classification, programmable inrush current limit, thermal limit, programmable undervoltage lockout, and current limit monitoring. The device also includes a high-voltage start-up bias regulator that operates over a wide input range up to 75V. The switch mode power supply (SMPS) control portion of the IC includes power good sensing, V_{CC} regulator under-voltage lockout, cycle-by-cycle current limit, error amplifier, slope compensation, softstart, and oscillator sync capability. This high speed BiCMOS IC has total propagation delays less than 100ns and a 1MHz capable oscillator programmed by a single external resistor. The LM5070 PWM controller provides current-mode control for dc-dc converter topologies requiring a single drive output, such as Flyback and Forward topologies. The LM5070 PWM enables all of the advantages of current-mode control including line feed-forward, cycle-by-cycle current limit and simplified loop compensation. The oscillator ramp is internally buffered and added to the PWM comparator input ramp to provide slope compensation necessary for current mode control at duty cycles greater than 50% (-80 suffix only).

Modes of Operation

The LM5070 PD interface is designed to provide a fully compliant IEEE 802.3af system. As such, the modes of operation take into account the barrel rectifiers often utilized to correctly polarize the dc input from the Ethernet cable. Table 1 shows the LM5070 operating modes and associated input voltage range.

Table 1. Operating Modes With Respect to Input Voltage

Input Voltage V_{IN} wrt V_{EE}	Mode of Operation
1.8V to 10.0V	Detection (Signature)
12.5V to 20.5V	Classification
23.0V to UVLO Rising Vth	Awaiting Full Power
75V to UVLO Falling Vth	Normal Powered Operation

An external signature resistor is connected to V_{EE} when V_{IN} exceeds 1.8V, initiating detection mode. During detection mode, quiescent current drawn by the LM5070 is less than 10uA. Between 10.0V and 12.5V, the device enters classification mode and the signature resistor is disabled. The nominal range for classification mode is 11.5V to 21.5V. The classification current is turned off once the classification range voltage is exceeded, to reduce power dissipation. Between 21.5V and UVLO release, the device is in a standby state, awaiting the input voltage to reach the operational range to complete the power up sequence. Once the V_{IN} voltage increases above the upper UVLO threshold voltage, the internal power MOSFET is enabled to deliver a constant current to charge the input capacitor of the dc-dc converter. When the MOSFET Vds voltage falls below 1.5V, the internal Power Good signal enables the SMPS controller. The LM5070 is specified to operate with an input voltage as high as 75V. The SMPS controller and internal MOSFET are disabled when V_{IN} falls to the lower UVLO threshold.

Detection Signature

To detect a potential powered device candidate, the PSE will apply a voltage from 2.8V to 10V across the input terminals of the PD. The voltage can be of either polarity so a diode barrel network is required on both lines to ensure this capability. The PSE will take two measurements, separated by at least 1V and 2ms of time. The voltage ramp between measurement points will not exceed 0.1V/us. The delta voltage / delta current calculation is then performed; if the detected impedance is above 23.75kΩ and below 26.25kΩ, the PSE will consider a PD to be present. If the impedance is less than 15kΩ or greater than 33kΩ a PD will be considered not present and will not receive power. Impedances between these values may or may not indicate the presence of a valid PD. The LM5070 will enable the signature resistor at a controller input voltage of 1.5V to take into account the diode voltage drops. The PSE will tolerate no more than 1.9V of offset voltage (caused by the external diodes) or more than 10uA of offset current (bias current). The input capacitance must be greater than 0.05uF and less than 0.12uF. To increase efficiency, the signature resistor is disabled by the LM5070 controller once the input voltage is above the detection range (> 11V).

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Classification

To classify the PD, the PSE will present a voltage between 14.5V and 20.5V to the PD. The LM5070 enables classification mode at a nominal input voltage of 11.5V. An internal 1.5V linear regulator and an external resistor connected to the RCLASS pin provide classification programming current. Table 2 shows the external classification resistor required for a particular class.

The classification current flows through the IC into the classification resistor. The suggested resistor values take into account the bias current flowing into the IC. A different desired RCLASS can be calculated by dividing 1.5V by the desired classification current.

Per the IEEE 802.3af specification, classification is optional, and the PSE will default to class 0 if a valid classification current is not detected. If PD classification is not desired (i.e., Class 0), simply leave the RCLASS pin open. The classification time period may not last longer then 75ms as per IEEE 802.3af. The LM5070 will remain in classification mode until V_{IN} is greater than 22V.

Table 2. Classification Levels and Required External Resistors

Class	PMIN	PMAX	ICLASS (MIN)	ICLASS (MAX)	RCLASS
0	0.44W	12.95W	0mA	4mA	Open
1	0.44W	3.84W	9mA	12mA	150Ω
2	3.84W	6.49W	17mA	20mA	82.5Ω
3	6.49W	12.95W	26mA	30mA	53.6Ω
4	Reserved	Reserved	36mA	44mA	38.3Ω

Undervoltage Lockout (UVLO)

The IEEE 802.3af specification states that the PSE will supply power to the PD within 400ms after completion of detection. The LM5070 contains a programmable line Under Voltage Lock Out (UVLO) circuit. The first resistor should be connected between the V_{IN} to UVLO pins; the bottom resistor in the divider should be connected between the UVLO and UVLORTN pins. The bottom resistor should not be tied to V_{EE} because any current from V_{IN} to V_{EE} will cause the system to violate the 10uA maximum offset current specification during detection mode.

The divider must be designed such that the voltage at the UVLO pin equals 2.0V when V_{IN} reaches the desired minimum operating level. If the UVLO threshold is not met, the interface control and SMPS control will remain in standby.

UVLO hysteresis is accomplished with an internal 10uA current source that is switched on and off into the impedance of the UVLO set point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.00V threshold, the current source is turned off, causing the voltage at the UVLO pin to fall. The LM5070 UVLO thresholds cannot be programmed lower than 23V, otherwise the device would operate in classification mode with both the classification current source and the SMPS enabled. The combined power dissipation of these two functions could exceed the maximum power dissipation of the package.

There are many additional uses for the UVLO pin. The UVLO function can also be used to implement a remote enable / disable function. Pulling the UVLO pin down below the UVLO threshold disables the interface and SMPS controller.

Power Supply Operation / Current Limit Programming

Once the UVLO threshold has been satisfied, the interface controller of the LM5070 will charge up the SMPS input capacitor through the internal power MOSFET. This load capacitance provides input filtering for the power converter section and must be at least 5uF per the IEEE 802.3af specification. To accomplish the charging in a controlled manner, the power MOSFET is current limited to 375mA. The IEEE 802.3af specification requires that the load capacitance be charged within 75ms.

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Some legacy PSEs may not be able to supply the IEEE maximum power of 15W to the PD, and this can be a problem during startup. Low power PDs that are used in these legacy systems will require a lower startup current limit. The LM5070 can be programmed for a reduced inrush current limit level with a resistor at RCLP pin. The programmable inrush current limit range is 75mA to 390mA. If the RCLP pin is left open, the LM5070 will default to 390mA, near the maximum allowed per the IEEE 802.3 specification. To set a desired inrush current limit (limit), the RCLP resistor can be calculated from:

$$RCLP = \frac{16000\Omega\text{-}A}{I_{limit}\ (A)} \quad (1)$$

The SMPS controller will not initiate operation until the load capacitor is completely charged. The power sequencing between the interface circuitry and the SMPS controller occurs automatically within the LM5070. Detection circuitry monitors the RTN pin to detect interface startup completion. When the RTN pin potential drops below 1.5V with respect to V_{EE}, the V_{CC} regulator of the SMPS controller is enabled. The soft-start function is enabled once the V_{CC} regulator achieves minimum operating voltage. The RCLP programmed inrush current limit only applies to the initial charging phase. The interface power MOSFET current limit will revert to the fixed default protection current limit of 390mA once the SMPS is powered up and the soft-start pin sequence begins.

High Voltage Start-Up Regulator

The LM5070 contains an internal high voltage startup regulator that allows the input pin (V_{IN}) to be connected directly to line voltages as high as 75V. The regulator output is internally current limited to 15mA. The recommended capacitance range for the V_{CC} regulator output is 0.1uF to 10uF. When the voltage on the V_{CC} pin reaches the regulation point of 7.8V, the controller output is enabled. The controller will remain enabled until V_{CC} falls below 6.25V.

In typical applications, a transformer auxiliary winding is diode connected to the V_{CC} pin. This winding should raise the V_{CC} voltage above 8.1V to shut off the internal startup regulator. Though not required, powering V_{CC} from an auxiliary winding improves conversion efficiency while reducing the power dissipated in the controller. The external V_{CC} capacitor must be selected such that the capacitor maintains the V_{CC} voltage greater than the V_{CC} UVLO falling threshold (6.25V) during the initial start-up. During a fault condition when the converter auxiliary winding is inactive, external current draw on the V_{CC} line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation capability of the LM5070 package.

Error Amplifier

An internal high gain error amplifier is provided within the LM5070. The amplifier's non-inverting reference is set to a fixed reference voltage of 1.25V. The inverting input is connected to the FB pin. In non-isolated applications, the power converter output is connected to the FB pin via voltage scaling resistors. Loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amplifier is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ARTN. An internal 5K pull-up resistor between a 5V reference and COMP can be used as the pull-up for an optocoupler in isolated applications.

Current Limit / Current Sense

The LM5070 provides a cycle-by-cycle over current protection function. Current limit is accomplished by an internal current sense comparator. If the voltage at the current sense comparator input CS exceeds 0.5V with respect to RTN/ARTN, the output pulse will be immediately terminated. A small RC filter, located near the CS pin of the controller, is recommended to filter noise from the current sense signal. The CS input has an internal MOSFET which discharges the CS pin capacitance at the conclusion of every cycle. The discharge device remains on an additional 50ns after the beginning of the new cycle to attenuate the leading edge spike on the current sense signal.

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The LM5070 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be located very close to the device and connected directly to the pins of the controller (CS and ARTN). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor and the current sense filter network. A sense resistor located in the source of the primary power MOSFET may be used for current sensing, but a low inductance resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together local to the controller and a single connection should be made to the high current power return (sense resistor ground point).

Oscillator, Shutdown and Sync Capability

A single external resistor connected between the RT and ARTN pins sets the LM5070 oscillator frequency. Internal to the LM5070–50 device (50% duty cycle limited option) is an oscillator divide by two circuit. This divide by two circuit creates an exact 50% duty cycle clock which is used internally to create a precise 50% duty cycle limit function. Because of this divide by two, the internal oscillator actually operates at twice the frequency of the output (OUT). For the LM5070–80 device the oscillator frequency and the operational output frequency are the same. To set a desired output operational frequency (F), the RT resistor can be calculated from:

LM5070-80:

$$RT = \frac{1}{F \times 165 \times 10^{-12}} \tag{2}$$

LM5070-50:

$$RT = \frac{1}{F \times 330 \times 10^{-12}} \tag{3}$$

The LM5070 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100pF capacitor. A peak voltage level greater than 3.7 volts at the RT pin is required for detection of the sync pulse. The sync pulse width should be set between 15 to 150ns by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to a 2 volts. The RT resistor should be located very close to the device and connected directly to the pins of the controller (RT and ARTN).

PWM Comparator / Slope Compensation

The PWM comparator compares the current ramp signal with the loop error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4V and then further attenuated by a 3:1 resistor divider. The PWM comparator polarity is such that 0 Volts on the COMP pin will result in zero duty cycle at the controller output. For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5070-80 integrates this slope compensation by summing a current ramp generated by the oscillator with the current sense signal. Additional slope compensation may be added by increasing the source impedance of the current sense signal (with an external resistor between the CS pin and current sense resistor). Since the LM5070-50 is not capable of duty cycles greater than 50%, there is no slope compensation feature in this device.

Softstart

The softstart feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses, output overshoot and current surges. At power on, after the V_{CC} undervoltage lockout threshold is satisfied, an internal 10µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and the duty cycle of the output pulses.

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Gate Driver and Maximum Duty Cycle Limit

The LM5070 provides an internal gate driver (OUT), which can source and sink a peak current of 800mA. The LM5070 is available in two duty cycle limit options. The maximum output duty cycle is typically 80% for the LM5070-80 option and precisely equal to 50% for the LM5070-50 option. The maximum duty cycle function for the LM5070-50 is accomplished with an internal toggle flip-flop which ensures an accurate duty cycle limit. The internal oscillator frequency of the LM5070-50 is therefore twice the operating frequency of the PWM controller (OUT pin).

The 80% maximum duty cycle limit of the LM5070-80 is determined by the internal oscillator and varies more than the 50% limit of the LM5070-50. For the LM5070-80, the internal oscillator frequency and the operational frequency of the PWM controller are equal.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. This feature prevents catastrophic failures from accidental device overheating. When activated, typically at 165 degrees Celsius, the controller is forced into a low power standby state, disabling the output driver, bias regulator, main interface pass MOSFET, and classification regulator if enabled. After the temperature is reduced (typical hysteresis = 25°C) the V_{CC} regulator will be enabled and a softstart sequence initiated.

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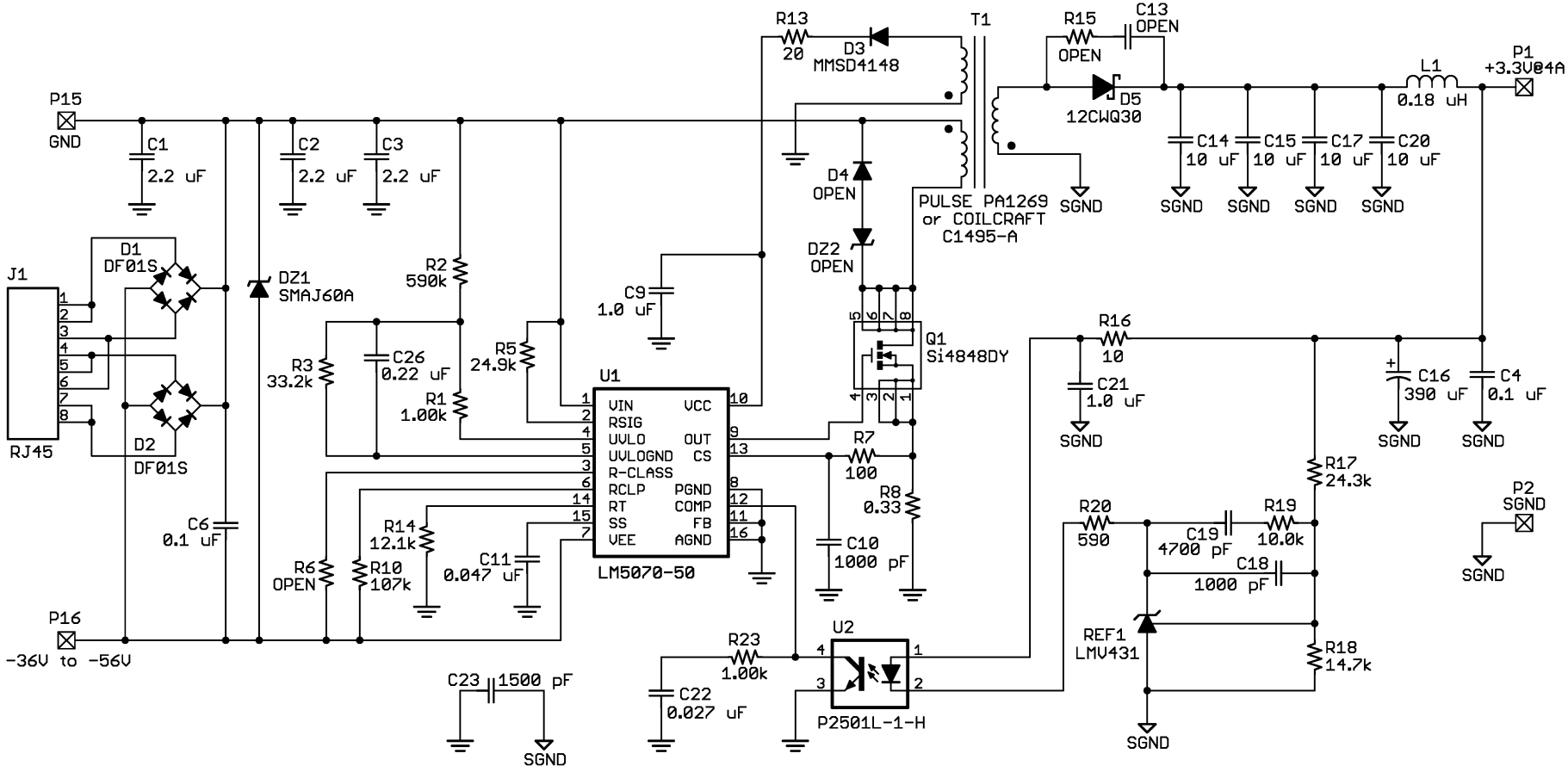
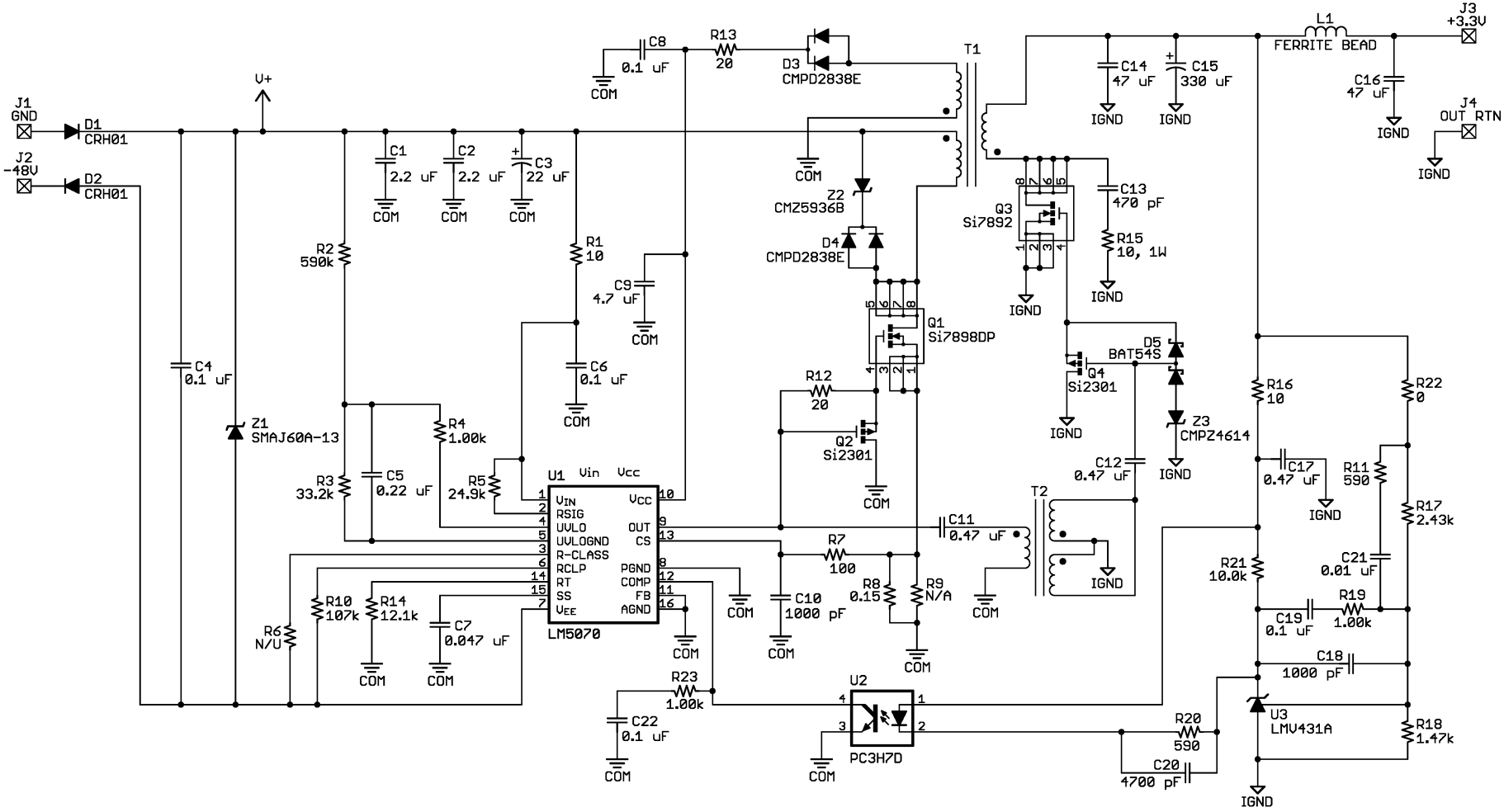
LM5070 Application Circuit – Isolated Output with Diode Rectification



LM5070 Application Circuit – Isolated Output with Synchronous Rectification



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REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	16

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5070MTC-50/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-50
LM5070MTC-50/NOPB.B	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-50
LM5070MTC-80/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070MTC-80/NOPB.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070MTC-80/NOPB.B	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070MTCX-50/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-50
LM5070MTCX-50/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-50
LM5070MTCX-80/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070MTCX-80/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070MTCX-80/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5070M TC-80
LM5070SD-50/NOPB	Active	Production	WSON (NHQ) | 16	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00051B
LM5070SD-50/NOPB.B	Active	Production	WSON (NHQ) | 16	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00051B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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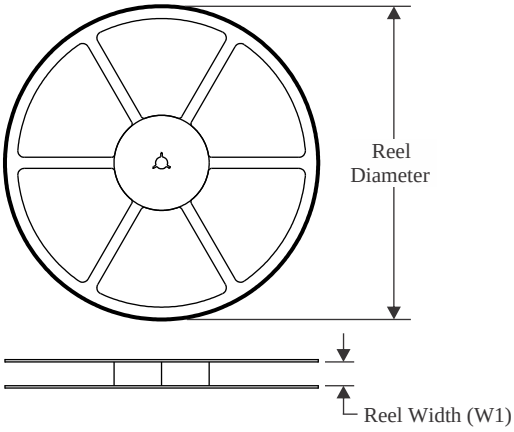
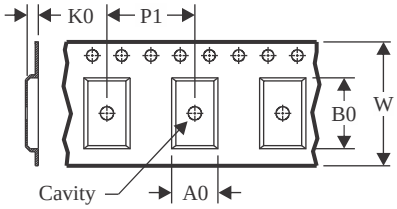
TAPE AND REEL INFORMATION

REEL DIMENSIONS

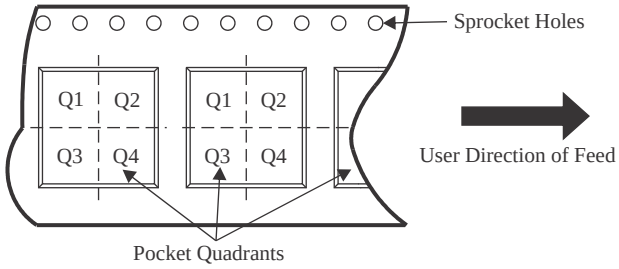


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

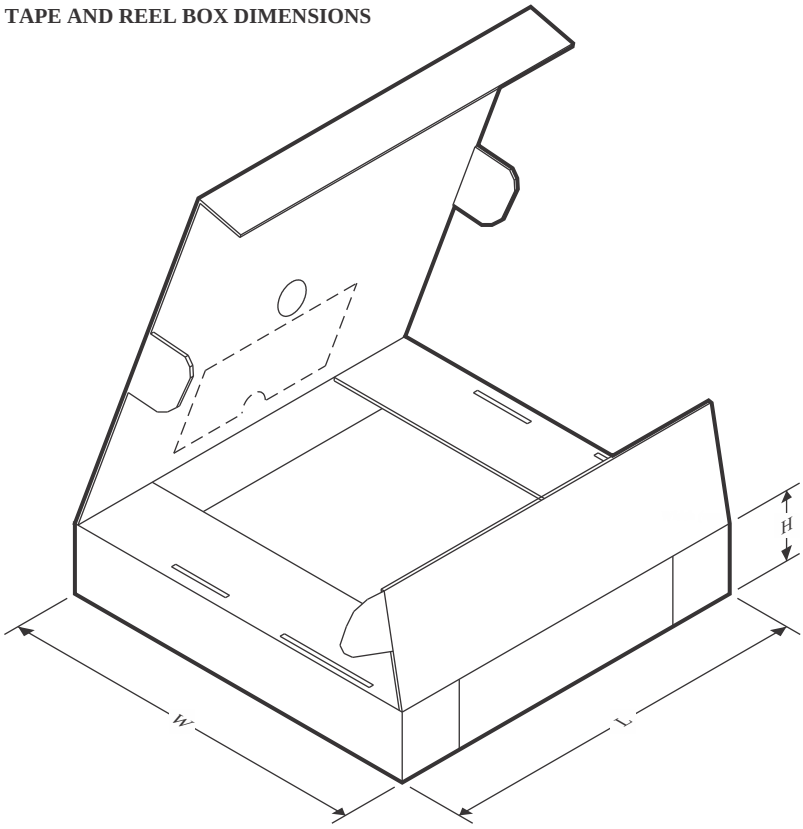
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5070MTCX-50/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5070MTCX-80/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5070SD-50/NOPB	WSON	NHQ	16	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

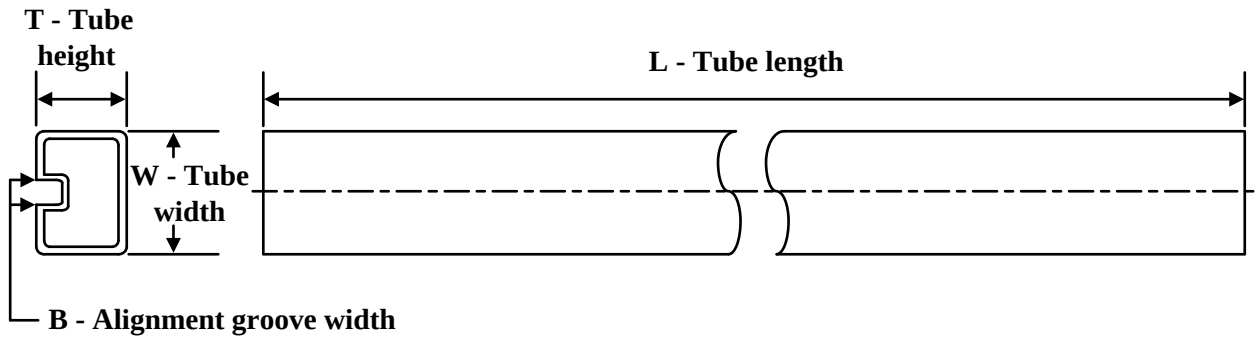
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5070MTCX-50/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5070MTCX-80/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5070SD-50/NOPB	WSON	NHQ	16	1000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

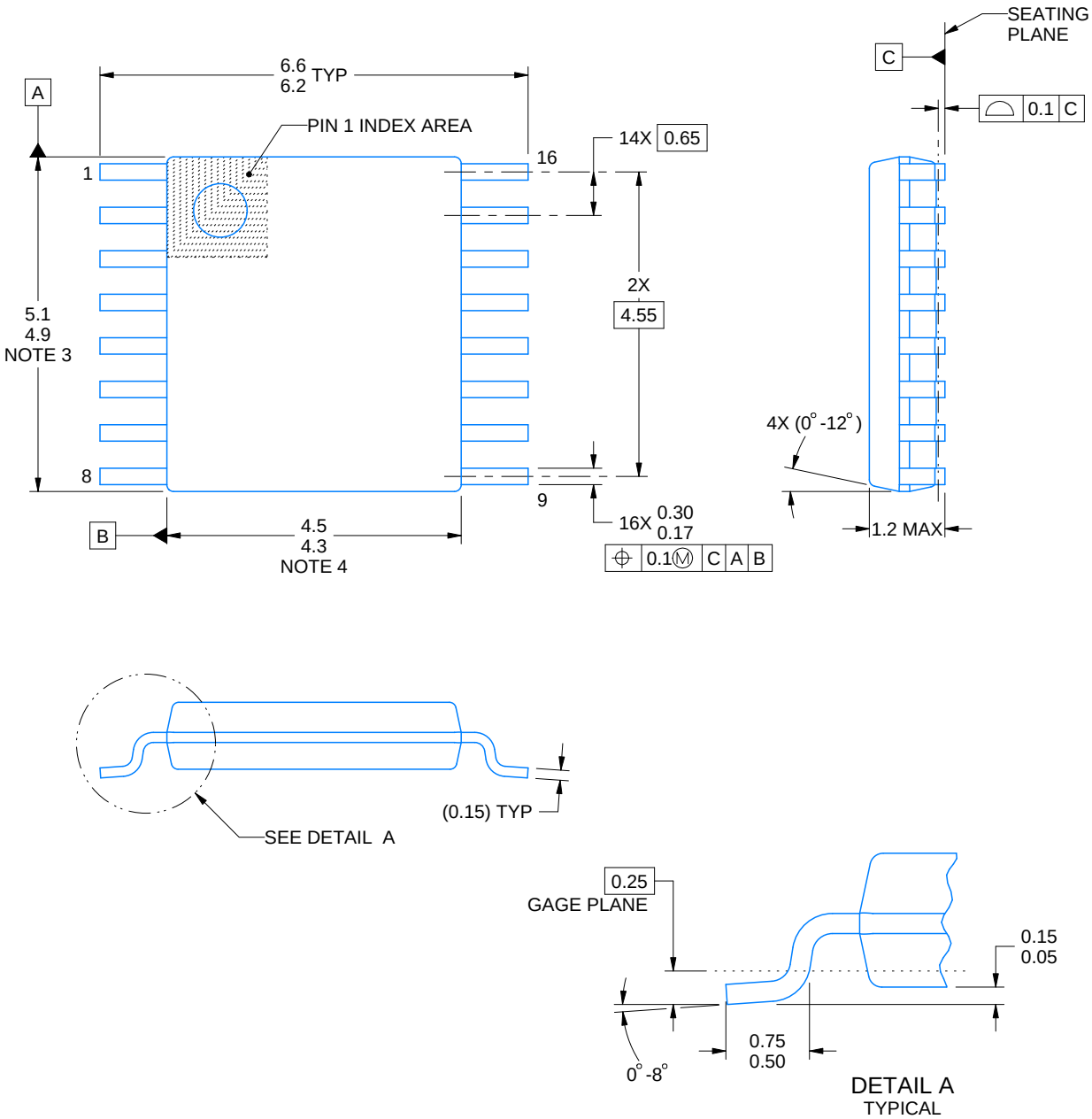
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5070MTC-50/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5070MTC-50/NOPB.B	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5070MTC-80/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5070MTC-80/NOPB.A	PW	TSSOP	16	92	495	8	2514.6	4.06
LM5070MTC-80/NOPB.B	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

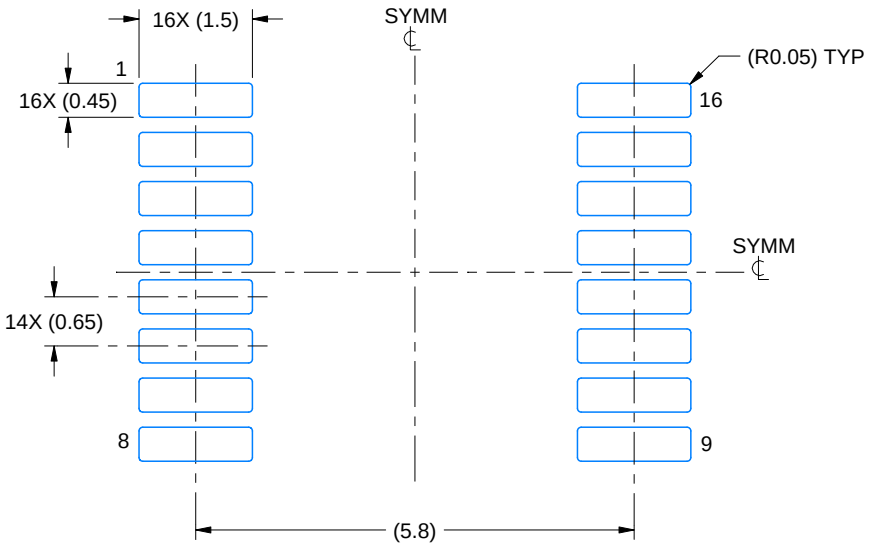
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

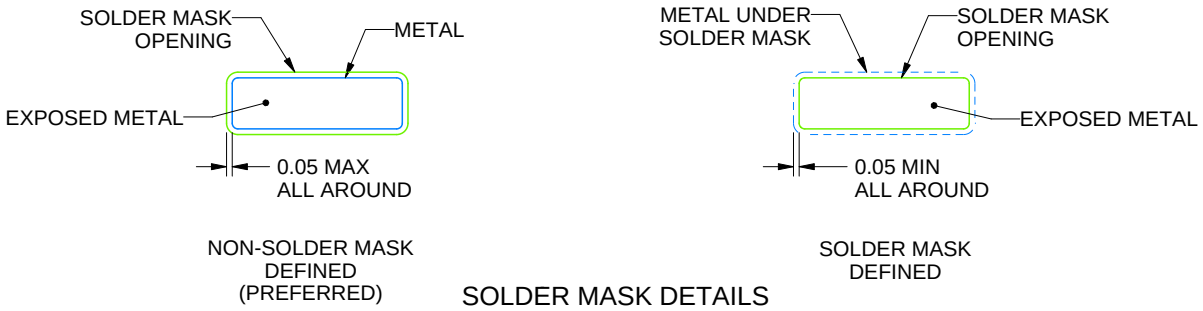


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

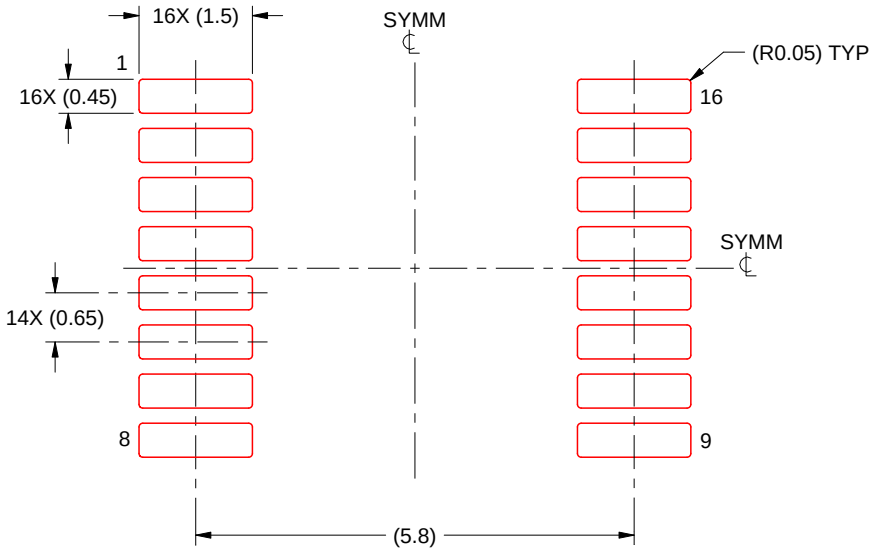


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



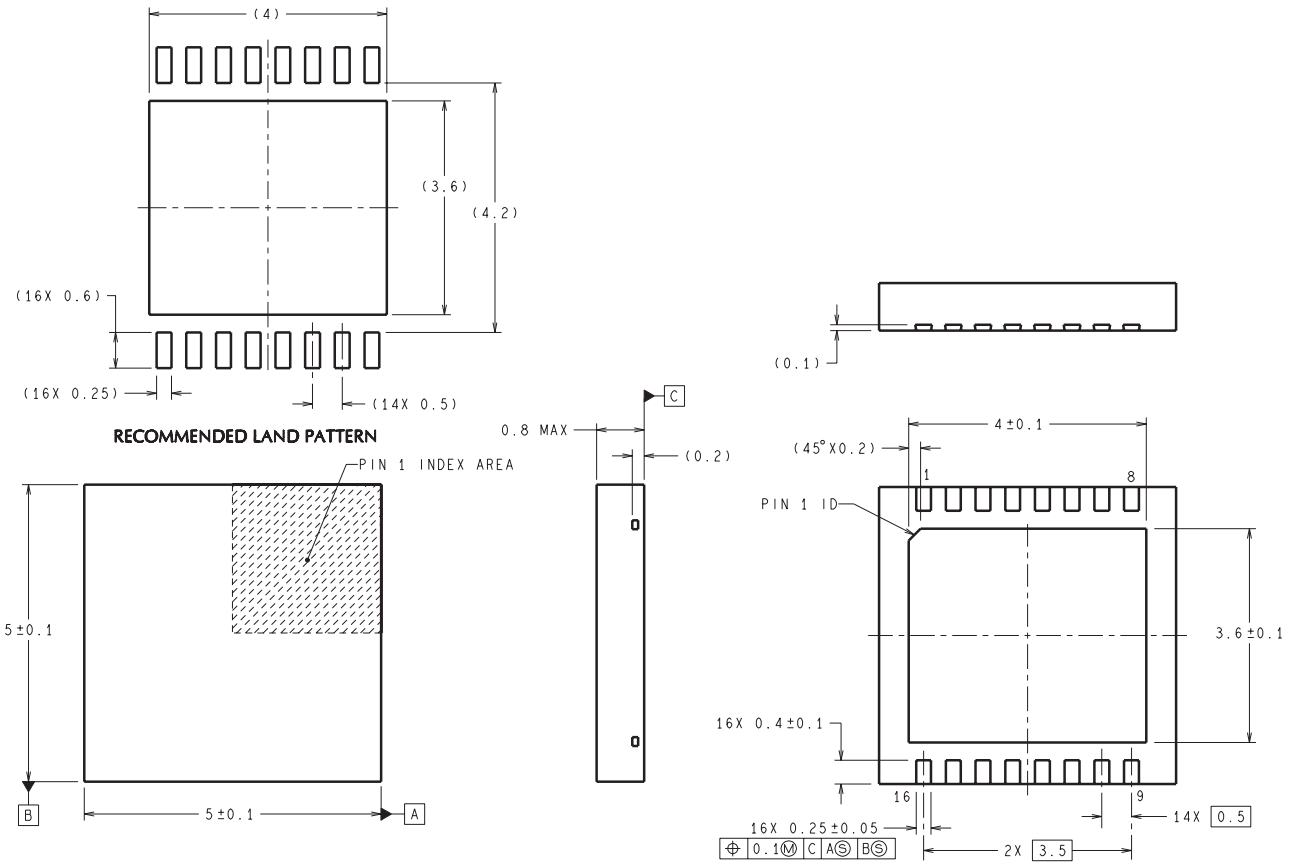
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NHQ0016A



DIMENSIONS ARE IN MILLIMETERS

SDA16A (Rev A)

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