

Quick Start Guide for testing the AD9257/AD9637 ADC Evaluation Board using the FPGA based Capture Board HSC-ADC-EVALCZ

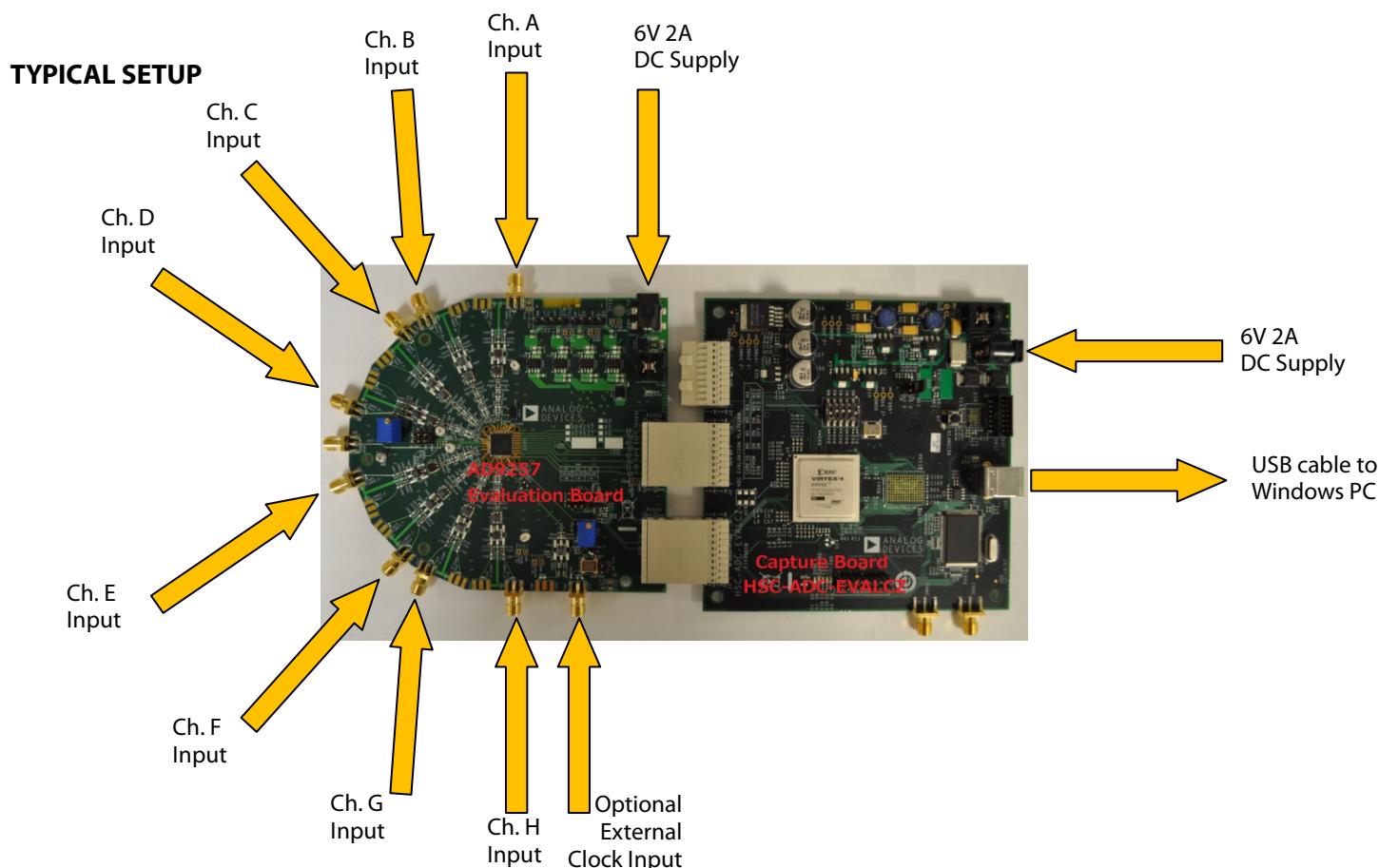


Figure 1. AD9257/AD9637 Evaluation Board and HSC-ADC-EVALCZ Data Capture Board

EQUIPMENT NEEDED

- 2x 6V 2A switching supply (such as CUI EPS060250UH-PHP-SZ)
- Analog signal source and anti aliasing filter
- Analog Clock source if not using the on-board crystal
- PC running Windows
- USB 2.0 port recommended (USB 1.1 compatible)
- AD9257/AD9637 Evaluation Board (AD9257-65EBZ or AD9637-80EBZ)
- HSC-ADC-EVALCZ FPGA Based Data Capture Board

HELPFUL DOCUMENTS

- AD9257/AD9637 Datasheet
- VisualAnalog Converter Evaluation Tool User Manual, AN-905
- High Speed ADC SPI Control Software User Manual, AN-878
- Interfacing to High Speed ADCs via SPI, AN-877

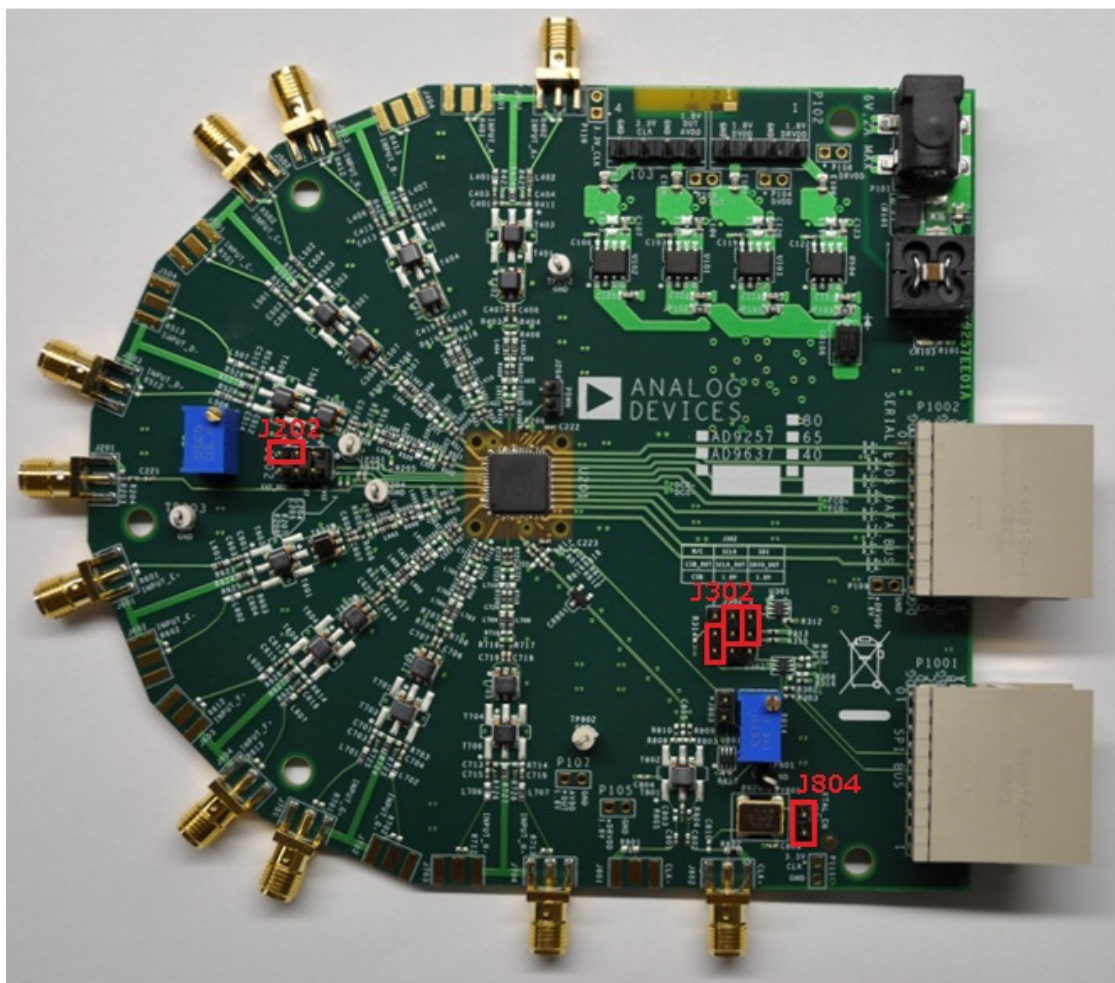
SOFTWARE NEEDED

- VisualAnalog
- SPIController

All documents and software are available at <http://www.analog.com> .
For any questions please send an email to highspeed.converters@analog.com.

TESTING

1. Install ADI VisualAnalog and SPIController software on a Windows PC. The installer for VisualAnalog is at ftp://ftp.analog.com/pub/HSSP_SW/VisualAnalog/VisualAnalog_Setup.exe . The installer for SPIController is at ftp://ftp.analog.com/pub/adispi/A2DComponents/Install/SPIController_Setup.exe . Complete the installation but please wait to start the software until the hardware is configured and powered up, as described below.
2. Connect the AD9257/AD9637 evaluation board and the HSC-ADC-EVALCZ board together as shown in Figure 1.
3. Connect one 6V, 2A power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD9257/AD9637 board.
4. Make sure a jumper is installed on header J9 at the 2.5V position on the HSC-ADC-EVALCZ evaluation board to set the FPGA I/O voltage to 2.5V. Connect one 6V, 2A power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
5. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable.
6. On the ADC evaluation board, make sure that jumpers are installed on headers J302, J804 and J202 as shown below for the default setup.



7. The AD9257/AD9637 Evaluation Board has a 65MHz/80MHz Valpey Fisher oscillator (VFAC3HL-65MHZ/VFAC3HL-80MHZ) which is enabled by default using the jumper on J804 (XTAL_EN). However, if the user wishes to provide another clock source, provide a clean, low-jitter clock source to connector J802 at the desired ADC conversion rate. Please remove J804 in order to override the built-in oscillator. The input clock level should be between 10dBm and 14dBm.
8. Start VisualAnalog software on the PC. The software should automatically detect the device on the evaluation board as shown in figure 2.

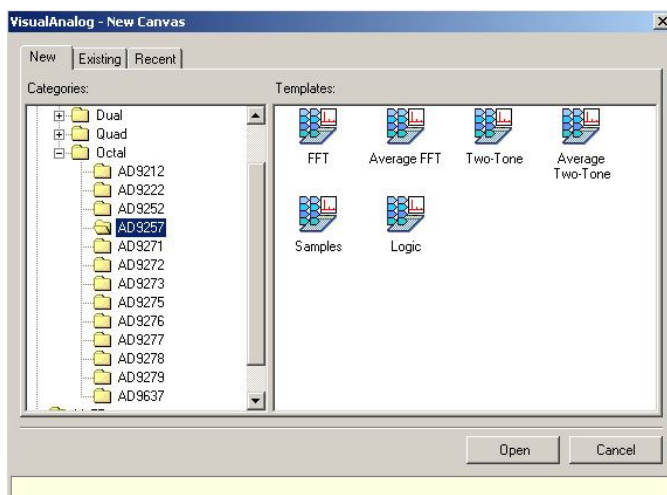
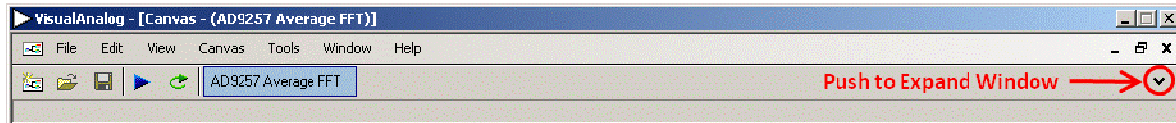


Figure 2. Visual Analog New Canvas window showing the AD9257/AD9637 device detected

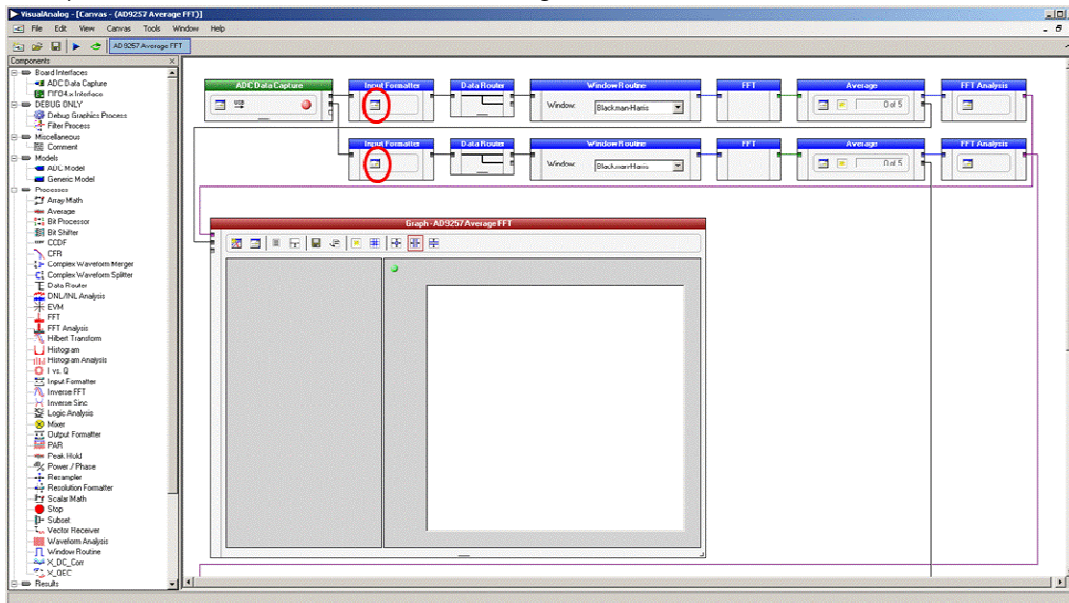
- Select the template that corresponds to the type of testing that needs to be performed. "Average FFT" is a good test to start with. Select "Yes" when Visual Analog prompts for programming the FPGA. The "Done" LED D6 should illuminate on the HSC-ADC-EVALCZ board indicating that the FPGA is correctly programmed.

You might see a window that looks like the following:



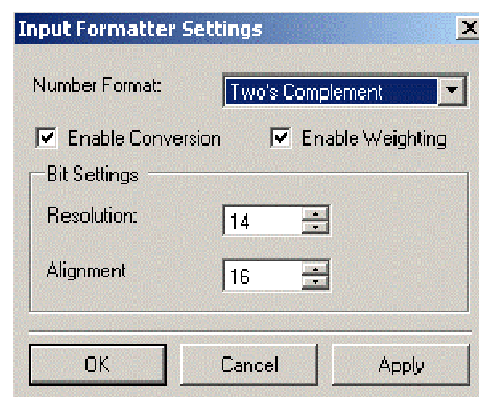
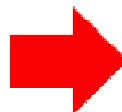
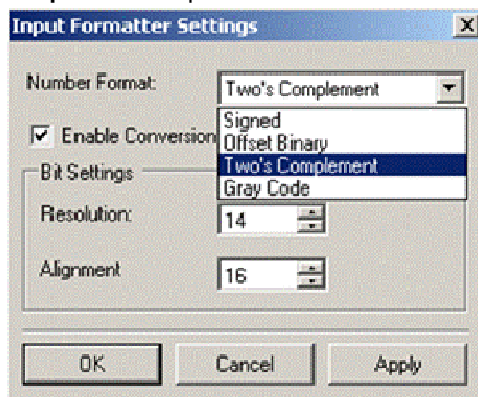
In this case, push the "v" icon on the right to expand the window.

The expanded window will look similar to the following:



Note that the GUI configuration shown above is for observing data from two of eight channels. More channels can be added by replicating (by copying and pasting) the VisualAnalog signal processing paths and their blocks.

Push the red circled icons in the top level GUI as shown above, to open the Input Formatter Settings Window. Select **Two's Complement** and push OK.



If VisualAnalog did not prompt for programming the FPGA and/or LED D6 on HSC-ADC-EVALCZ is not lit, click the Settings button on the left side of the ADC Data Capture block in the GUI, to bring up the ADC Data Capture Settings window. Click on the 'Capture Board' tab. In the FPGA box click on the Program button to configure the FPGA. LED D6 should now be lit.

- On the ADC evaluation board, use a signal generator with low phase noise and low distortion to provide an input signal to the analog input at connector J402 (Channel A), J403 (Channel B), J502 (Channel C), J503 (Channel D), J601 (Channel E), J604 (Channel

F), J701(Channel G), J704(Channel H). It is OK to provide signals to all eight channels simultaneously. Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator to the channel inputs. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency (ADI uses TTE, Allen Avionics, and K&L band-pass filters). In order for the input level to be near the ADC's full scale, the generator level should be set to 8dBm to 12dBm; this level depends on the input frequency, how many channels are simultaneously driven and any losses in bandpass filters.

11. Next, start the SPIController software. If prompted for a configuration file, select the configuration file titled AD9257_14Bit_65MSspiR03.cfg for AD9257 or AD9637_14Bit_80MSspiR03.cfg for AD9637. If not prompted, check the title bar of the window to see which configuration is loaded. If necessary, choose "Cfg Open" from the "File" menu and select the configuration file named above. Note that the CHIP ID(1) field may be filled whether the correct SPI Controller configuration file is loaded or not.
12. Click the New DUT button () in SPI Controller.

13. The SPI Controller window (shown in Figure 3) helps customize the AD9257/AD9637 to fit the data capture needs of the customer.

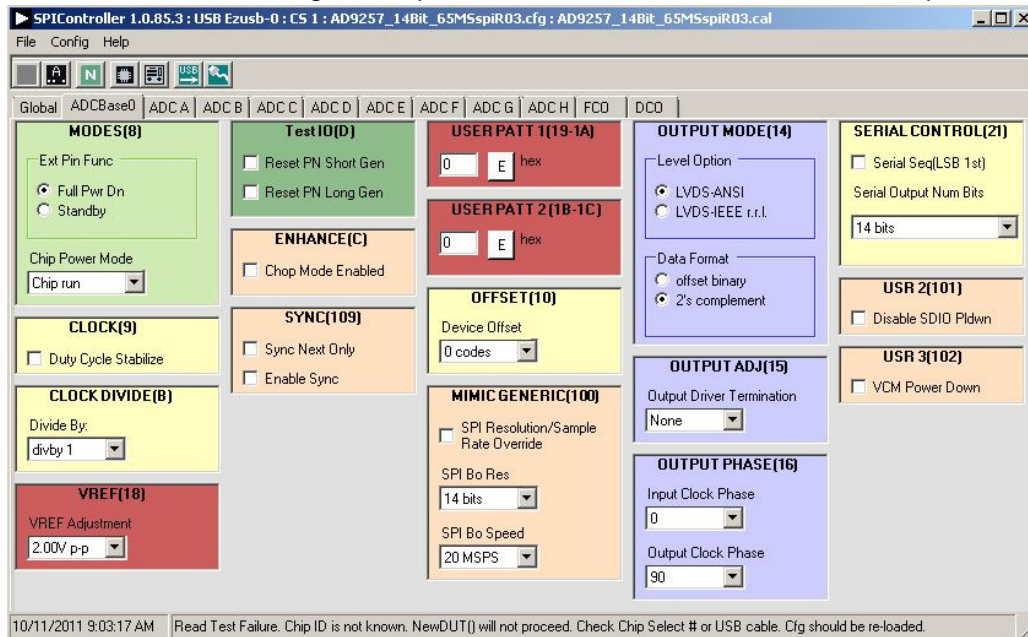


Figure 3. SPI Controller window for the AD9257/AD9637

14. In the SPIController ADCBase0 window shown in Figure 3, in the MODES(8) section in the upper left, push the arrow under “Chip Power Mode” to see the pull-down menu. Select “Reset”. The select “Chip run” in the same menu to restore the ADC to normal operation.
15. Click the Continuous Run button () in VisualAnalog to start data capture and enable viewing of the outputs.
16. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the “Fund Power” reading in the left panel of the VisualAnalog FFT window.)
17. If desired, click on File>Save Form as in the FFT window to save the FFT plot.

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

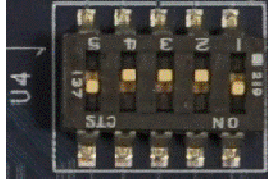
- If you see an abnormal noise floor, go to the ADCBase0 tab of the SPIController window and toggle the Chip Power Mode in MODES(8) from Chip Run to Reset and back.
- If the noise floor returns to normal when you disconnect the signal generator from the analog input, be sure that you are not overdriving the ADC. Reduce the input level if necessary.
- In VisualAnalog, click the Settings icon in the Input Formatter block. Check that Number Format is set to the same output format as is selected in SPIController (e.g. two's complement is selected in both VisualAnalog_InputFormatter AND SPIController ADCBase0 tab). Repeat for the other channels.

If the FFT appears normal but the performance is poor, check the following:

- Make sure that an appropriate filter is used on the analog input.
- Make sure that the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure that the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after Run in VisualAnalog (see Figure 11) is clicked, do the following:

- Make sure that the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure that the FPGA has been programmed by verifying that the D6 DONE LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated:
 - o Please go to the ADC Data Capture block in Visual Analog. Click on the settings icon on the left side. Go to the Capture Board tab and push the "Program" button on the right side.
 - o Please make sure that the U4 switch on the HSC-ADC-EVALCZ board is in the correct position for USB CONFIG.



- Make sure that the correct FPGA program was installed by clicking the Settings icon on the left side of the ADC Data Capture block in the VisualAnalog GUI to bring up the ADC Data Capture Settings window. Click on the 'Capture Board' tab. In the FPGA field verify that the proper FPGA bin file is selected for the part. It should be "Octal_High_Speed.bin". If sampling at less than 30Msps, "Octal_Low_Speed.bin" is supplied and installed in the same PC folder.
- Check that J9 on the HSC-ADC-EVALCZ has a jumper in the 2.5V position.

If VisualAnalog indicates that the FIFO Capture timed out, do the following:

- Make sure that all power and USB connections are secure.