

N-Channel and P-Channel Enhancement-Mode Dual MOSFET

Features

- 500V Breakdown Voltage
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdowns
- Low Input and Output Leakage
- Independent, Electrically Isolated N-channel and P-channel

Applications

- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers

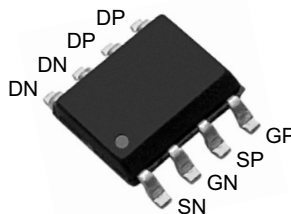
General Description

The TC1550 consists of a high-voltage N-channel and P-channel MOSFET in an 8-Lead SOIC package. It is an Enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where extremely low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

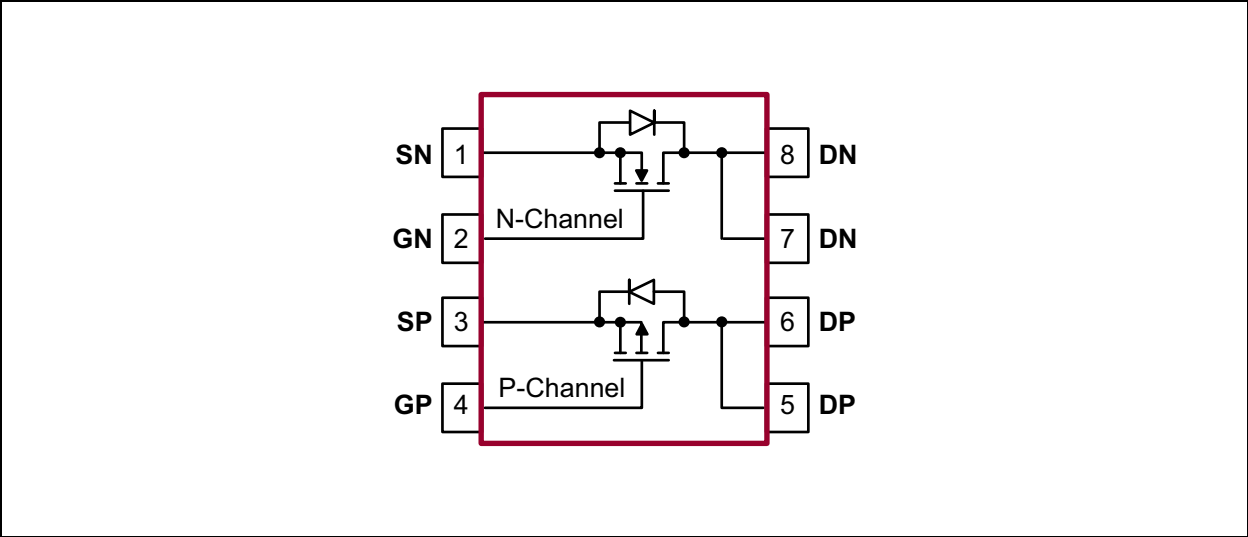
8-lead SOIC
(Top view)



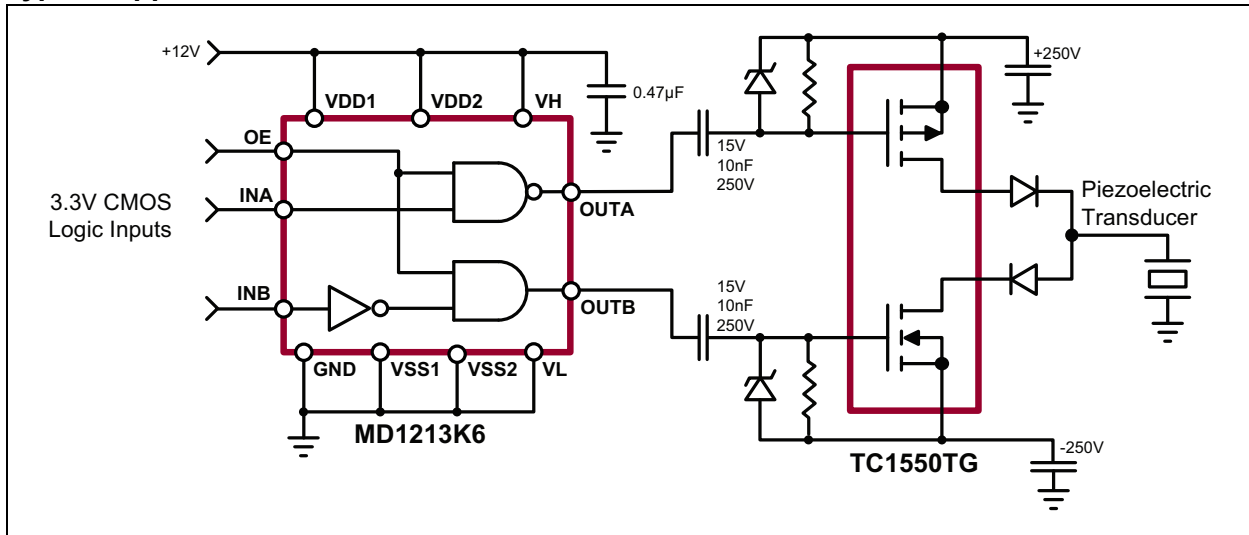
See [Table 2-1](#) for pin information.

TC1550

Functional Block Diagram



Typical Application Circuit



TC1550

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T _A = 25°C.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
N-CHANNEL						
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV _{DSS}	500	—	—	V	V _{GS} = 0V, I _D = 1 mA
Gate Threshold Voltage	V _{GS(th)}	2	—	4	V	V _{GS} = V _{DS} , I _D = 1 mA
Change in V _{GS(th)} with Temperature	ΔV _{GS(th)}	—	–3.8	–5	mV/°C	V _{GS} = V _{DS} , I _D = 1 mA (Note 2)
Gate Body Leakage Current	I _{GSS}	—	—	100	nA	V _{GS} = ±20V, V _{DS} = 0V
Zero-gate Voltage Drain Current	I _{DSS}	—	—	10	μA	V _{GS} = 0V, V _{DS} = Maximum rating
		—	—	1	mA	V _{DS} = 0.8 Maximum rating, V _{GS} = 0V, T _A = 125°C (Note 2)
On-state Drain Current	I _{D(ON)}	—	100	—	mA	V _{GS} = 5V, V _{DS} = 25V
		150	350	—		V _{GS} = 10V, V _{DS} = 25V
Static Drain-to-Source On-state Resistance	R _{DS(ON)}	—	45	—	Ω	V _{GS} = 5V, I _D = 50 mA
		—	40	60		V _{GS} = 10V, I _D = 50 mA
Change in R _{DS(ON)} with Temperature	ΔR _{DS(ON)}	—	1	1.7	%/°C	V _{GS} = 10V, I _D = 50 mA (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G _{FS}	50	100	—	mmho	V _{DS} = 25V, I _D = 50 mA
Input Capacitance	C _{ISS}	—	45	55	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C _{OSS}	—	8	10		
Reverse Transfer Capacitance	C _{RSS}	—	2	5		
Turn-on Delay Time	t _{d(ON)}	—	—	10	ns	V _{DD} = 25V, I _D = 150 mA, R _{GEN} = 25Ω
Rise Time	t _r	—	—	15		
Turn-off Delay Time	t _{d(OFF)}	—	—	10		
Fall Time	t _f	—	—	10		
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	0.8	—	V	V _{GS} = 0V, I _{SD} = 500 mA (Note 1)
Reverse Recovery Time	T _{rr}	—	300	—	ns	V _{GS} = 0V, I _{SD} = 500 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested and at $+25^{\circ}C$. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% sample tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T _A = 25°C.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
P-CHANNEL						
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV _{DSS}	−500	—	—	V	V _{GS} = 0V, I _D = −1 mA
Gate Threshold Voltage	V _{GS(th)}	−2	—	−4.5	V	V _{GS} = V _{DS} , I _D = −1 mA
Change in V _{GS(th)} with Temperature	ΔV _{GS(th)}	—	3.5	6	mV/°C	V _{GS} = V _{DS} , I _D = −1 mA (Note 2)
Gate Body Leakage Current	I _{GSS}	—	—	100	nA	V _{GS} = ±20V, V _{DS} = 0V
Zero-Gate Voltage Drain Current	I _{DSS}	—	—	−10	μA	V _{GS} = 0V, V _{DS} = Maximum rating
		—	—	−1	mA	V _{DS} = 0.8 Maximum rating V _{GS} = 0V, T _A = 125°C, (Note 2)
On-State Drain Current	I _{D(ON)}	—	−90	—	mA	V _{GS} = −5V, V _{DS} = −25V
		−100	−240	—		V _{GS} = −10V, V _{DS} = −25V
Static Drain-to-Source On-state Resistance	R _{DS(ON)}	—	85	—	Ω	V _{GS} = −5V, I _D = −5 mA
		—	80	125		V _{GS} = −10V, I _D = −10 mA
Change in R _{DS(ON)} with Temperature	ΔR _{DS(ON)}	—	0.85	—	%/°C	V _{GS} = −10V, I _D = −10mA (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G _{FS}	25	40	—	mmho	V _{DS} = −25V, I _D = −10 mA
Input Capacitance	C _{ISS}	—	40	70	pF	V _{GS} = 0V, V _{DS} = −25V, f = 1 MHz
Common-Source Output Capacitance	C _{OSS}	—	10	20		
Reverse Transfer Capacitance	C _{RSS}	—	3	10		
Turn-on Delay Time	t _{d(ON)}	—	5	10	ns	V _{DD} = −25V, I _D = −100 mA, R _{GEN} = 25Ω
Rise Time	t _r	—	8	10		
Turn-on Delay Time	t _{d(OFF)}	—	8	15		
Fall Time	t _f	—	5	16		
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	−0.8	−1.5	V	V _{GS} = 0V, I _{SD} = −100 mA (Note 1)
Reverse Recovery Time	t _{rr}	—	200	—	ns	V _{GS} = 0V, I _{SD} = −100 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested and at $+25^\circ\text{C}$. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% sample tested.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55°C	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55°C	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC	θ_{JA}	—	101	—	$^\circ\text{C/W}$	Note

Note 1: 1 oz, 4-layer, 3" x 4" PCB.

2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TC1550.
Refer to [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SN	Source N-Channel
2	GN	Gate N-Channel
3	SP	Source P-Channel
4	GP	Gate P-Channel
5	DP	Drain P-Channel
6	DP	Drain P-Channel
7	DN	Drain N-Channel
8	DN	Drain N-Channel

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC1550.

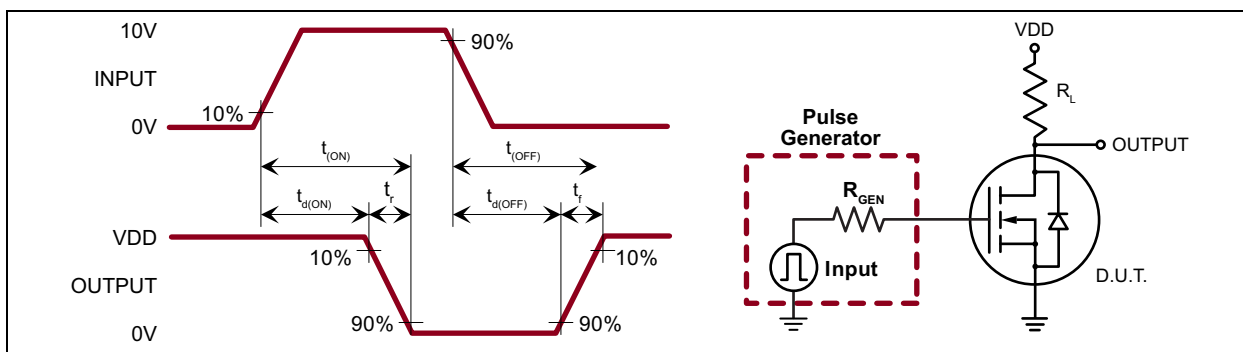


FIGURE 3-1: N-Channel Switching Waveforms and Test Circuit.

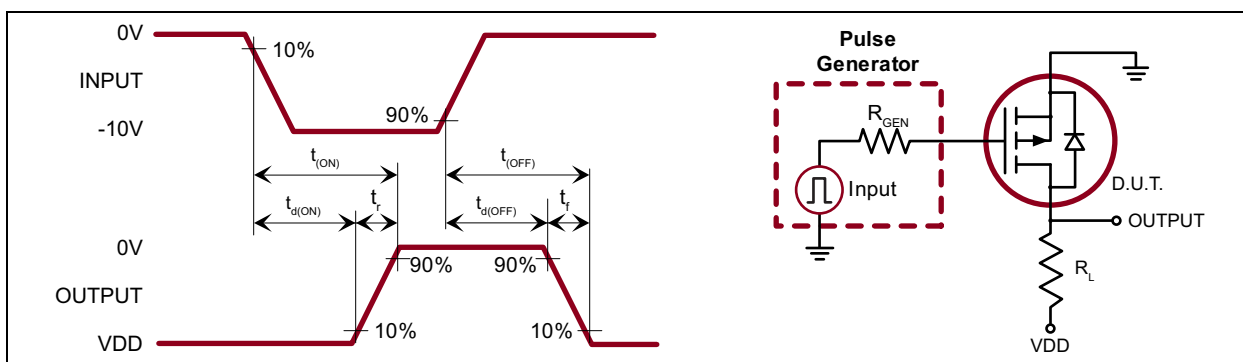


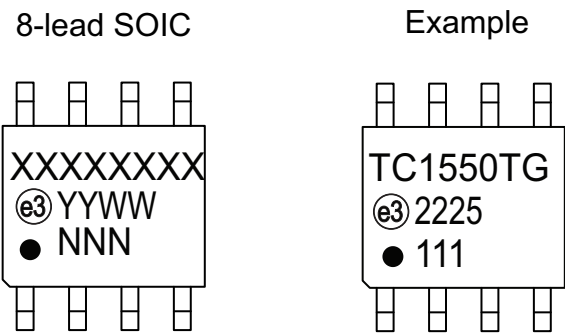
FIGURE 3-2: P-Channel Switching Waveforms and Test Circuit.

TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (Maximum) (Ω)	
N-Channel	P-Channel	N-Channel	P-Channel
500	-500	60	125

4.0 PACKAGING INFORMATION

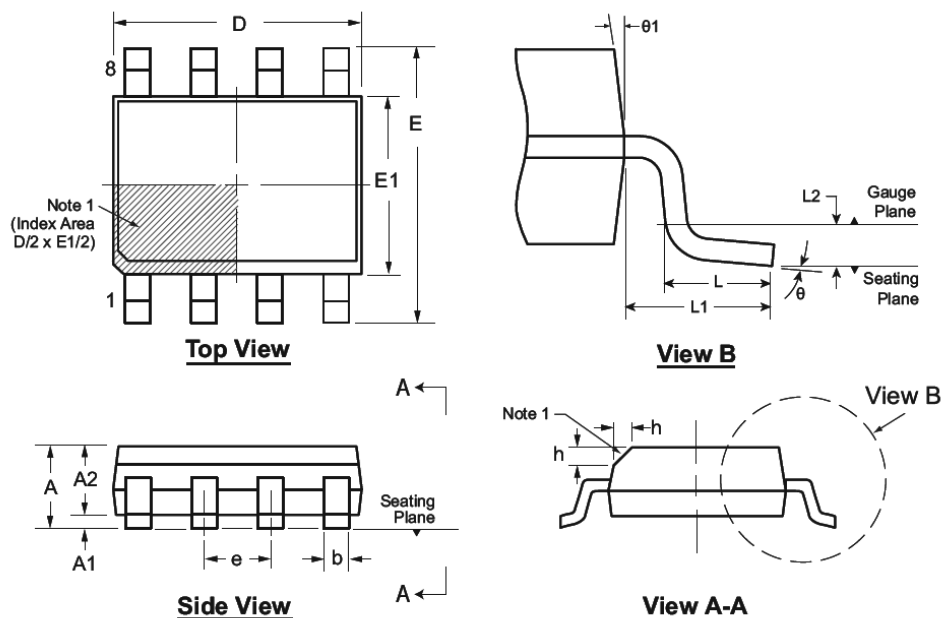
4.1 Package Marking Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

TC1550

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2022)

- Converted Supertex Doc# DSFP-TC1550 to Microchip DS20005773A
- Changed the package marking format
- Changed the packaging quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	TC1550	=	N-Channel and P-Channel Enhancement-Mode Dual MOSFET		
Package:	TG	=	8-lead SOIC		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3300/Reel for a TG Package		
Example:					
a) TC1550TG-G: N-Channel and P-Channel Enhancement-Mode Dual MOSFET, 8-lead SOIC, 3300/Reel					

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