# LM5025C Active Clamp Voltage Mode PWM Controller

**Check for Samples: LM5025C**

## FEATURES

- **Internal Start-Up Bias Regulator**
- **3A Compound Main Gate Driver**
- **Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis**
- **Voltage Mode Control with Feed-Forward**
- **Adjustable Dual Mode Over-Current Protection**
- **Programmable Overlap or Deadtime between the Main and Active Clamp Outputs**
- **Volt x Second Clamp**
- **Programmable Soft-start**
- **Leading Edge Blanking**
- **Single Resistor Programmable Oscillator**
- **Oscillator UP / DOWN Sync Capability**
- **Precision 5V Reference**
- **Thermal Shutdown**

## PACKAGE

- **TSSOP-16**

## DESCRIPTION

The LM5025C is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025C are: The maximum duty cycle of the LM5025C is increased from 80% to 91%. The soft-start capacitor charging current is increased from 20 µA to 90 µA. The $V_{CC}$ regulator current limit threshold is increased from 25 mA to 55 mA. The CS1 and CS2 current limit thresholds have been increased to 0.5V. The internal CS2 filter discharge device has been disabled and no longer operates each clock cycle. The internal $V_{CC}$ and $V_{REF}$ regulators continue to operate when the line UVLO pin is below threshold.

The LM5025C PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp / Reset technique. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1MHz and total PWM and current sense propagation delays less than 100 ns. The LM5025C includes a high-voltage start-up regulator that operates over a wide input range of 13V to 90V. Additional features include: Line Under Voltage Lockout (UVLO), softstart, oscillator UP/DOWN sync capability, precision reference and thermal shutdown.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Application Circuit

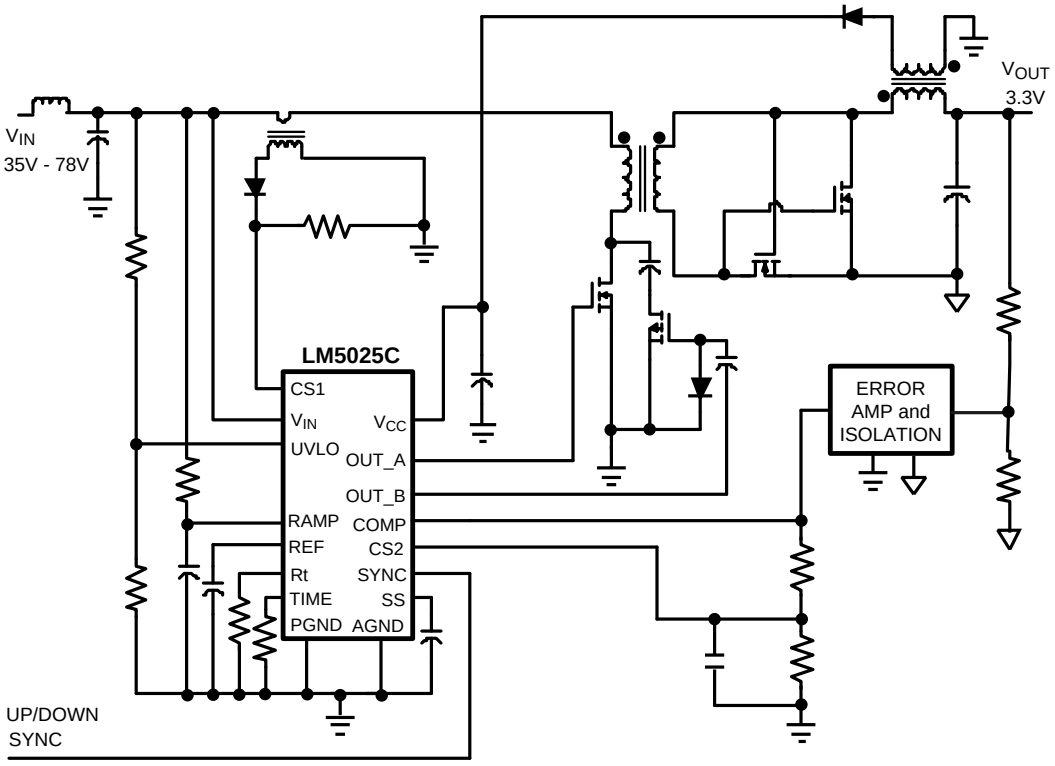



**Figure 1. Simplified Active Clamp Forward Power Converter**


Copyright © 2008–2013, Texas Instruments Incorporated

## Connection Diagram

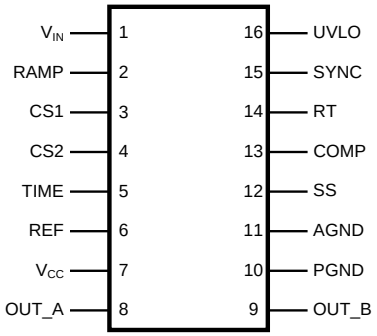



**Figure 2. 16-Lead TSSOP**
**Package Number PW0016A**

### PIN DESCRIPTIONS

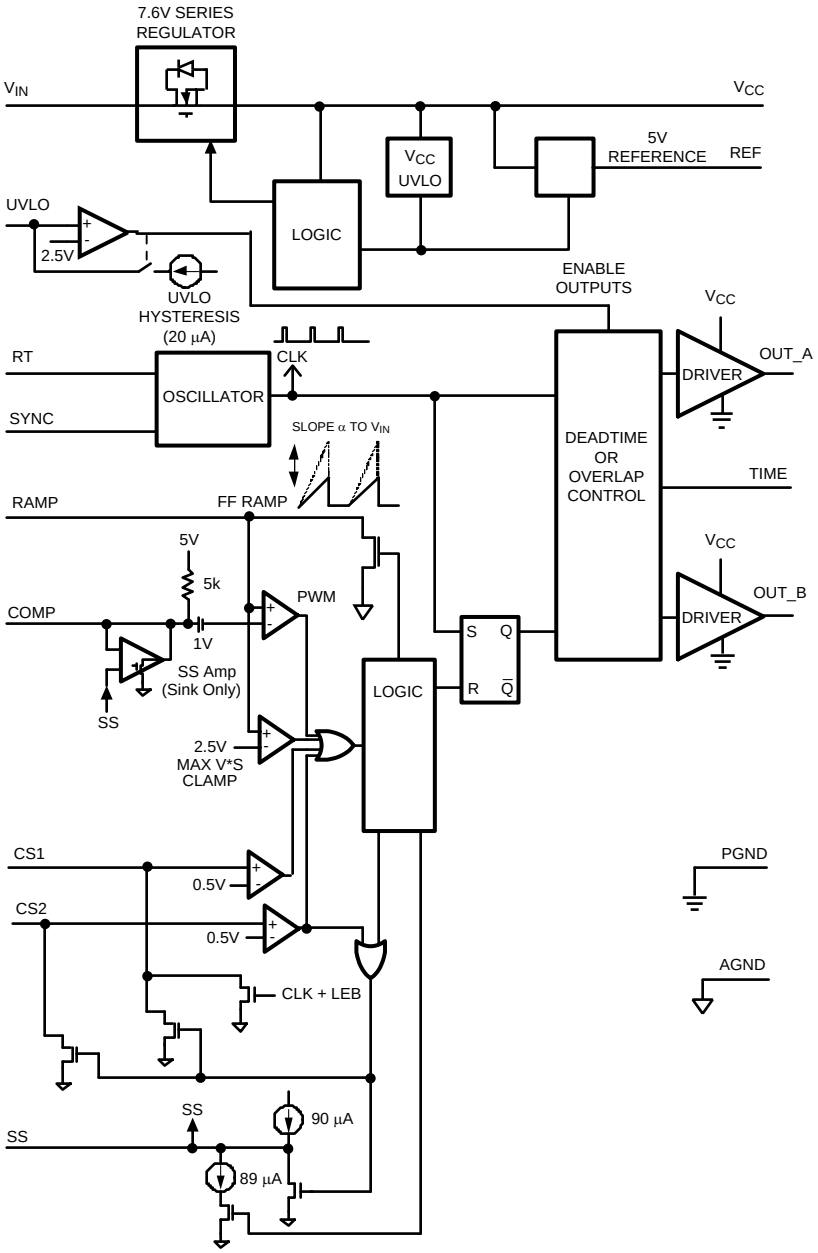
| Pin | Name | Description | Application Information |
|---|---|---|---|
| 1 | $V_{IN}$ | Source Input Voltage | Input to start-up regulator. Input range 13V to 90V, with transient capability to 105V. |
| 2 | RAMP | Modulator ramp signal | An external RC circuit from Vin sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET, initiated by either the internal clock or the V*Sec Clamp comparator. |
| 3 | CS1 | Current sense input for cycle-by-cycle limiting | If CS1 exceeds 0.5V the outputs will go into Cycle-by-Cycle current limit. CS1 is held low for 50ns after OUT_A switches high providing leading edge blanking. |
| 4 | CS2 | Current sense input for soft restart | If CS2 exceeds 0.5V the outputs will be disabled and a softstart commenced. The soft-start capacitor will be fully discharged and then released with a pull-up current of 1µA. After the first output pulse (when SS =1V), the SS charge current will revert back to 90 µA. |
| 5 | TIME | Output overlap/Deadtime control | An external resistor ($R_{SET}$) sets either the overlap time or dead time for the active clamp output. An $R_{SET}$ resistor connected between TIME and GND produces in-phase OUT_A and OUT_B pulses with overlap. An $R_{SET}$ resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime. |
| 6 | REF | Precision 5 volt reference output | Maximum output current: 10 mA Locally decouple with a 0.1 µF capacitor. Reference stays low until the $V_{CC}$ UV comparator is satisfied. |
| 7 | $V_{CC}$ | Output from the internal high voltage start-up regulator. The $V_{CC}$ voltage is regulated to 7.6V. | If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, reducing the IC power dissipation. |
| 8 | OUT_A | Main output driver | Output of the main switch PWM output gate driver. Output capability of 3A peak sink current. |
| 9 | OUT_B | Active Clamp output driver | Output of the Active Clamp switch gate driver. Capable of 1.25A peak sink current.. |
| 10 | PGND | Power ground | Connect directly to analog ground. |
| 11 | AGND | Analog ground | Connect directly to power ground. |
| 12 | SS | Soft-start control | An external capacitor and an internal 90 µA current source set the softstart ramp. The SS current source is reduced to 1 µA initially following a CS2 over-current event or an over temperature event. |
| 13 | COMP | Input to the Pulse Width Modulator | An internal 5 kΩ resistor pull-up is provided on this pin. The external opto-coupler sinks current from COMP to control the PWM duty cycle. |
| 14 | RT | Oscillator timing resistor pin | An external resistor connected from RT to ground sets the internal oscillator frequency. |

Copyright © 2008–2013, Texas Instruments Incorporated

**PIN DESCRIPTIONS (continued)**

| Pin | Name | Description | Application Information |
|---|---|---|---|
| 15 | SYNC | Oscillator UP/DOWN synchronization input | The internal oscillator can be synchronized to an external clock with a frequency 20% lower than the internal oscillator's free running frequency. There is no constraint on the maximum sync frequency. |
| 16 | UVLO | Line Under-Voltage shutdown | An external voltage divider from the power source sets the shutdown comparator levels. The comparator threshold is 2.5V. Hysteresis is set by an internal current source (20 µA) that is switched on or off as the UVLO pin potential crosses the 2.5V threshold. |

## Block Diagram





Copyright © 2008–2013, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | |
|---|---|
| $V_{IN}$ to GND | -0.3V to 105V |
| $V_{CC}$ to GND | -0.3V to 16V |
| CS1, CS2 to GND | -0.3 to 1.00V |
| All other inputs to GND | -0.3 to 7V |
| ESD Rating (3) | |
| Human Body Model | 2kV |
| Storage Temperature Range | -55°C to 150°C |
| Junction Temperature | 150°C |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) For detailed information on soldering plastic TSSOP package, refer to the Packaging Data Book available from Texas Instruments.

## Operating Ratings (1)

| | |
|---|---|
| $V_{IN}$ Voltage | 13 to 90V |
| External Voltage Applied to $V_{CC}$ | 8 to 15V |
| Operating Junction Temperature | -40°C to +125°C |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

## Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 32 kΩ, $R_{SET}$ = 27.4 kΩ) unless otherwise stated (1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Startup Regulator** | | | | | | |
| $V_{CC}$ Reg | $V_{CC}$ Regulation | No Load | **7.3** | 7.6 | **7.9** | V |
| | $V_{CC}$ Current Limit | (2) | **40** | 55 | | mA |
| I-$V_{IN}$ | Startup Regulator Leakage (external Vcc Supply) | $V_{IN}$ = 100V | | 165 | **500** | µA |
| **$V_{CC}$ Supply** | | | | | | |
| | $V_{CC}$ Under-voltage Lockout Voltage (positive going $V_{cc}$) | | **$V_{CC}$ Reg - 220mV** | $V_{CC}$ Reg - 120mV | | V |
| | $V_{CC}$ Under-voltage Hysteresis | | **1.0** | 1.5 | **2.0** | V |
| | $V_{CC}$ Supply Current ($I_{CC}$) | $C_{gate}$ = 0 | | | **4.2** | mA |
| **Reference Supply** | | | | | | |
| $V_{REF}$ | Ref Voltage | $I_{REF}$ = 0 mA | **4.85** | 5 | **5.15** | V |
| | Ref Voltage Regulation | $I_{REF}$ = 0 to 10 mA | | 25 | **50** | mV |
| | Ref Current Limit | | **10** | 20 | | mA |
| **Current Limit** | | | | | | |
| CS1 Prop | CS1 Delay to Output | CS1 Step from 0 to 0.6V Time to onset of OUT Transition (90%) $C_{gate}$ = 0 | | 40 | | ns |

(1) All electrical characteristics having room temperature limits are tested during production with $T_A$ = $T_J$ = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Device thermal limitations may limit usable range.

Copyright © 2008–2013, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Specifications with standard typeface are for $T_J$ = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 32 kΩ, $R_{SET}$ = 27.4 kΩ) unless otherwise stated (1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CS2 Prop | CS2 Delay to Output | CS2 Step from 0 to 0.6V Time to onset of OUT Transition (90%) $C_{gate}$ = 0 | | 50 | | ns |
| | Cycle by Cycle Threshold Voltage (CS1) | | **0.45** | 0.5 | **0.55** | V |
| | Cycle Skip Threshold Voltage (CS2) | Resets SS capacitor; auto restart | **0.45** | 0.5 | **0.55** | V |
| | Leading Edge Blanking Time (CS1) | | | 50 | | ns |
| | CS1 Sink Impedance (clocked) | CS1 = 0.4V | | 30 | **50** | Ω |
| | CS1 Sink Impedance (Post Fault Discharge) | CS1 = 0.6V | | 15 | **30** | Ω |
| | CS2 Sink Impedance (Post Fault Discharge) | CS2 = 0.6V | | 55 | **85** | Ω |
| | CS1 and CS2 Leakage Current | CS = CS Threshold - 100mV | | | **1** | µA |
| **Soft-Start** | | | | | | |
| | Soft-start Current Source Normal | | **65** | 90 | **115** | µA |
| | Soft-start Current Source following a CS2 event | | **0.5** | 1 | **1.5** | µA |
| **Oscillator** | | | | | | |
| | Frequency1 | $T_A$ = 25°C<br>$T_J = T_{low}$ to $T_{high}$ | 180<br>**175** | 200 | 220<br>**225** | kHz |
| | Frequency2 | RT = 10.8 kΩ | **510** | 580 | **650** | kHz |
| | Sync threshold | | | 2 | | V |
| | Min Sync Pulse Width | | | | **100** | ns |
| | Sync Frequency Range | | **160** | | | kHz |
| **PWM Comparator** | | | | | | |
| | Delay to Output | COMP step 5V to 0V Time to onset of OUT_A transition low | | 40 | | ns |
| | Duty Cycle Range | | **0** | | **91** | % |
| | COMP to PWM Offset | | **0.7** | 1 | **1.3** | V |
| | COMP Open Circuit Voltage | | **4.3** | | **5.9** | V |
| | COMP Short Circuit Current | COMP = 0V | **0.6** | 1 | **1.4** | mA |
| **Volt x Second Clamp** | | | | | | |
| | Ramp Clamp Level | Delta RAMP measured from onset of OUT_A to Ramp peak. COMP = 5V | **2.4** | 2.5 | **2.6** | V |
| **UVLO Shutdown** | | | | | | |
| | Undervoltage Shutdown Threshold | | **2.44** | 2.5 | **2.56** | V |
| | Undervoltage Shutdown Hysteresis | | **16** | 20 | **24** | µA |
| **Output Section** | | | | | | |
| | OUT_A High Saturation | MOS Device @ Iout = -10mA, | | 5 | **10** | Ω |


Copyright © 2008–2013, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Specifications with standard typeface are for $T_J$ = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. $V_{IN}$ = 48V, $V_{CC}$ = 10V, RT = 32 kΩ, $R_{SET}$ = 27.4 kΩ) unless otherwise stated (1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | OUTPUT_A Peak Current Sink | Bipolar Device @ Vcc/2 | | 3 | | A |
| | OUT_A Low Saturation | MOS Device @ Iout = 10mA, | | 6 | **9** | Ω |
| | OUTPUT_A Rise Time | $C_{gate}$ = 2.2nF | | 20 | | ns |
| | OUTPUT_A Fall Time | $C_{gate}$ = 2.2nF | | 15 | | ns |
| | OUT_B High Saturation | MOS Device @ Iout = -10mA, | | 10 | **20** | Ω |
| | OUTPUT_B Peak Current Sink | Bipolar Device @ Vcc/2 | | 1 | | A |
| | OUT_B Low Saturation | MOS Device @ Iout = 10mA, | | 12 | **18** | Ω |
| | OUTPUT_B Rise Time | $C_{gate}$ = 1nF | | 20 | | ns |
| | OUTPUT_B Fall Time | $C_{gate}$ = 1nF | | 15 | | ns |
| **Output Timing Control** | | | | | | |
| | Overlap Time | $R_{SET}$ = 38 kΩ connected to GND, 50% to 50% transitions | **75** | 105 | **135** | ns |
| | Deadtime | $R_{SET}$ = 29.5 kΩ connected to REF, 50% to 50% transitions | **75** | 105 | **135** | ns |
| **Thermal Shutdown** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold | | | 165 | | °C |
| | Thermal Shutdown Hysteresis | | | 25 | | °C |
| **Thermal Resistance** | | | | | | |
| $\theta_{JA}$ | Junction to Ambient | PW0016A Package | | 125 | | °C/W |

Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics

**$V_{CC}$ Regulator Start-up Characteristics, $V_{CC}$ vs Vin**

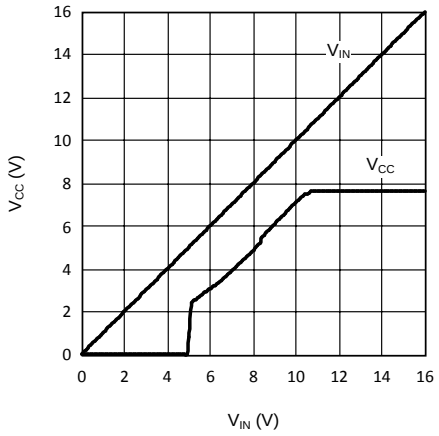



**Figure 3.**

**$V_{CC}$ vs $I_{CC}$**

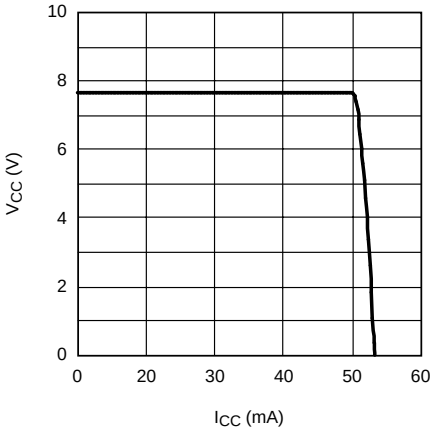



**Figure 4.**

**$V_{REF}$ vs $I_{REF}$**

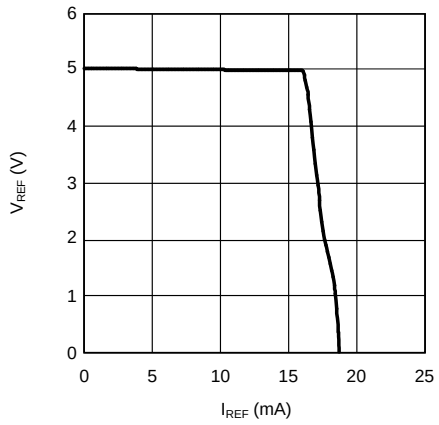



**Figure 5.**

**Oscillator Frequency vs RT**

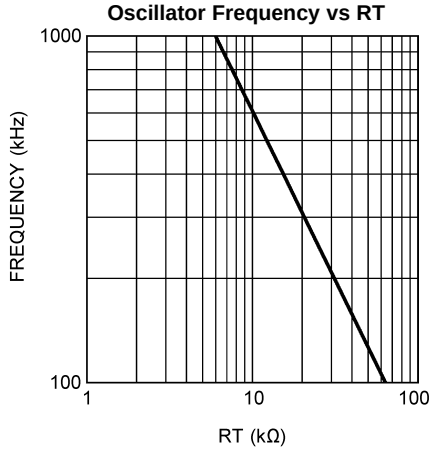



**Figure 6.**

**Overlap Time vs $R_{SET}$**

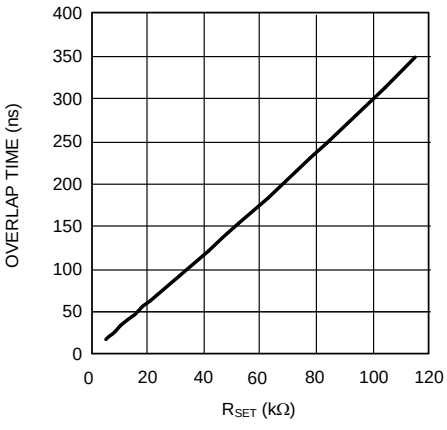



**Figure 7.**

**Overlap Time vs Temperature**
**$R_{SET}$ = 38K**

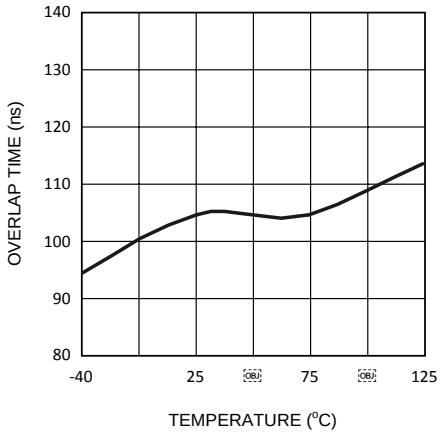



**Figure 8.**


Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

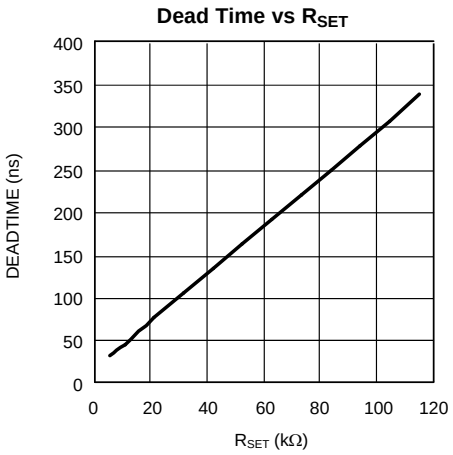



**Figure 9.**

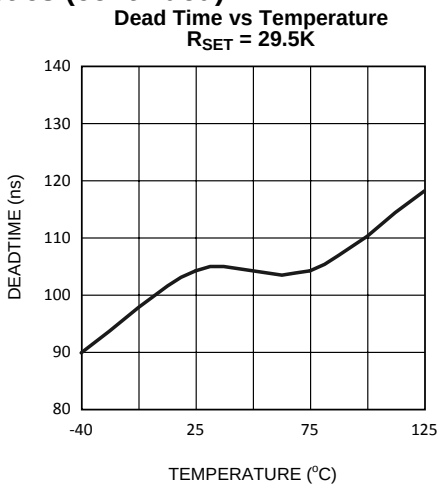



**Figure 10.**

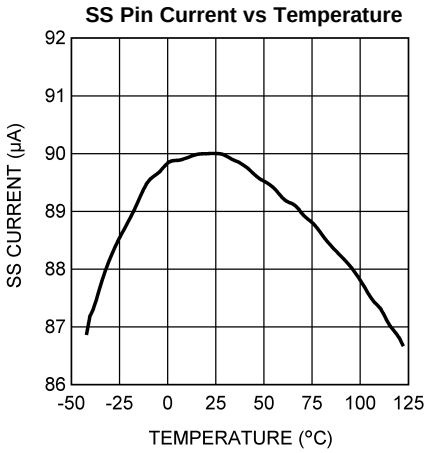



**Figure 11.**

## DETAILED OPERATING DESCRIPTION

The LM5025C is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025C are:

The maximum duty cycle of the LM5025C is increased from 80% to 91%. The soft-start capacitor charging current is increased from 20 µA to 90 µA. The $V_{CC}$ regulator current limit threshold is increased from 25 mA to 55 mA.

The CS1 and CS2 current limit thresholds have been increased to 0.5V (same as LM5025A).

The internal CS2 filter discharge device has been disabled and no longer operates each clock cycle (same as LM5025A).

The internal $V_{CC}$ and $V_{REF}$ regulators continue to operate when the line UVLO pin is below threshold (same as LM5025A).

The LM5025C PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp Reset technique. The device can be configured to control either a P-Channel clamp switch or an N-Channel clamp switch. With the active clamp technique higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The active clamp output can be configured for either a specified overlap time (for P-Channel switch applications) or a specified dead time (for N_Channel applications). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1MHz and total PWM and current sense propagation delays less than 100ns. The LM5025C includes a high-voltage start-up regulator that operates over a wide input range of 13V to 90V. Additional features include: Line Under Voltage Lockout (UVLO), softstart, oscillator UP/DOWN sync capability, precision reference and thermal shutdown.

### High Voltage Start-Up Regulator

The LM5025C contains an internal high voltage start-up regulator that allows the input pin ($V_{IN}$) to be connected directly to the line voltage. The regulator output is internally current limited to 55 mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the $V_{CC}$ pin. The recommended capacitance range for the $V_{CC}$ regulator is 0.1 µF to 100 µF. When the voltage on the $V_{CC}$ pin reaches the regulation point of 7.6V and the internal voltage reference (REF) reaches its regulation point of 5V, the controller outputs are enabled. The outputs will remain enabled until $V_{CC}$ falls below 6.2V or the line Under Voltage Lock Out detector indicates that $V_{IN}$ is out of range. In typical applications, an auxiliary transformer winding is connected through a diode to the $V_{CC}$ pin. This winding must raise the $V_{CC}$ voltage above 8V to shut off the internal start-up regulator. Powering $V_{CC}$ from an auxiliary winding improves efficiency while reducing the controller power dissipation.

When the converter auxiliary winding is inactive, external current draw on the $V_{CC}$ line should be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the $V_{CC}$ and the $V_{IN}$ pins together and feeding the external bias voltage into the two pins.

### Line Under-Voltage Detector

The LM5025C contains a line Under Voltage Lock Out (UVLO) circuit. An external set-point voltage divider from Vin to GND, sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 2.5V when Vin is in the desired operating range. If the undervoltage threshold is not met, both outputs are disabled,all other functions of the controller remain active. UVLO hysteresis is accomplished with an internal 20 uA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. Pulling the UVLO pin below the 2.5V threshold disables the PWM outputs.


Copyright © 2008–2013, Texas Instruments Incorporated

## PWM Outputs

The relative phase of the main (OUT_A) and active clamp outputs (OUT_B) can be configured for the specific application. For active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase with the active clamp output overlapping the main output. For active clamp configurations utilizing a high side N-Channel switch, the active clamp output should be out of phase with main output and there should be a dead time between the two gate drive pulses. A distinguishing feature of the LM5025C is the ability to accurately configure either dead time (both off) or overlap time (both on) of the gate driver outputs. The overlap / deadtime magnitude is controlled by the resistor value connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or GND for overlap control. The internal configuration detector senses the connection and configures the phase relationship of the main and active clamp outputs. The magnitude of the overlap/dead time can be calculated as follows:

- Overlap Time (ns) = 2.8 x $R_{SET}$ - 1.2
- Dead Time (ns) = 2.9 x $R_{SET}$ +20
- $R_{SET}$ in kΩ, Time in ns

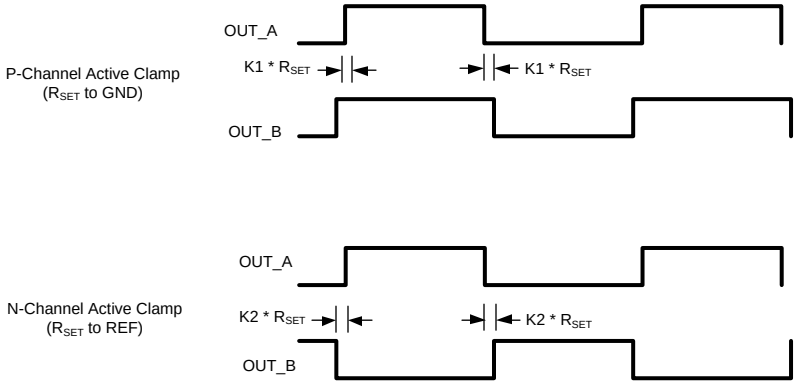
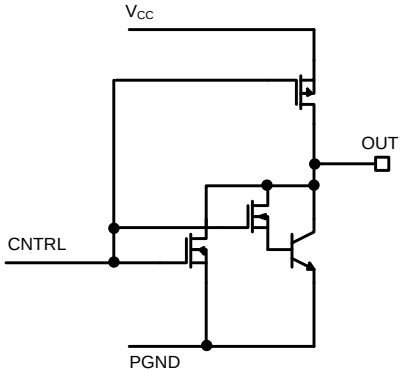



**Figure 12. Active Clamp Configurations**

## Compound Gate Drivers

The LM5025C contains two unique compound gate drivers, which parallel both MOS and Bipolar devices to provide high drive current throughout the entire switching event. The Bipolar device provides most of the drive current capability and provides a relatively constant sink current which is ideal for driving large power MOSFETs. As the switching event nears conclusion and the Bipolar device saturates, the internal MOS device continues to provide a low impedance to compete the switching event.

During turn-off at the Miller plateau region, typically around 2V - 3V, is where gate driver current capability is needed most. The resistive characteristics of all MOS gate drivers are adequate for turn-on since the supply to output voltage differential is fairly large at the Miller region. During turn-off however, the voltage differential is small and the current source characteristic of the Bipolar gate driver is beneficial to provide fast drive capability.




Copyright © 2008–2013, Texas Instruments Incorporated

## PWM Comparator

The PWM comparator compares the ramp signal (RAMP) to the loop error signal (COMP). This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The internal 5kΩ pull-up resistor, connected between the internal 5V reference and COMP, can be used as the pull-up for an optocoupler. The comparator polarity is such that 0V on the COMP pin will produce a zero duty cycle on both gate driver outputs.

## Volt Second Clamp

The Volt x Second Clamp comparator compares the ramp signal (RAMP) to a fixed 2.5V reference. By proper selection of RFF and CFF, the maximum ON time of the main switch can be set to the desired duration. The ON time set by Volt x Second Clamp varies inversely with the line voltage because the RAMP capacitor is charged by a resistor connected to Vin while the threshold of the clamp is a fixed voltage (2.5V). An example will illustrate the use of the Volt x Second Clamp comparator to achieve a 50% duty cycle limit, at 200 kHz, at a 48V line input: A 50% duty cycle at a 200 kHz requires a 2.5 µs of ON time. At 48V input the Volt x Second product is 120V x µs (48V x 2.5µs). To achieve this clamp level:

$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5V$

- Select $C_{FF}$ = 470 pF
- $R_{FF}$ = 102kΩ (1)

$48 \times 2.5\mu / 2.5 = 48\mu$ (2)

The recommended capacitor value range for CFF is 100 pF to 1000 pF.

The $C_{FF}$ ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the internal clock or by the V x S Clamp comparator, whichever event occurs first.

## Current Limit

The LM5025C contains two modes of over-current protection. If the sense voltage at the CS1 input exceeds 0.5V the present power cycle is terminated (cycle-by-cycle current limit). If the sense voltage at the CS2 input exceeds 0.5V, the controller will terminate the present cycle, discharge the softstart capacitor and reduce the softstart current source to 1 µA. The softstart (SS) capacitor is released after being fully discharged and slowly charges with a 1 µA current source. When the voltage at the SS pin reaches approximately 1V, the PWM comparator will produce the first output pulse at OUT_A. After the first pulse occurs, the softstart current source will revert to the normal 90 µA level. Fully discharging and then slowly charging the SS capacitor protects a continuously over-loaded converter with a low duty cycle hiccup mode.

These two modes of over-current protection allow the user great flexibility to configure the system behavior in over-load conditions. If it is desired for the system to act as a current source during an over-load, then the CS1 cycle-by-cycle current limiting should be used. In this case the current sense signal should be applied to the CS1 input and the CS2 input should be grounded. If during an overload condition it is desired for the system to briefly shutdown, followed by softstart retry, then the CS2 hiccup current limiting mode should be used. In this case the current sense signal should be applied to the CS2 input and the CS1 input should be grounded. This shutdown / soft-start retry will repeat indefinitely while the over-load condition remains. The hiccup mode will greatly reduce the thermal stresses to the system during heavy overloads. The cycle-by-cycle mode will have higher system thermal dissipations during heavy overloads, but provides the advantage of continuous operation for short duration overload conditions.

It is possible to utilize both over-current modes concurrently, whereby slight overload conditions activate the CS1 cycle-by-cycle mode while more severe overloading activates the CS2 hiccup mode. Generally the CS1 input will always be configured to monitor the main switch FET current each cycle. The CS2 input can be configured in several different ways depending upon the system requirements.

a. The CS2 input can also be set to monitor the main switch FET current except scaled to a higher threshold than CS1.
b. An external over-current timer can be configured which trips after a pre-determined over-current time, driving the CS2 input high, initiating a hiccup event.
c. In a closed loop voltage regulaton system, the COMP input will rise to saturation when the cycle-by-cycle current limit is active. An external filter/delay timer and voltage divider can be configured between the COMP pin and the CS2 pin to scale and delay the COMP voltage. If the CS2 pin voltage reaches 0.5V a hiccup event will initiate.


Copyright © 2008–2013, Texas Instruments Incorporated

A small RC filter, located near the controller, is recommended for each of the CS pins. The CS1 input has an internal FET which discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance. This same FET remains on an additional 50ns at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal. The CS2 discharge FET only operates following a CS2 event, UVLO and thermal shutdown.

The LM5025C CS comparators are very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network , which should be located close to the IC. If a sense resistor in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the IC GND and a single connection should be made to the power ground (sense resistor ground point).

## Oscillator and Sync Capability

The LM5025C oscillator is set by a single external resistor connected between the RT pin and GND. To set a desired oscillator frequency (F), the necessary RT resistor can be calculated from:

$$RT = (6002/F)^{1.0192} \quad (3)$$

where

- F is in kHz
- RT in kΩ

The RT resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND).

A unique feature of LM5025C is the ability to synchronize the oscillator to an external clock with a frequency that is either higher or lower than the frequency of the internal oscillator. The lower frequency sync frequency range is 91% of the free running internal oscillator frequency. There is no constraint on the maximum SYNC frequency. A minimum pulse width of 100 ns is required for the synchronization clock . If the synchronization feature is not required, the SYNC pin should be connected to GND to prevent any abnormal interference . The internal oscillator can be completely disabled by connecting the RT pin to REF. Once disabled, the sync signal will act directly as the master clock for the controller. Both the frequency and the maximum duty cycle of the PWM controller can be controlled by the SYNC signal (within the limitations of the Volt x Second Clamp). The maximum duty cycle (D) will be (1-D) of the SYNC signal.

## Feed-Forward Ramp

An external resistor ($R_{FF}$) and capacitor ($C_{FF}$) connected to $V_{IN}$ and GND are required to create the PWM ramp signal. The slope of the signal at the RAMP pin will vary in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal at the COMP pin by the pulse width modulator comparator to control the duty cycle of the main switch output. The Volt Second Clamp comparator also monitors the RAMP pin and if the ramp amplitude exceeds 2.5V the present cycle is terminated. The ramp signal is reset to GND at the end of each cycle by either the internal clock or the Volt Second comparator, which ever occurs first.

Copyright © 2008–2013, Texas Instruments Incorporated

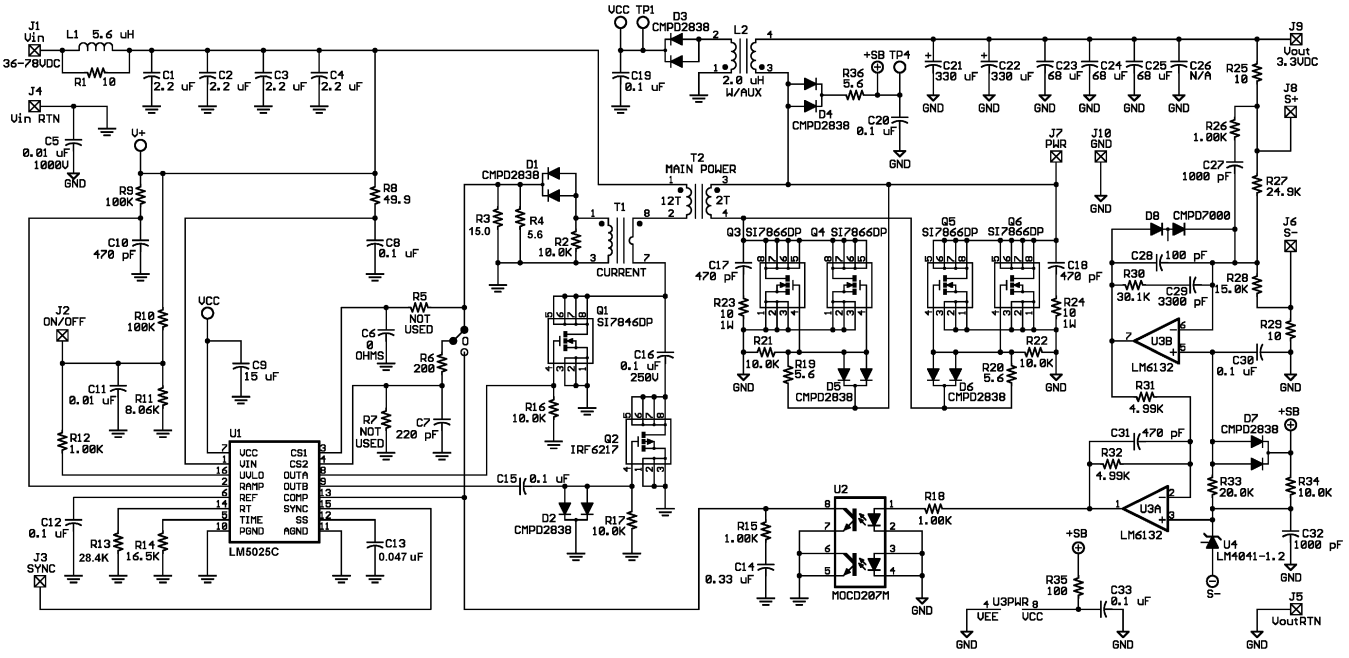
## Soft-Start

The softstart feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. At power on, a 90 µA current is sourced out of the softstart pin (SS) into an external capacitor. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and therefore the PWM duty cycle. In the event of a fault as determined by $V_{CC}$ undervoltage, line undervoltage (UVLO) or second level current limit, the output gate drivers are disabled and the softstart capacitor is fully discharged. When the fault condition is no longer present a softstart sequence will be initiated. Following a second level current limit detection (CS2), the softstart current source is reduced to 1 µA until the first output pulse is generated by the PWM comparator. The current source returns to the nominal 90 µA level after the first output pulse (~1V at the SS pin).

## Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart after the thermal hysteresis (typically 25°C). During a restart after thermal shutdown, the softstart capacitor will be fully discharged and then charged in the low current mode (1 µA) similar to a second level current limit event. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

## Application Circuit: Input 36-78V, Output 3.3V, 30A





Copyright © 2008–2013, Texas Instruments Incorporated

## REVISION HISTORY

| Changes from Revision B (March 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 14 |

Copyright © 2008–2013, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM5025CMTC/NOPB | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 125 | L5025C MTC |
| LM5025CMTCE/NOPB | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 125 | L5025C MTC |
| LM5025CMTCX/NOPB | Active | Production | TSSOP (PW) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L5025C MTC |
| LM5025CMTCX/NOPB.A | Active | Production | TSSOP (PW) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L5025C MTC |
| LM5025CMTCX/NOPB.B | Active | Production | TSSOP (PW) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | L5025C MTC |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

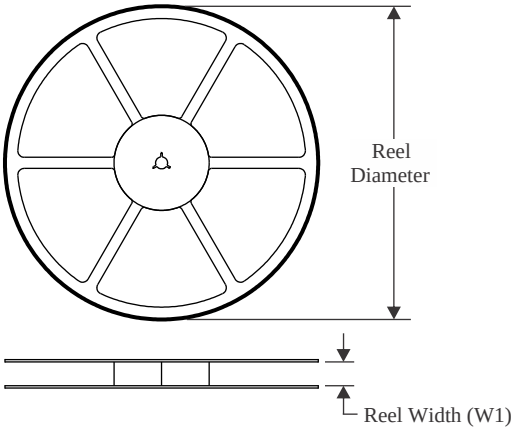
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

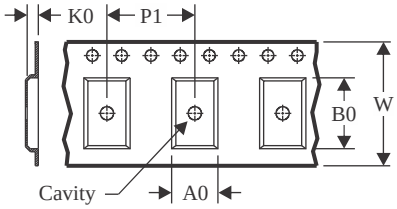
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

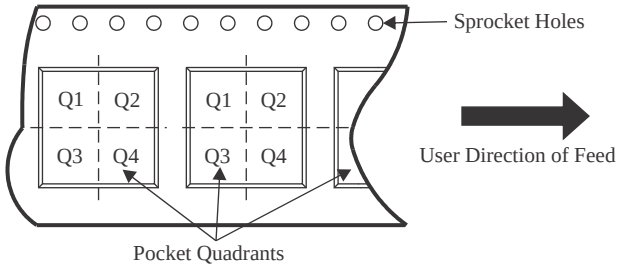



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

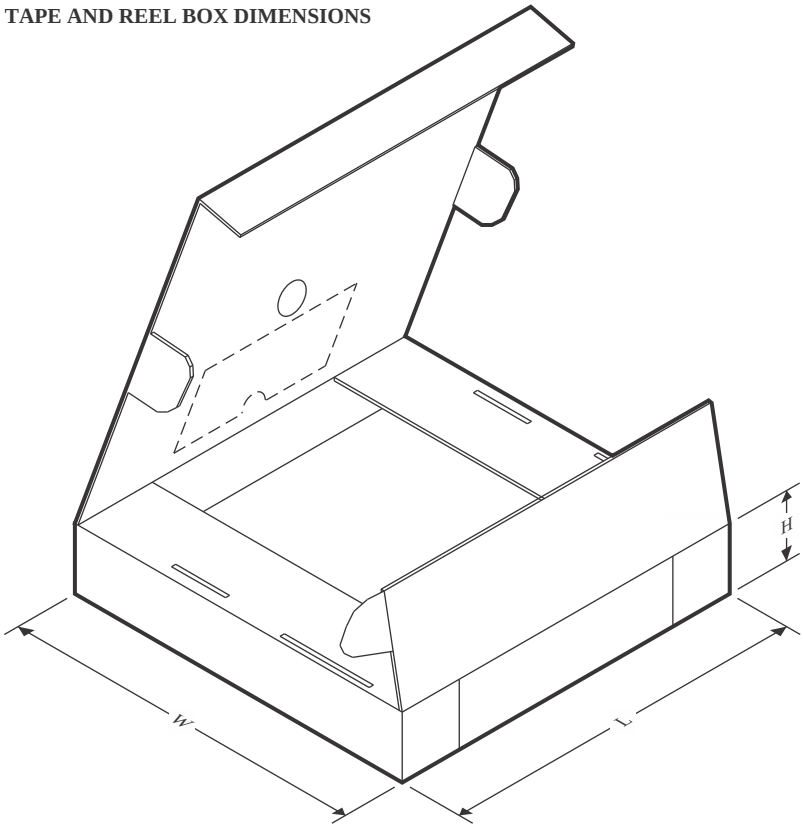
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5025CMTCX/NOPB | TSSOP | PW | 16 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LM5025CMTCX/NOPB | TSSOP | PW | 16 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

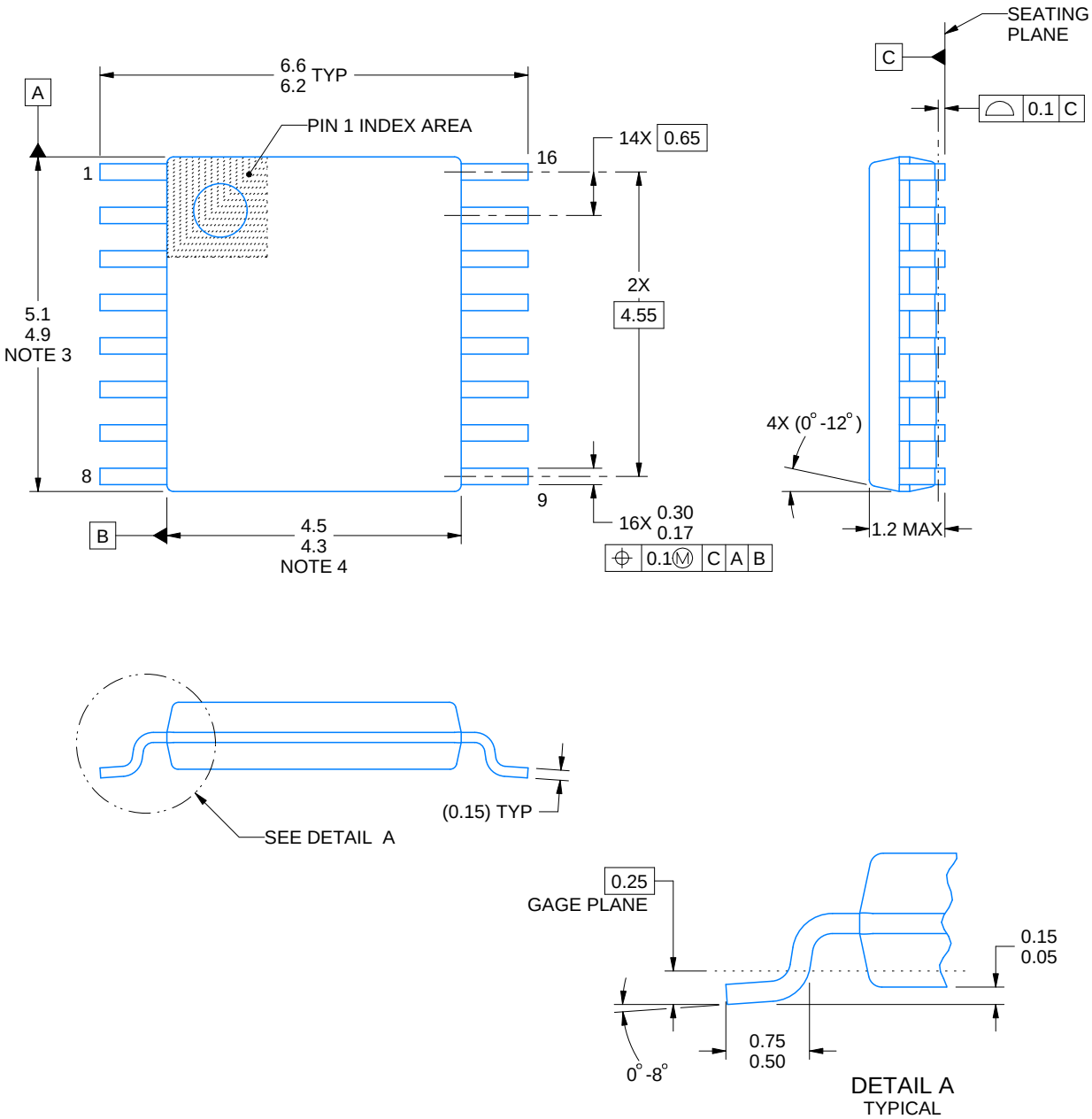
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5025CMTCX/NOPB | TSSOP | PW | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| LM5025CMTCX/NOPB | TSSOP | PW | 16 | 2500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## PW0016A

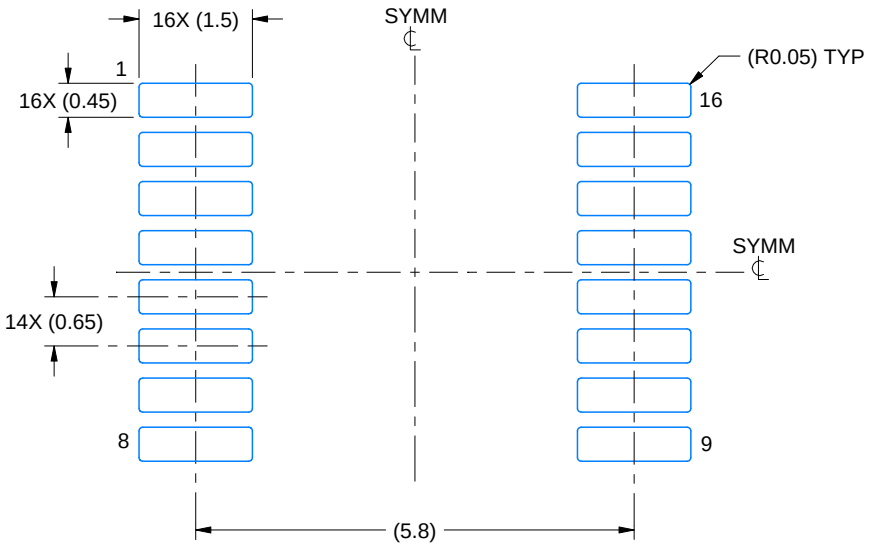
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

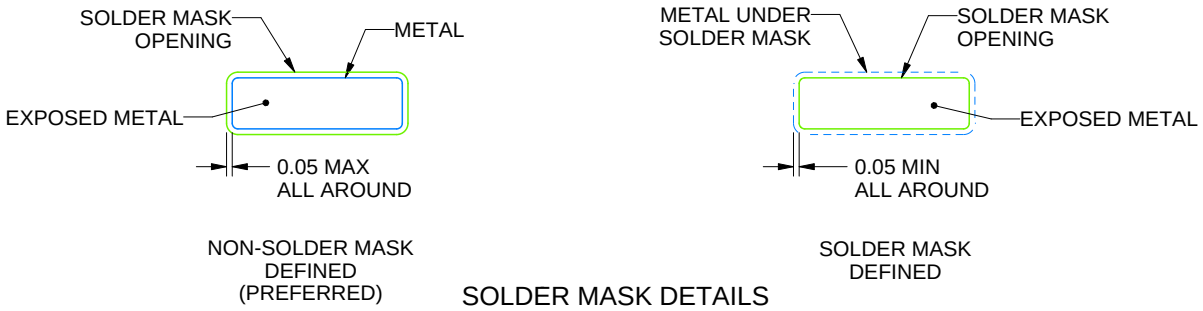



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

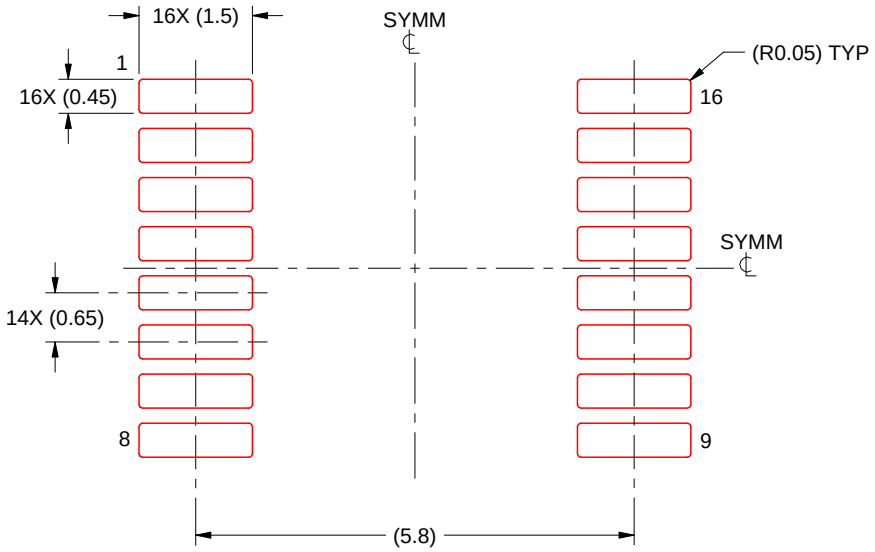



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025