

# SN74LVC244A-Q1 Automotive Octal Buffer or Driver With 3-State Outputs

## 1 Features

- Qualified for Automotive Applications
- Operates from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Maximum  $t_{pd}$  of 5.9ns at 3.3V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Supports mixed-mode signal operation on all ports (5V input or output voltage with 3.3V  $V_{CC}$ )
- $I_{off}$  supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- [Combining power good signals](#)
- [Enable digital signals](#)

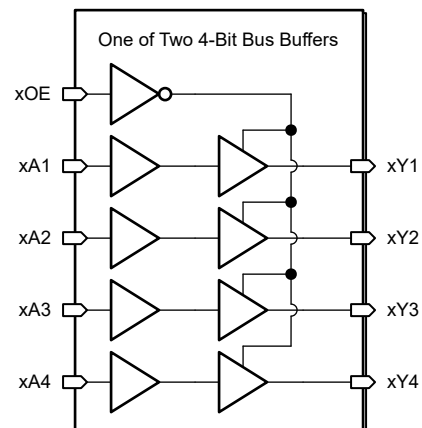
## 3 Description

These octal bus buffers are designed for 1.65V to 3.6V  $V_{CC}$  operation. The SN74LVC244A-Q1 devices are designed for asynchronous communication between data buses.

### Package Information

| PART NUMBER    | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|----------------|------------------------|-----------------------------|--------------------------|
| SN74LVC244A-Q1 | RKS (VQFN, 20)         | 4.50mm × 2.50mm             | 4.50mm × 2.50mm          |
|                | DW (SOIC, 20)          | 12.80mm × 10.3mm            | 12.80mm × 7.50mm         |
|                | PW (TSSOP, 20)         | 6.50mm × 6.4mm              | 6.50mm × 4.40mm          |
|                | DGS (VSSOP, 20)        | 5.10mm × 4.90mm             | 5.10mm × 3.00mm          |

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



**Logic Diagram (Positive Logic)**



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## 4 Pin Configuration and Functions

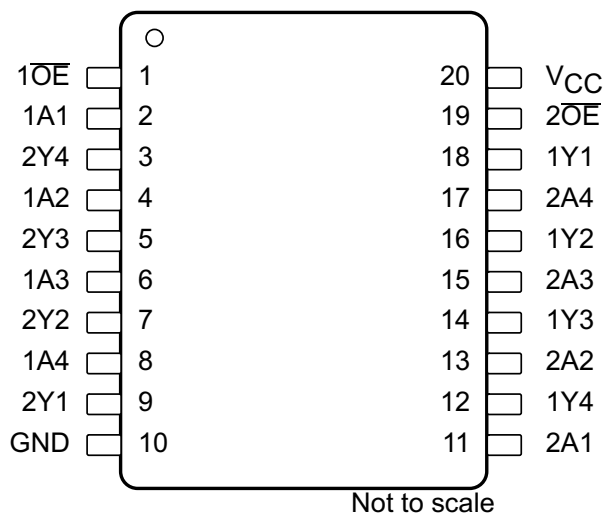


**Figure 4-1. DW, DGS and PW Packages 20-Pin SOIC, VSSOP and TSSOP Front View**

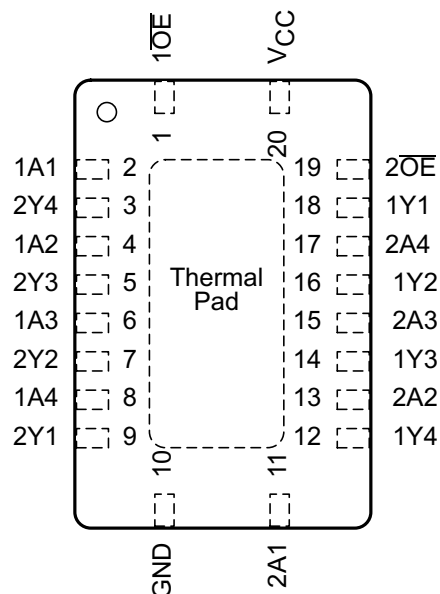


**Figure 4-2. RKS Package 20-Pin VQFN Top View**

**Table 4-1. Pin Functions**

| PIN               |                        | TYPE | DESCRIPTION     |
|-------------------|------------------------|------|-----------------|
| NAME              | DW, PW, DGS<br>and RKS |      |                 |
| 1A1               | 2                      | I    | Port 1A1 input  |
| 1A2               | 4                      | I    | Port 1A2 input  |
| 1A3               | 6                      | I    | Port 1A3 input  |
| 1A4               | 8                      | I    | Port 1A4 input  |
| 1 $\overline{OE}$ | 1                      | I    | Output enable   |
| 1Y1               | 18                     | O    | Port 1Y1 output |
| 1Y2               | 16                     | O    | Port 1Y2 output |
| 1Y3               | 14                     | O    | Port 1Y3 output |
| 1Y4               | 12                     | O    | Port 1Y4 output |
| 2A1               | 11                     | I    | Port 2A1 input  |
| 2A2               | 13                     | I    | Port 2A2 input  |
| 2A3               | 15                     | I    | Port 2A3 input  |
| 2A4               | 17                     | I    | Port 2A4 input  |
| 2 $\overline{OE}$ | 19                     | I    | Output enable   |
| 2Y1               | 9                      | O    | Port 2Y1 output |
| 2Y2               | 7                      | O    | Port 2Y2 output |
| 2Y3               | 5                      | O    | Port 2Y3 output |
| 2Y4               | 3                      | O    | Port 2Y4 output |
| GND               | 10                     | —    | Ground          |
| V <sub>CC</sub>   | 20                     | —    | Power pin       |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                             | MIN                                                 | MAX                   | UNIT |
|------------------|---------------------------------------------------------------------------------------------|-----------------------------------------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                                                              | –0.5                                                | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                                                                | –0.5                                                | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | –0.5                                                | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>             | –0.5                                                | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0                                  | –50                   | mA   |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0                                  | –50                   | mA   |
| I <sub>O</sub>   | Continuous output current                                                                   |                                                     | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                                                     | ±100                  | mA   |
| P <sub>tot</sub> | Power dissipation                                                                           | T <sub>A</sub> = –40°C to +125°C <sup>(4) (5)</sup> | 500                   | mW   |
| T <sub>J</sub>   | Junction temperature                                                                        |                                                     | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature                                                                         | –65                                                 | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the [Section 5.3](#) table.
- (4) For the DW package: above 70°C the value of P<sub>tot</sub> derates linearly with 8mW/K.
- (5) For the DB, DGV, N, NS, and PW packages: above 60°C the value of P<sub>tot</sub> derates linearly with 5.5mW/K.

### 5.2 ESD Ratings

|                    |                                                                               | VALUE | UNIT |
|--------------------|-------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge                                                       |       |      |
|                    | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>             | ±2000 | V    |
|                    | Charged-device model (CDM), per JEDEC specification JESD22C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                           | T <sub>A</sub> = 25°C            |                        | –40 TO +85°C    |                        | –40 TO +125°C   |                        | UNIT            |    |
|-----------------|---------------------------|----------------------------------|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|----|
|                 |                           | MIN                              | MAX                    | MIN             | MAX                    | MIN             | MAX                    |                 |    |
| V <sub>CC</sub> | Supply voltage            | Operating                        | 1.65                   | 3.6             | 1.65                   | 3.6             | 1.65                   | 3.6             | V  |
|                 |                           | Data retention only              | 1.5                    |                 | 1.5                    |                 | 1.5                    |                 |    |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 1.65V to 1.95V | 0.65 × V <sub>CC</sub> |                 | 0.65 × V <sub>CC</sub> |                 | 0.65 × V <sub>CC</sub> |                 | V  |
|                 |                           | V <sub>CC</sub> = 2.3V to 2.7V   | 1.7                    |                 | 1.7                    |                 | 1.7                    |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7V to 3.6V   | 2                      |                 | 2                      |                 | 2                      |                 |    |
| V <sub>IL</sub> | Low-level input voltage   | V <sub>CC</sub> = 1.65V to 1.95V | 0.35 × V <sub>CC</sub> |                 | 0.35 × V <sub>CC</sub> |                 | 0.35 × V <sub>CC</sub> |                 | V  |
|                 |                           | V <sub>CC</sub> = 2.3V to 2.7V   | 0.7                    |                 | 0.7                    |                 | 0.7                    |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7V to 3.6V   | 0.8                    |                 | 0.8                    |                 | 0.8                    |                 |    |
| V <sub>I</sub>  | Input voltage             |                                  | 0                      | 5.5             | 0                      | 5.5             | 0                      | 5.5             | V  |
| V <sub>O</sub>  | Output voltage            |                                  | 0                      | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | 0                      | V <sub>CC</sub> | V  |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65V          | –4                     |                 | –4                     |                 | –4                     |                 | mA |
|                 |                           | V <sub>CC</sub> = 2.3V           | –8                     |                 | –8                     |                 | –8                     |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7V           | –12                    |                 | –12                    |                 | –12                    |                 |    |
|                 |                           | V <sub>CC</sub> = 3V             | –24                    |                 | –24                    |                 | –24                    |                 |    |
| I <sub>OL</sub> | Low-level output current  | V <sub>CC</sub> = 1.65V          | 4                      |                 | 4                      |                 | 4                      |                 | mA |
|                 |                           | V <sub>CC</sub> = 2.3V           | 8                      |                 | 8                      |                 | 8                      |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7V           | 12                     |                 | 12                     |                 | 12                     |                 |    |
|                 |                           | V <sub>CC</sub> = 3V             | 24                     |                 | 24                     |                 | 24                     |                 |    |
| T <sub>A</sub>  | Ambient temperature       | BGA package                      |                        |                 | –40                    | 85              |                        |                 | °C |
|                 |                           | All other packages               |                        |                 |                        |                 | –40                    | 125             |    |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC244A                 |                              |                              | UNIT |
|-------------------------------|----------------------------------------------|-----------------------------|------------------------------|------------------------------|------|
|                               |                                              | DW <sup>(2)</sup><br>(SOIC) | PW <sup>(2)</sup><br>(TSSOP) | RKS <sup>(3)</sup><br>(VQFN) |      |
|                               |                                              | 20 PINS                     |                              |                              |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 58                          | 83                           | 87.2                         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    |                             |                              | 93.4                         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         |                             |                              | 59.8                         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   |                             |                              | 24.9                         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter |                             |                              | 59.6                         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | —                           | —                            | 44.3                         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

(3) The package thermal impedance is calculated in accordance with JESD 51-5.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                                             |                    | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | –40 TO +85°C          |     | –40 TO +125°C         |     | UNIT |
|-------------------------|-----------------------------------------------------------------------------|--------------------|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|-----|------|
|                         |                                                                             |                    |                 | MIN                   | TYP | MAX | MIN                   | MAX | MIN                   | MAX |      |
| V <sub>OH</sub>         | I <sub>OH</sub> = –100μA                                                    |                    | 1.65V to 3.6V   | V <sub>CC</sub> – 0.2 |     |     | V <sub>CC</sub> – 0.2 |     | V <sub>CC</sub> – 0.3 |     | V    |
|                         | I <sub>OH</sub> = –4mA                                                      |                    | 1.65V           | 1.29                  |     |     | 1.2                   |     | 1.05                  |     |      |
|                         | I <sub>OH</sub> = –8mA                                                      |                    | 2.3V            | 1.9                   |     |     | 1.7                   |     | 1.55                  |     |      |
|                         | I <sub>OH</sub> = –12mA                                                     |                    | 2.7V            | 2.2                   |     |     | 2.2                   |     | 2.05                  |     |      |
|                         |                                                                             |                    | 3V              | 2.4                   |     |     | 2.4                   |     | 2.25                  |     |      |
| I <sub>OH</sub> = –24mA |                                                                             | 3V                 | 2.3             |                       |     | 2.2 |                       | 2   |                       |     |      |
| V <sub>OL</sub>         | I <sub>OL</sub> = 100μA                                                     |                    | 1.65V to 3.6V   | 0.1                   |     |     | 0.2                   |     | 0.3                   |     | V    |
|                         | I <sub>OL</sub> = 4mA                                                       |                    | 1.65V           | 0.24                  |     |     | 0.45                  |     | 0.6                   |     |      |
|                         | I <sub>OL</sub> = 8mA                                                       |                    | 2.3V            | 0.3                   |     |     | 0.7                   |     | 0.75                  |     |      |
|                         | I <sub>OL</sub> = 12mA                                                      |                    | 2.7V            | 0.4                   |     |     | 0.4                   |     | 0.6                   |     |      |
|                         | I <sub>OL</sub> = 24mA                                                      |                    | 3V              | 0.55                  |     |     | 0.55                  |     | 0.8                   |     |      |
| I <sub>I</sub>          | V <sub>I</sub> = 5.5V or GND                                                |                    | 3.6V            | ±1                    |     |     | ±5                    |     | ±20                   |     | μA   |
| I <sub>off</sub>        | V <sub>I</sub> or V <sub>O</sub> = 5.5V                                     |                    | 0               | ±1                    |     |     | ±10                   |     | ±20                   |     | μA   |
| I <sub>OZ</sub>         | V <sub>O</sub> = 0 to 5.5V                                                  |                    | 3.6V            | ±1                    |     |     | ±10                   |     | ±20                   |     | μA   |
| I <sub>CC</sub>         | V <sub>I</sub> = V <sub>CC</sub> or GND                                     | I <sub>O</sub> = 0 | 3.6V            | 1                     |     |     | 10                    |     | 40                    |     | μA   |
|                         | 3.6V ≤ V <sub>I</sub> ≤ 5.5V <sup>(1)</sup>                                 |                    |                 | 10                    |     | 40  |                       |     |                       |     |      |
| ΔI <sub>CC</sub>        | One input at V <sub>CC</sub> – 0.6V, Other inputs at V <sub>CC</sub> or GND |                    | 2.7V to 3.6V    | 500                   |     |     | 500                   |     | 5000                  |     | μA   |
| C <sub>i</sub>          | V <sub>I</sub> = V <sub>CC</sub> or GND                                     |                    | 3.3V            | 4                     |     |     |                       |     |                       |     | pF   |
| C <sub>o</sub>          | V <sub>O</sub> = V <sub>CC</sub> or GND                                     |                    | 3.3V            | 5.5                   |     |     |                       |     |                       |     | pF   |

(1) This applies in the disabled state only.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER          | FROM<br>(INPUT)        | TO<br>(OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | –40 TO +85°C |      | –40 TO +125°C |      | UNIT |
|--------------------|------------------------|----------------|-----------------|-----------------------|-----|------|--------------|------|---------------|------|------|
|                    |                        |                |                 | MIN                   | TYP | MAX  | MIN          | MAX  | MIN           | MAX  |      |
| t <sub>pd</sub>    | A                      | Y              | 1.5V            |                       | 7   | 14.4 |              | 14.9 |               | 16.4 | ns   |
|                    |                        |                | 1.8V ± 0.15V    |                       | 5.9 | 10.4 |              | 10.9 |               | 12.4 |      |
|                    |                        |                | 2.5V ± 0.2V     |                       | 4.2 | 7.4  |              | 7.9  |               | 10   |      |
|                    |                        |                | 2.7V            |                       | 4.2 | 6.7  |              | 6.9  |               | 8.2  |      |
|                    |                        |                | 3.3V ± 0.3V     |                       | 3.9 | 5.7  |              | 5.9  |               | 7.2  |      |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y              | 1.5V            |                       | 8.3 | 17.8 |              | 18.3 |               | 19.8 | ns   |
|                    |                        |                | 1.8V ± 0.15V    |                       | 6.4 | 12.1 |              | 12.6 |               | 14.1 |      |
|                    |                        |                | 2.5V ± 0.2V     |                       | 4.6 | 9.1  |              | 9.6  |               | 11.7 |      |
|                    |                        |                | 2.7V            |                       | 5   | 8.4  |              | 8.6  |               | 10.3 |      |
|                    |                        |                | 3.3V ± 0.3V     |                       | 4.5 | 7.4  |              | 7.6  |               | 9.4  |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y              | 1.5V            |                       | 7.2 | 15.6 |              | 16.1 |               | 17.6 | ns   |
|                    |                        |                | 1.8V ± 0.15V    |                       | 5.8 | 11.6 |              | 12.1 |               | 13.6 |      |
|                    |                        |                | 2.5V ± 0.2V     |                       | 3.7 | 7.3  |              | 7.8  |               | 9.9  |      |
|                    |                        |                | 2.7V            |                       | 3.8 | 6.6  |              | 6.8  |               | 8.6  |      |
|                    |                        |                | 3.3V ± 0.3V     |                       | 3.8 | 6.3  |              | 6.5  |               | 8    |      |
| t <sub>sk(o)</sub> |                        |                | 3.3V ± 0.3V     |                       |     |      |              | 1    |               | 1.5  | ns   |

## 5.7 Operating Characteristics

T<sub>A</sub> = 25°C

| PARAMETER       |                                                 | TEST CONDITIONS |           | V <sub>CC</sub> | TYP | UNIT |
|-----------------|-------------------------------------------------|-----------------|-----------|-----------------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10MHz | 1.8V            | 43  | pF   |
|                 |                                                 |                 |           | 2.5V            | 43  |      |
|                 |                                                 |                 |           | 3.3V            | 44  |      |
|                 | Outputs disabled                                | f = 10MHz       |           | 1.8V            | 1   |      |
|                 |                                                 |                 |           | 2.5V            | 1   |      |
|                 |                                                 |                 |           | 3.3V            | 2   |      |

## 5.8 Typical Characteristics

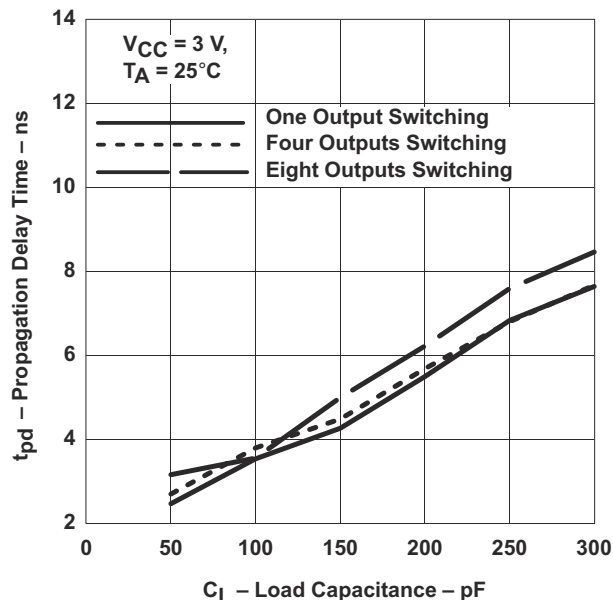


**Figure 5-1. Propagation Delay (Low to High Transition)  
vs Load Capacitance**

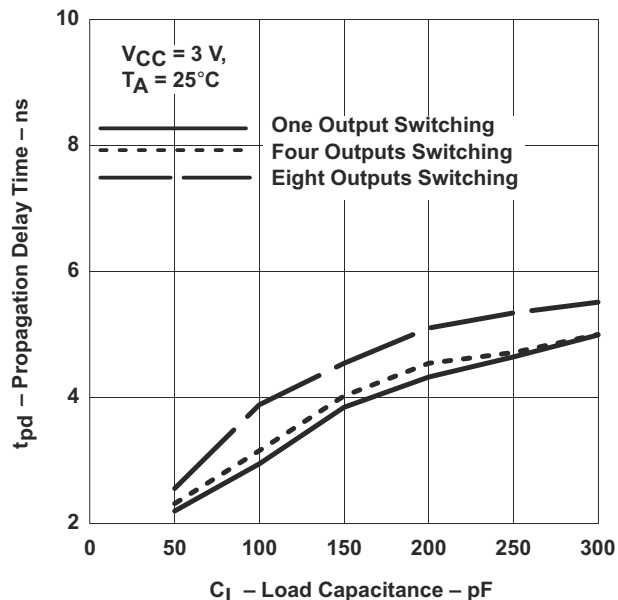
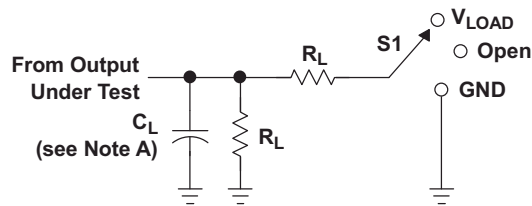


**Figure 5-2. Propagation Delay (High to Low Transition)  
vs Load Capacitance**

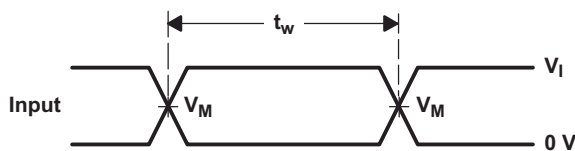
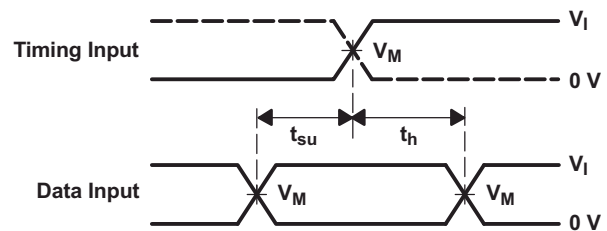
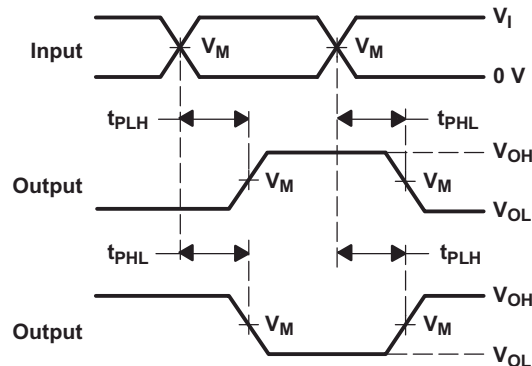
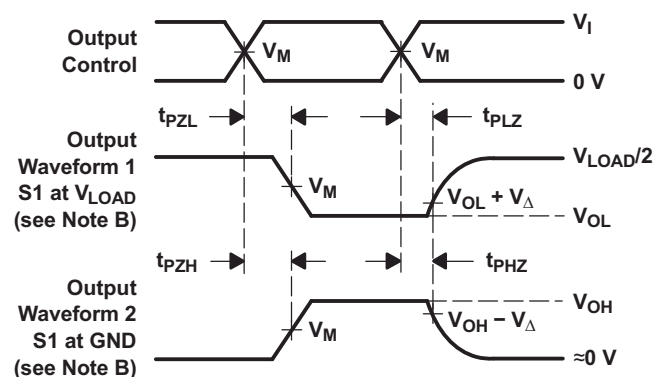
## 6 Parameter Measurement Information



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                           | INPUTS   |               | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|------------------------------------|----------|---------------|------------|-------------------|-------|--------------|--------------|
|                                    | $V_I$    | $t_r/t_f$     |            |                   |       |              |              |
| 1.5 V                              | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 2 k $\Omega$ | 0.1 V        |
| $1.8 \text{ V} \pm 0.15 \text{ V}$ | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5 \text{ V} \pm 0.2 \text{ V}$  | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                              | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3 \text{ V} \pm 0.3 \text{ V}$  | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |

VOLTAGE WAVEFORMS  
PULSE DURATIONVOLTAGE WAVEFORMS  
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74LVC244A-Q1 contains 8 individual high speed CMOS buffers organized as two 4-bit buffers/line drives with 3-state outputs.

Each buffer performs the boolean logic function  $xY_n = xA_n$ , with  $x$  being the bank number and  $n$  being the channel number.

Each output enable ( $x\overline{OE}$ ) controls four buffers. When the  $x\overline{OE}$  pin is in the low state, the outputs of all buffers in the bank  $x$  are enabled. When the  $x\overline{OE}$  pin is in the high state, the outputs of all buffers in the bank  $x$  are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both  $\overline{OE}$  pins to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

### 7.2 Functional Block Diagram

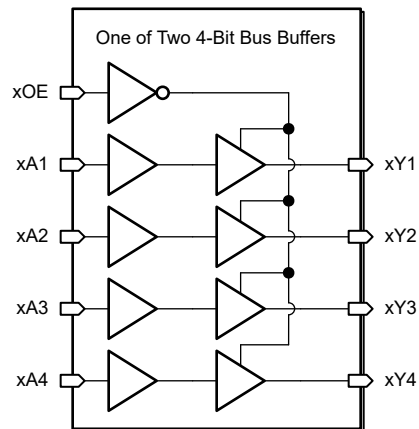


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k $\Omega$  resistor, however, is recommended and will typically meet all requirements.

### 7.3.3 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

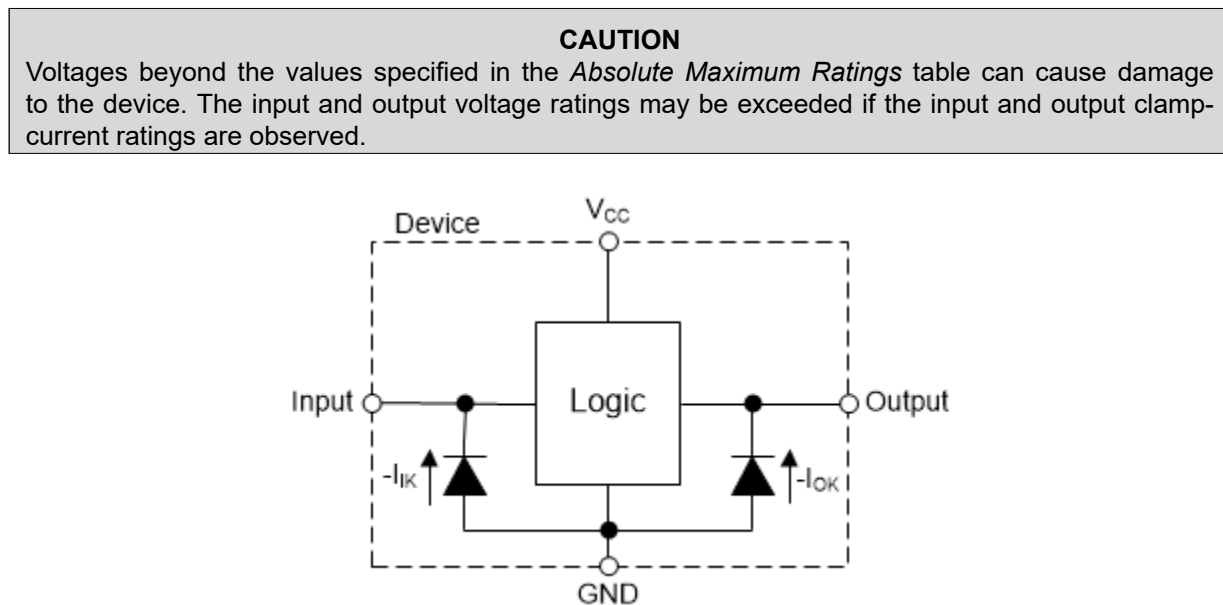


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

## 7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC244A-Q1.

Table 7-1. Function Table

| INPUTS <sup>(1)</sup> |   | OUTPUTS |
|-----------------------|---|---------|
| $\overline{OE}$       | A | Y       |
| L                     | L | L       |
| L                     | H | H       |
| H                     | X | Z       |

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

SN74LVC244A-Q1 is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 8.2 Typical Application

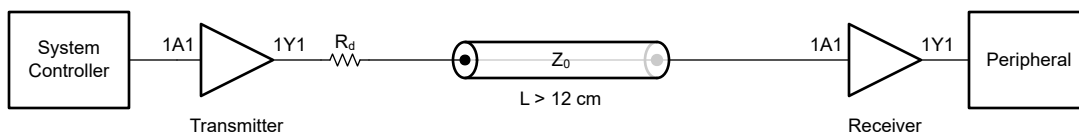


**Figure 8-1. Application Schematic**

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive will also create fast edges into light loads, so consider routing and load conditions to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - For rise time and fall time specification, see  $(\Delta t/\Delta V)$  in the *Recommended Operating Conditions* table.
  - For specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in the *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the *Recommended Operating Conditions* table at any valid  $V_{CC}$ .
- Recommended maximum Output Conditions:
  - Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
  - Outputs should not be pulled above  $V_{CC}$ .

#### 8.2.3 Application Curves

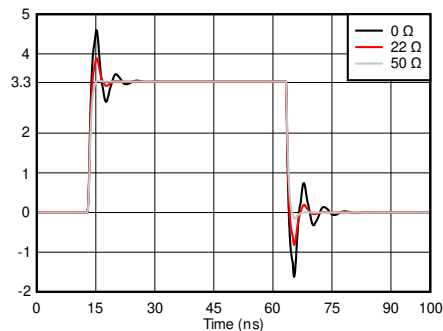


**Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ( $R_d$ ) Values**

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1 $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 $\mu$ F and 1 $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

#### 8.4.2 Layout Example

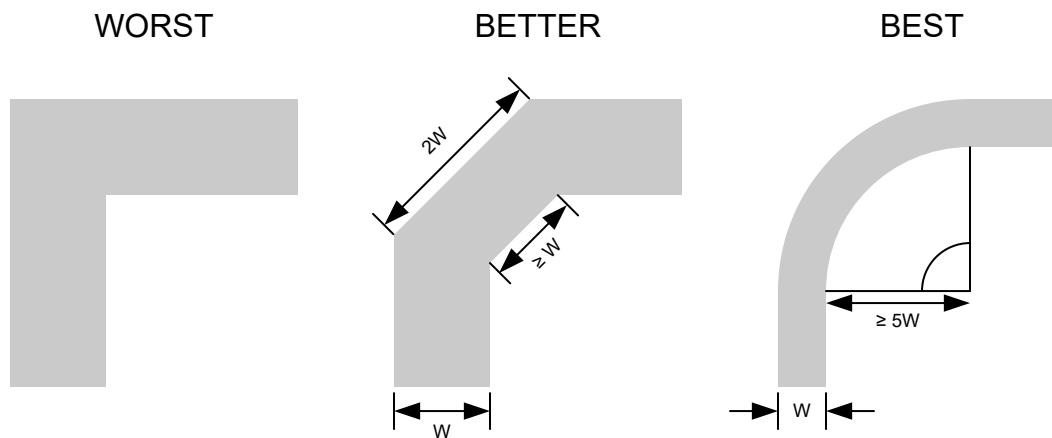


Figure 8-3. Example Trace Corners for Improved Signal Integrity

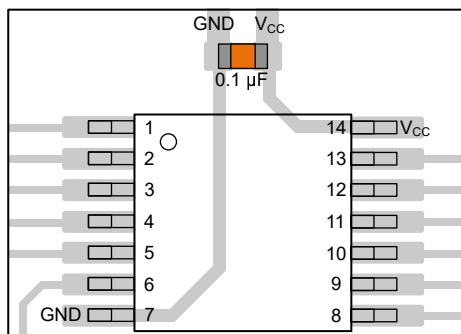


**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

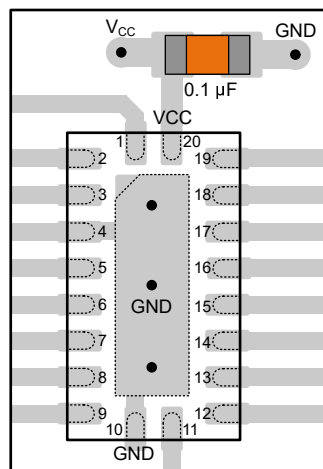


**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

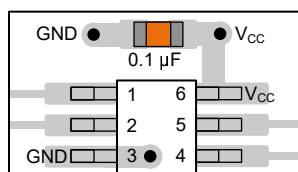


**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

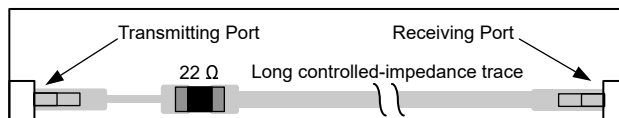


**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision C (March 2025) to Revision D (February 2026) Page

- |                                             |   |
|---------------------------------------------|---|
| • Added DGS (VSSOP, 20) package option..... | 1 |
|---------------------------------------------|---|

### Changes from Revision B (December 2008) to Revision C (March 2025) Page

- |                                            |   |
|--------------------------------------------|---|
| • Added RKS (VQFN, 20) package option..... | 1 |
|--------------------------------------------|---|

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CLVC244AQDWRG4Q1</a>  | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| CLVC244AQDWRG4Q1.B                | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| <a href="#">CLVC244AQPWRG4Q1</a>  | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| CLVC244AQPWRG4Q1.B                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| <a href="#">SN74LVC244ADGSRQ1</a> | Active        | Production           | VSSOP (DGS)   20 | 5000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | C244Q               |
| <a href="#">SN74LVC244AQPWRQ1</a> | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| SN74LVC244AQPWRQ1.A               | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |
| SN74LVC244AQPWRQ1.B               | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC244AQ            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

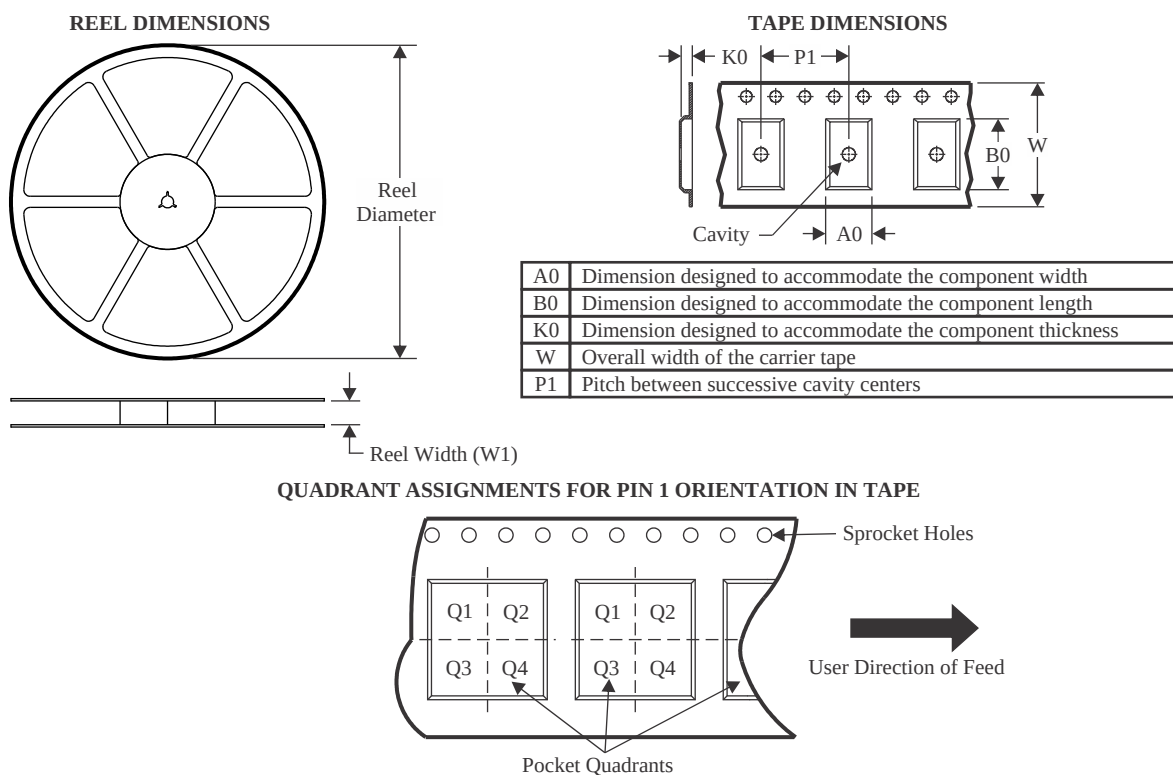
**OTHER QUALIFIED VERSIONS OF SN74LVC244A-Q1 :**

- Catalog : [SN74LVC244A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

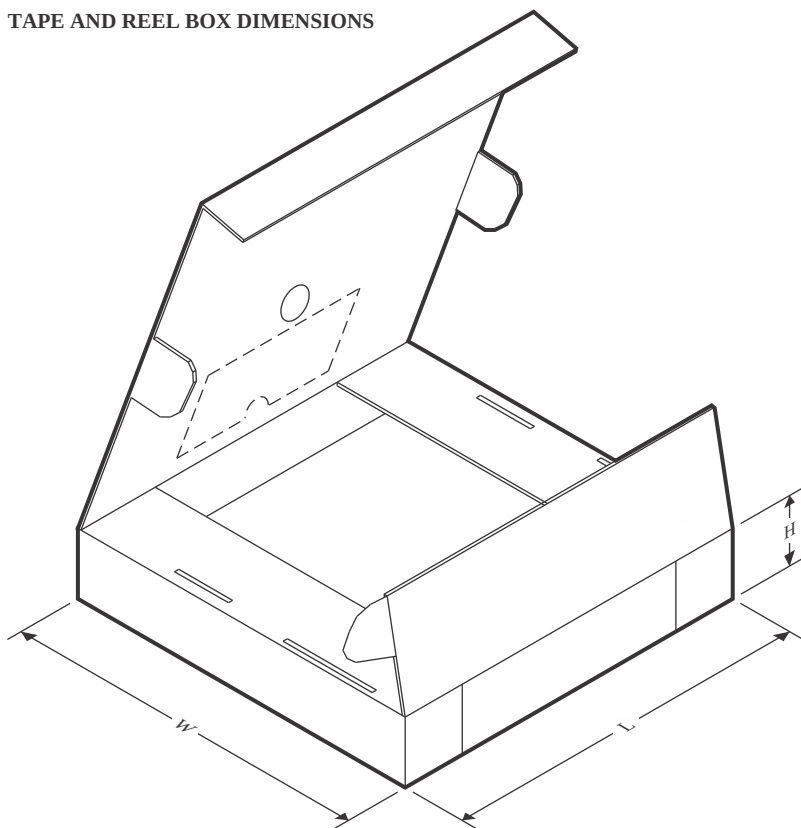
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

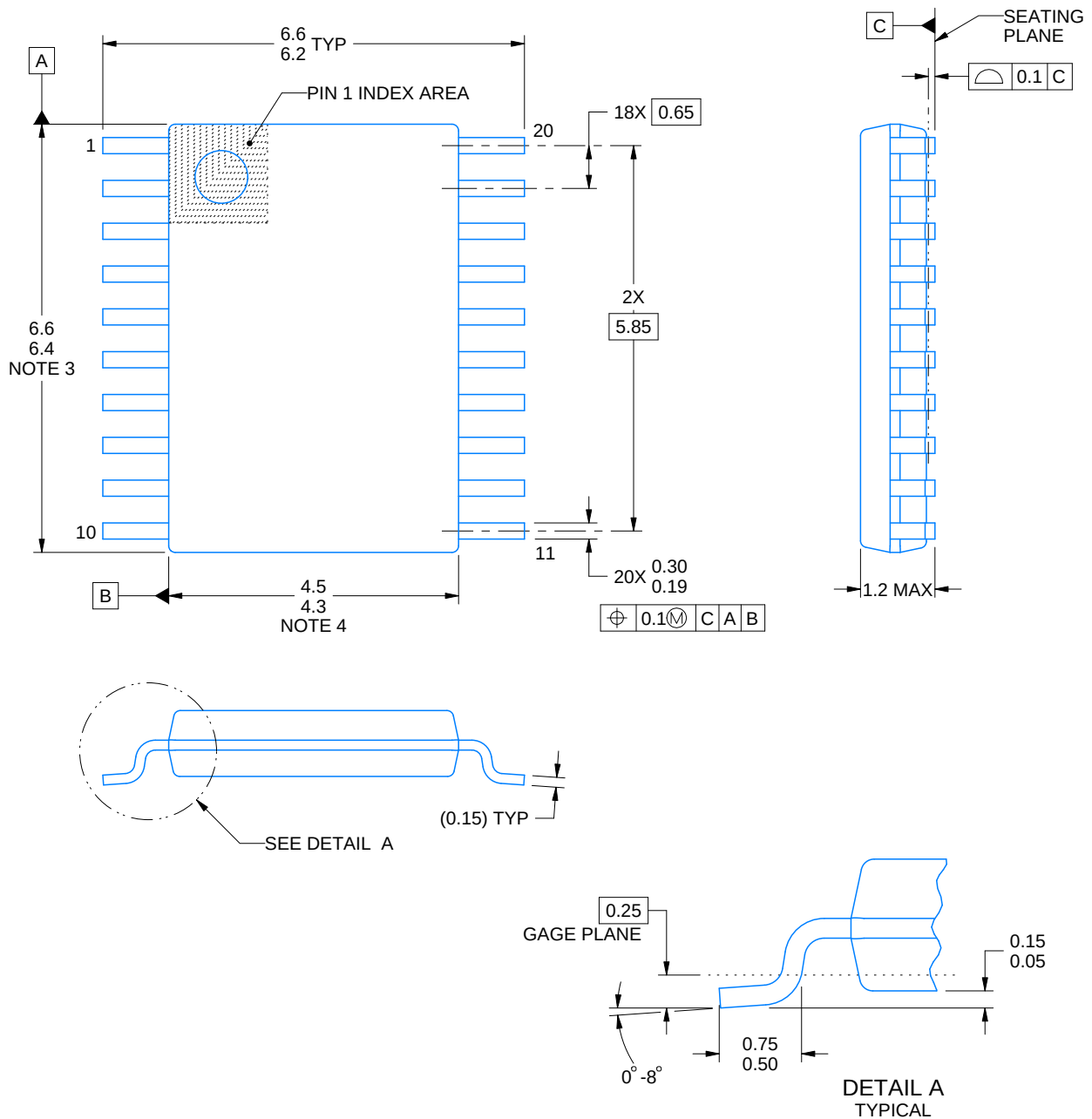
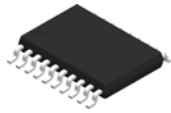
| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVC244AQDWRG4Q1  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| CLVC244AQPWRG4Q1  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| CLVC244AQPWRG4Q1  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LVC244ADGSRQ1 | VSSOP        | DGS             | 20   | 5000 | 330.0              | 16.4               | 5.4     | 5.4     | 1.45    | 8.0     | 16.0   | Q1            |
| SN74LVC244AQPWRQ1 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CLVC244AQDWRG4Q1  | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| CLVC244AQPWRG4Q1  | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| CLVC244AQPWRG4Q1  | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC244ADGSRQ1 | VSSOP        | DGS             | 20   | 5000 | 353.0       | 353.0      | 32.0        |
| SN74LVC244AQPWRQ1 | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |



4220206/A 02/2017

## NOTES:

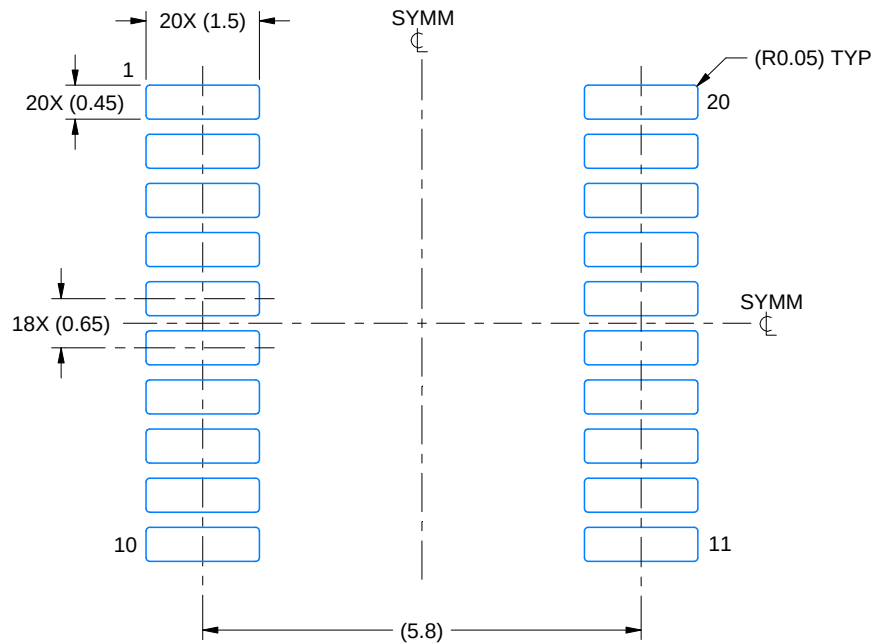
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

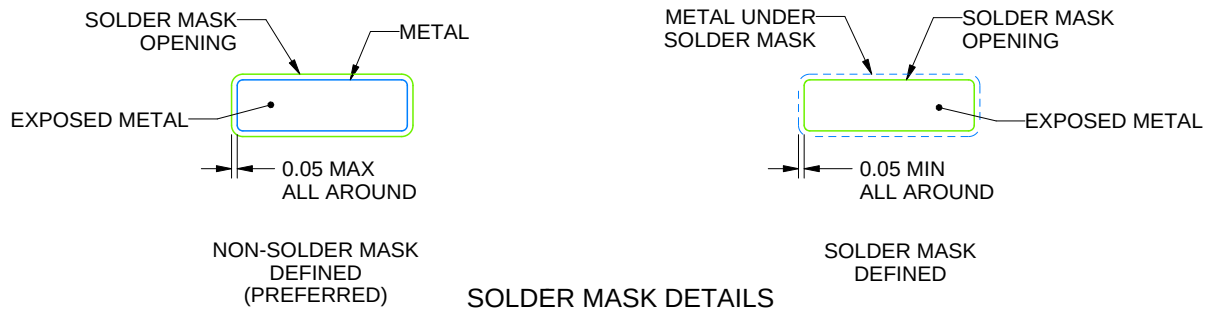
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

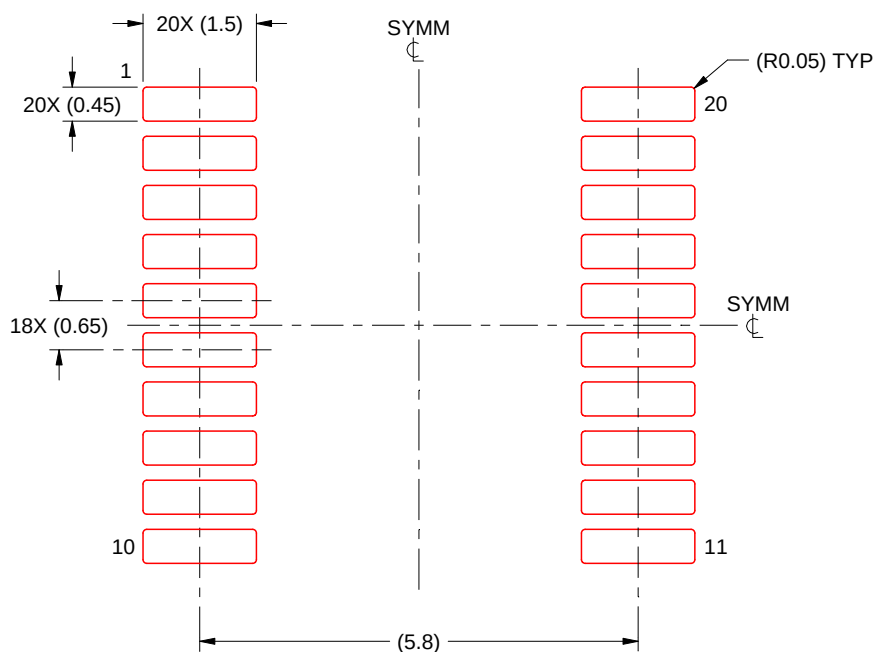
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

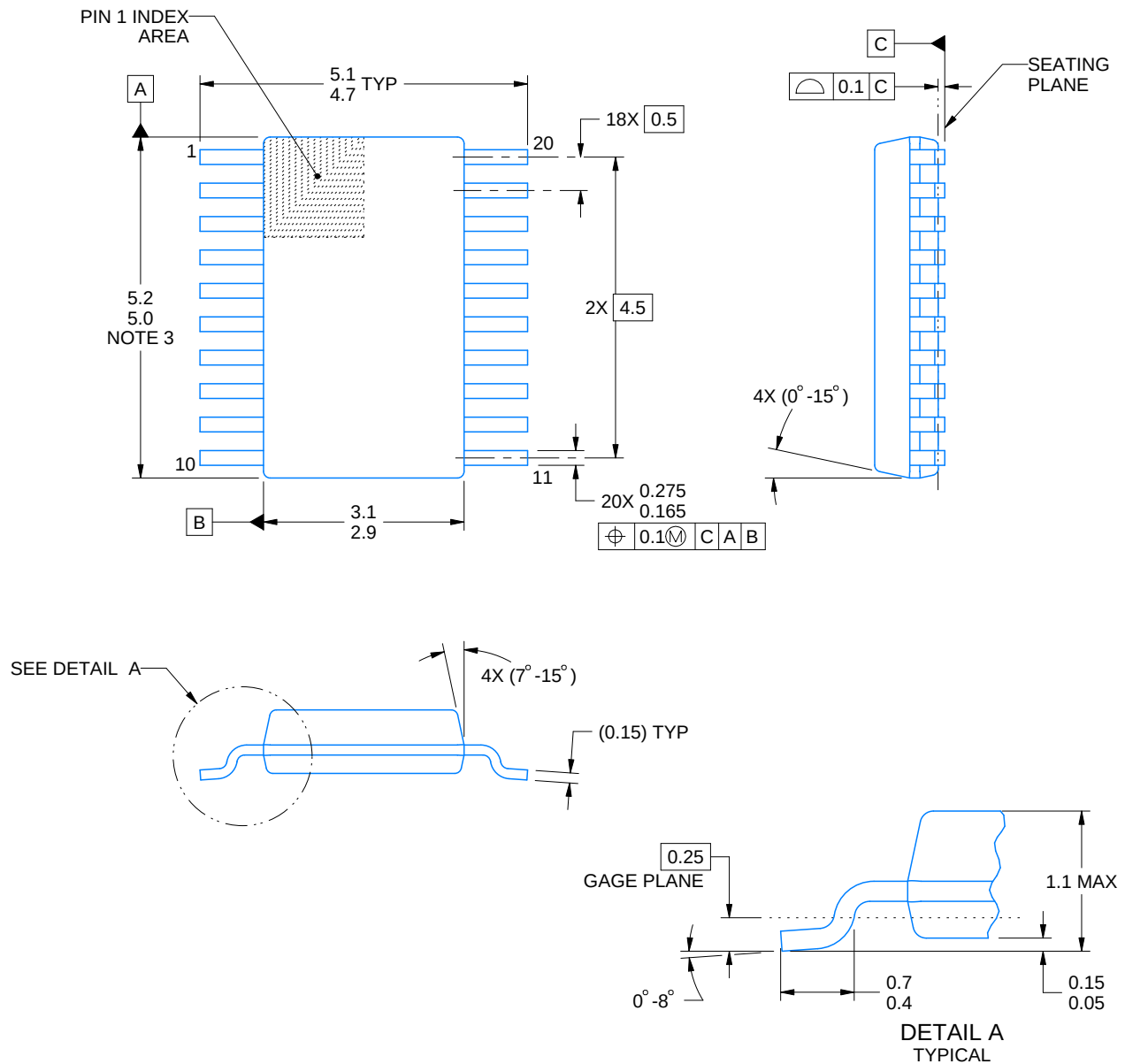


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

## NOTES:

PowerPAD is a trademark of Texas Instruments.

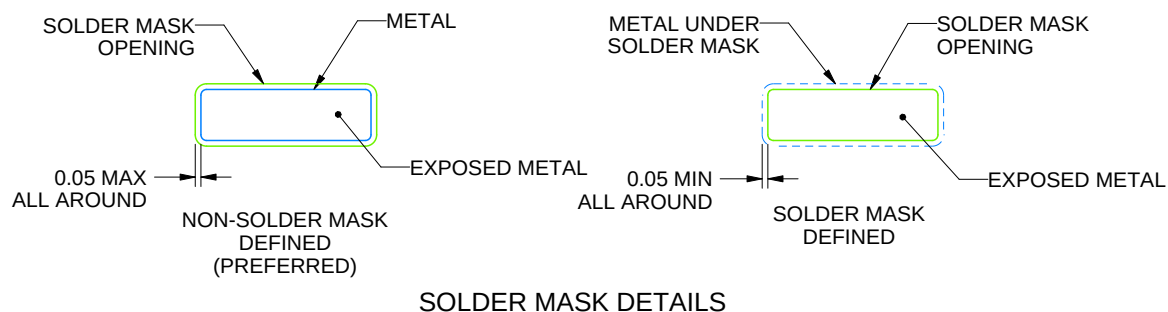
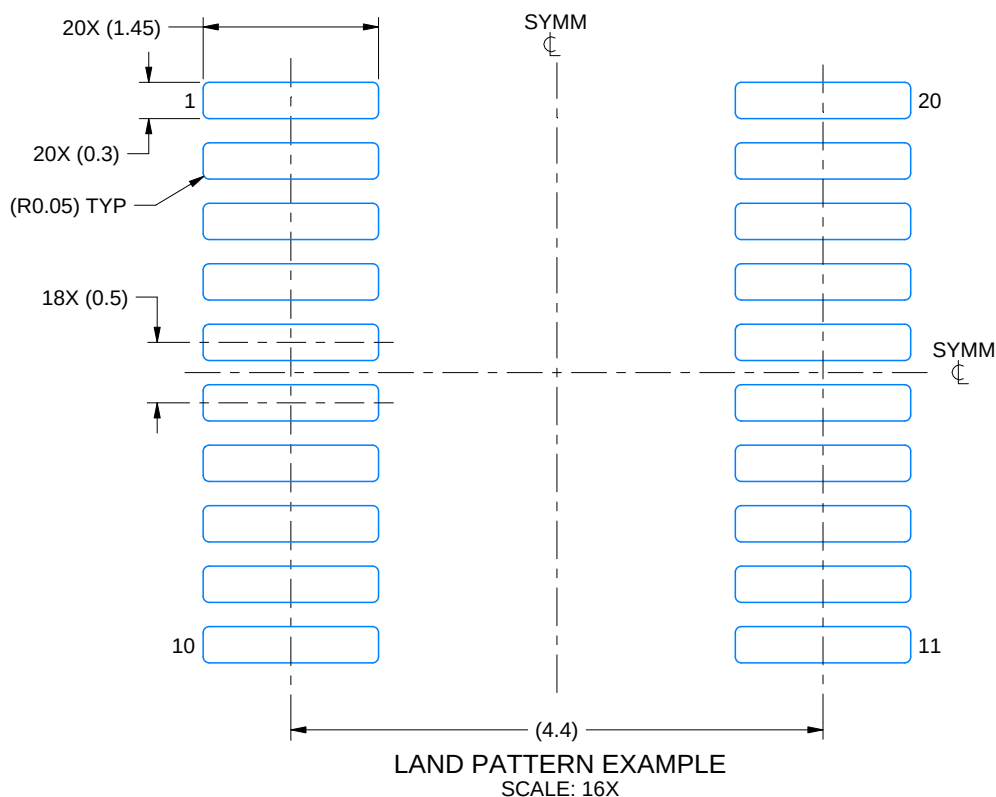
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

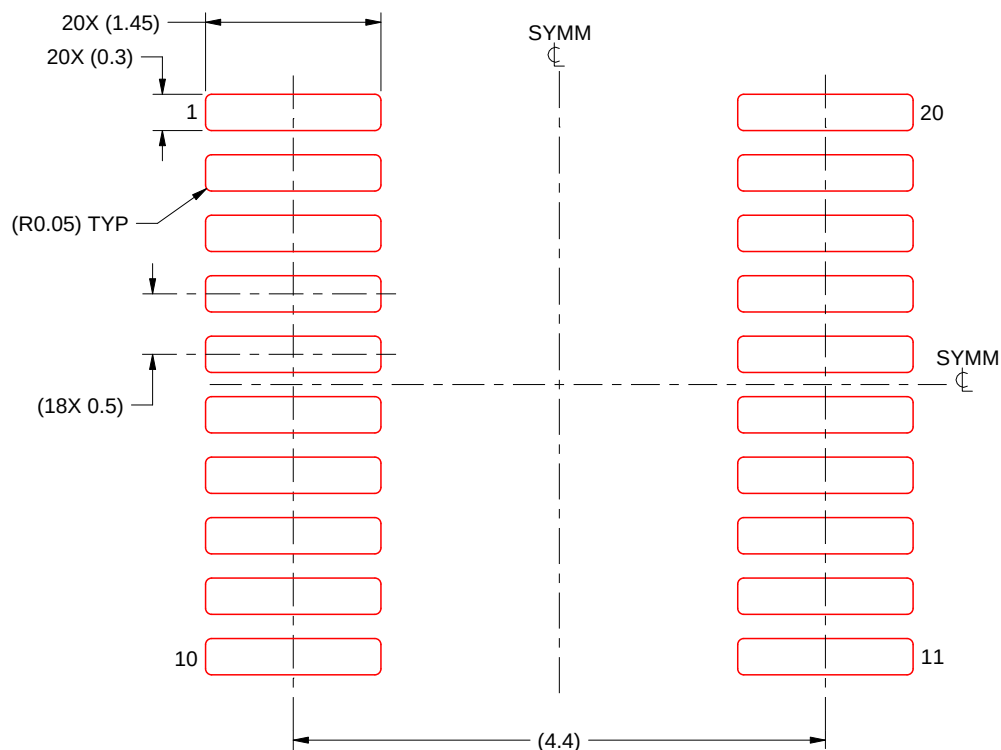
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

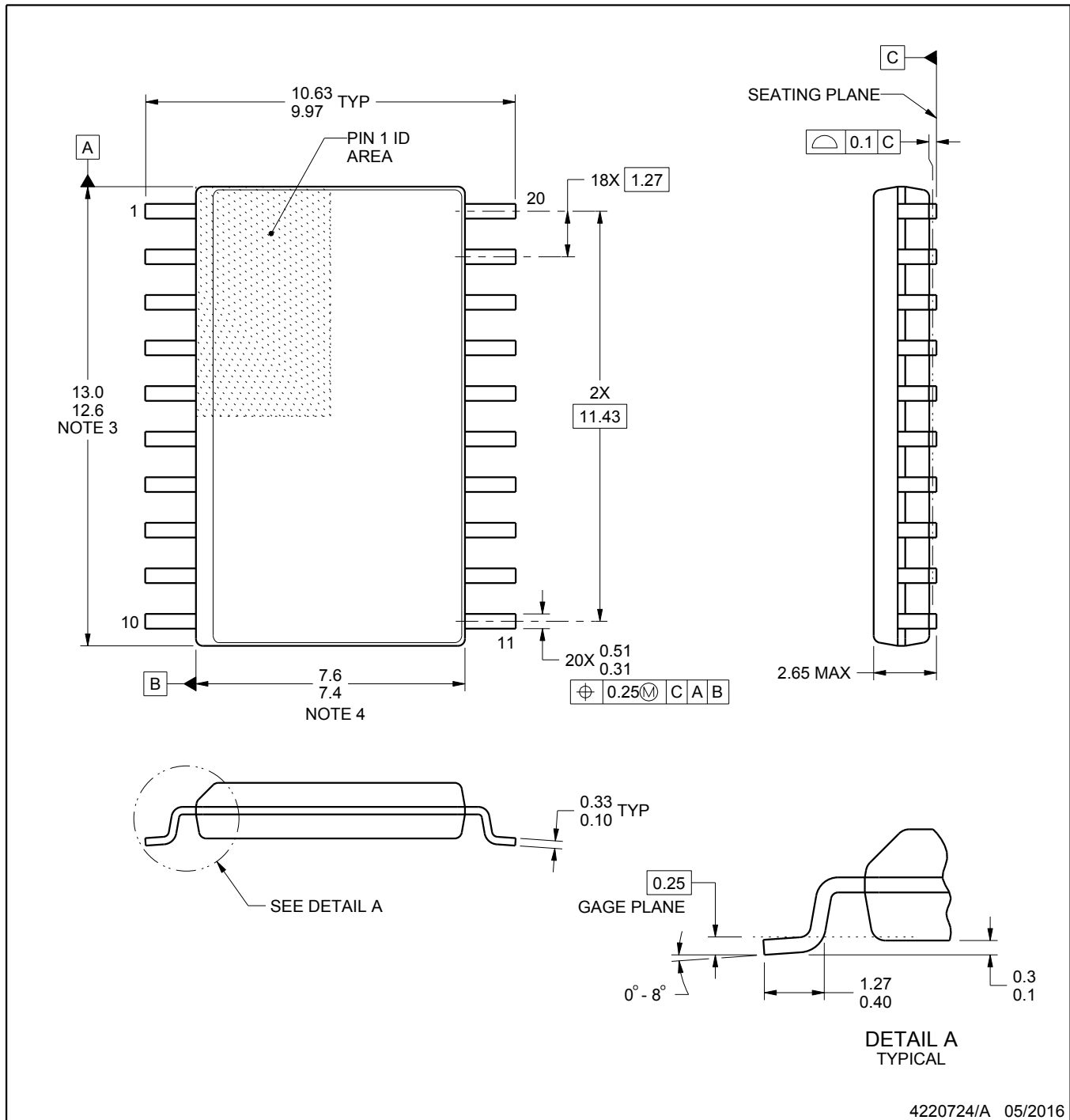
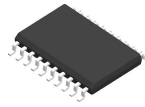


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4220724/A 05/2016

## NOTES:

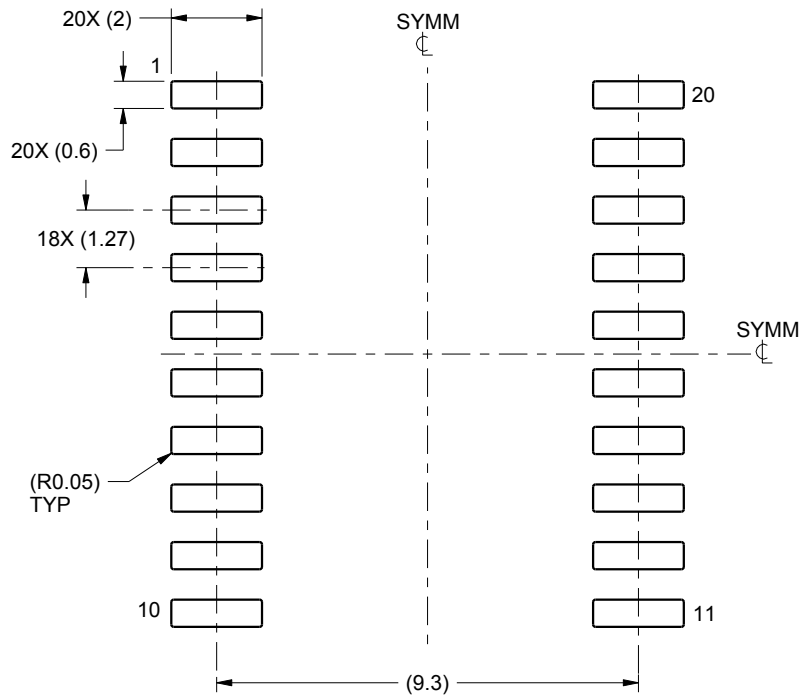
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

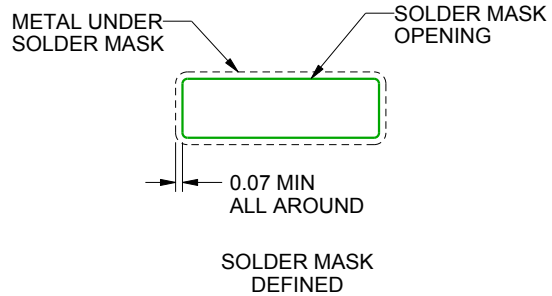
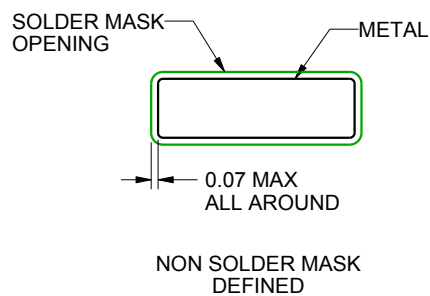
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

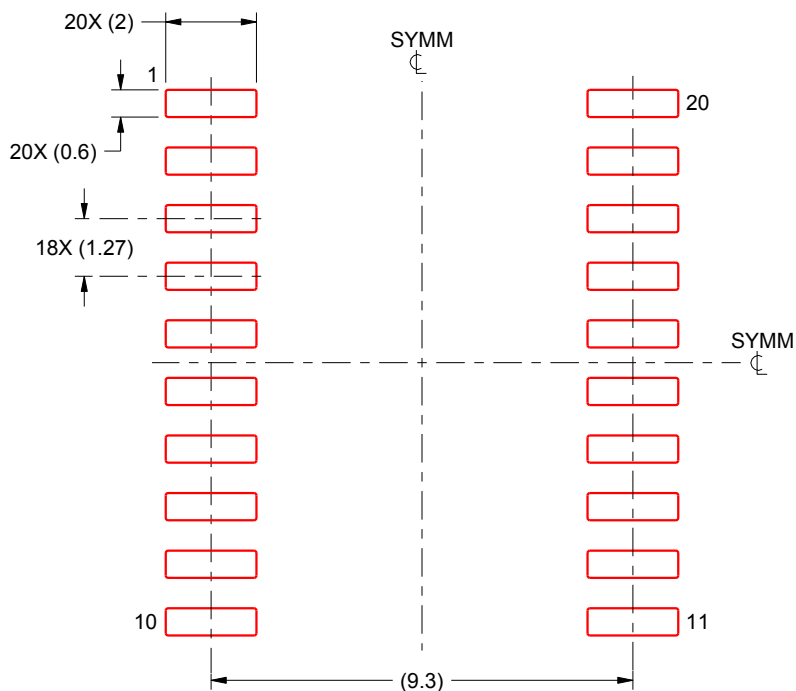
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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