

SN74LVC1G08-Q1 Single 2-Input Positive-AND Gate

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- Supports operation: $5\text{V } V_{CC}$
- Over-voltage tolerant inputs accept voltages: to 5.5V
- Provides down translation: to V_{CC}
- Low power consumption: $10\mu\text{A}$ maximum I_{CC}
- $\pm 24\text{mA}$ output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Fully qualified for automotive applications
- Combine power good signals for multiple power rails
- Prevent a signal from being passed until a condition is true
- Combine active-low error signals

3 Description

This single 2-input positive-AND gate is designed for 1.65V to $5.5\text{V } V_{CC}$ operation.

The SN74LVC1G08-Q1 device performs the Boolean function or $Y = A \cdot B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I off. The I off circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G08-Q1 is available in a variety of packages, including the small DRY package with a body size of $1.45\text{mm} \times 1.00\text{mm}$.

Package Information

DEVICE NAME	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LVC1G08-Q1	DBV (SOT-23, 5)	$2.90\text{mm} \times 1.60\text{mm}$
	DCK (SC70, 5)	$2.00\text{mm} \times 1.25\text{mm}$
	DRY, (SON, 6)	$1.45\text{mm} \times 1.00\text{mm}$

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.



Positive Logic Diagram



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4 Pin Configuration and Functions

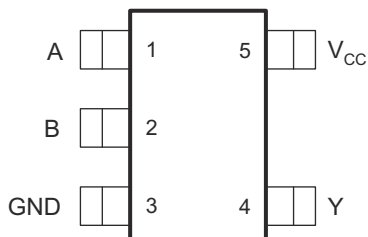


Figure 4-1. DBV package 5-pin SOT-23 (Top View)

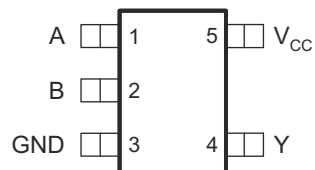
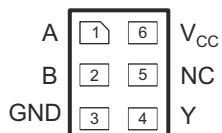


Figure 4-2. DCK package 5-pin SC-70 (Top View)



NC – No internal connection
See mechanical drawings for dimensions.

Figure 4-3. DRY package 6-pin SON (Top View)

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. DBV, DCK	NO. DRY		
A	1	1	Input	Input A
B	2	2	Input	Input B
GND	3	3	—	Ground
NC		5	—	No internal connection
V _{CC}	5	6	—	Positive Supply
Y	4	4	Output	Output Y

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		
		V _{CC} = 3V to 3.6V	2		
		V _{CC} = 4.5V to 5.5V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V		0.35 × V _{CC}	V
		V _{CC} = 2.3V to 2.7V		0.7	
		V _{CC} = 3V to 3.6V		0.8	
		V _{CC} = 4.5V to 5.5V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V		–4	mA
		V _{CC} = 2.3V		–8	
		V _{CC} = 3V		–16	
		V _{CC} = 4.5V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 3V		16	
		V _{CC} = 4.5V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V _{CC} = 3.3V ± 0.3V		10	
		V _{CC} = 5V ± 0.5V		5	
T _A	Operating free-air temperature	Q-suffix devices	–40	125	°C
		I-suffix devices	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI [Implications of Slow or Floating CMOS Inputs application note](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G08-Q1			UNIT
		DBV	DCK	DRY	
		5 PINS	5 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	357.1	371	264.4	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	263.7	297.5	166.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	264.4	258.6	142.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	195.6	195.6	26.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	262.2	256.2	141.6	°C/W
R _{θJCbott}	Junction-to-case (bottom) thermal resistance	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application note](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	–40°C to 85°C		–40°C to 125°C RECOMMENDED			UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP	
V _{OH}		I _{OH} = –100μA	1.65V to 5.5V	V _{CC} – 0.1		V _{CC} – 0.15			V
		I _{OH} = –4mA	1.65V	1.2		1.2			
		I _{OH} = –8mA	2.3V	1.9		1.9			
		I _{OH} = –16mA	3V	2.4		2.4			
		I _{OH} = –24mA		2.3		2.3			
		I _{OH} = –32mA	4.5V	3.8		3.8			
V _{OL}		I _{OL} = 100μA	1.65V to 5.5V	0.1		0.1			V
		I _{OL} = 4mA	1.65V	0.45		0.45			
		I _{OL} = 8mA	2.3V	0.3		0.3			
		I _{OL} = 16mA	3V	0.4		0.4			
		I _{OL} = 24mA		0.55		0.55			
		I _{OL} = 32mA	4.5V	0.55		0.55			
I _I	A or B inputs	V _I = 5.5V or GND	0 to 5.5V	±5		±5			μA
I _{off}		V _I or V _O = 5.5V	0	±10		±10			μA
I _{CC}		V _I = 5.5V or GND, I _O = 0	1.65V to 5.5V	10		10			μA
ΔI _{CC}		One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	500		500			μA
C _i		V _I = V _{CC} or GND	3.3V	4		4			pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, T_A = –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	10	1	7.5	1	6.5	1	6	ns

5.7 Switching Characteristics, T_A = –40°C to 85°C

over recommended operating free-air temperature range, (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8V	V _{CC} = 2.5V	V _{CC} = 3.3V	V _{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	f = 10MHz	21	24	26	31	pF

5.9 Typical Characteristics

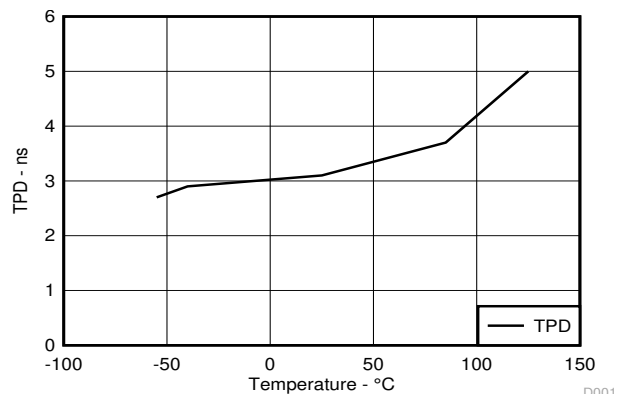


Figure 5-1. Propagation Delay (t_{pd}) Across Temperature at 3.3V V_{CC}

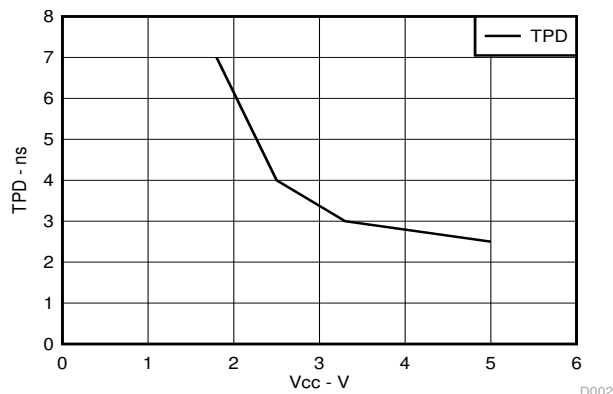
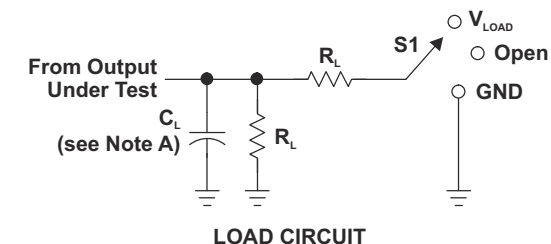


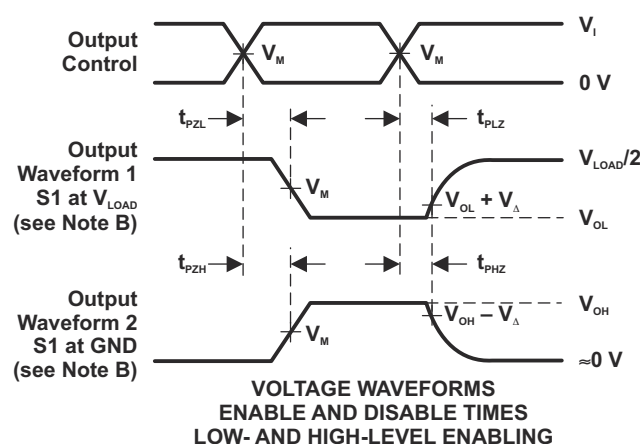
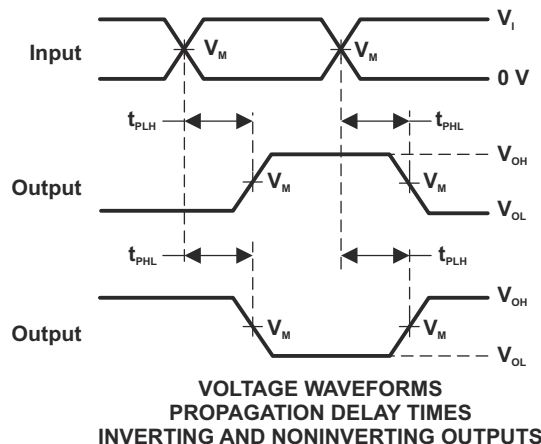
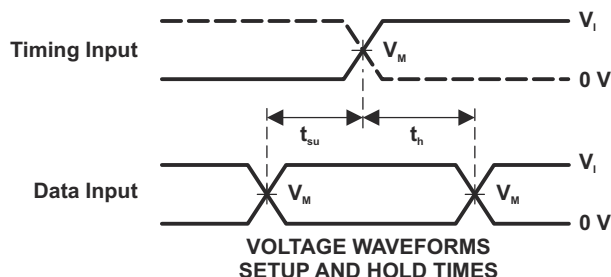
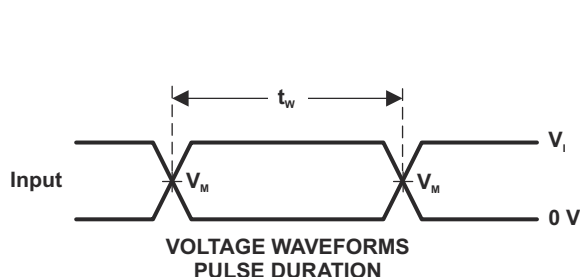
Figure 5-2. Propagation Delay (t_{pd}) Across V_{CC} at 25°C

6 Parameter Measurement Information



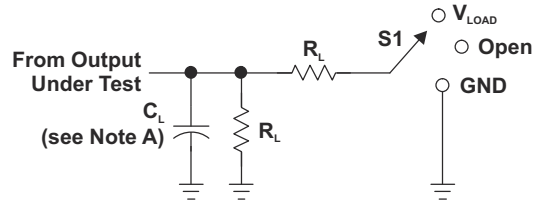
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{on} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

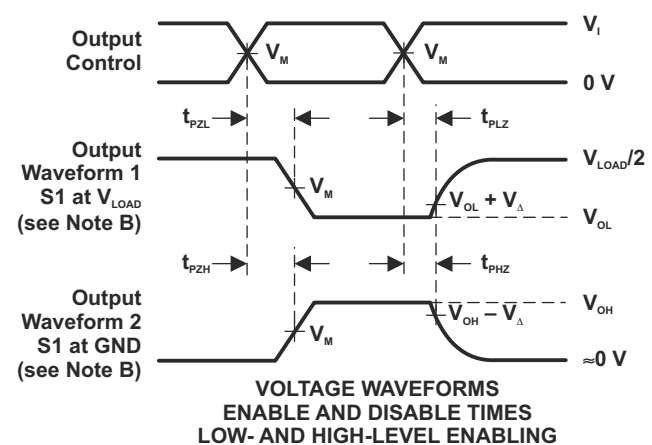
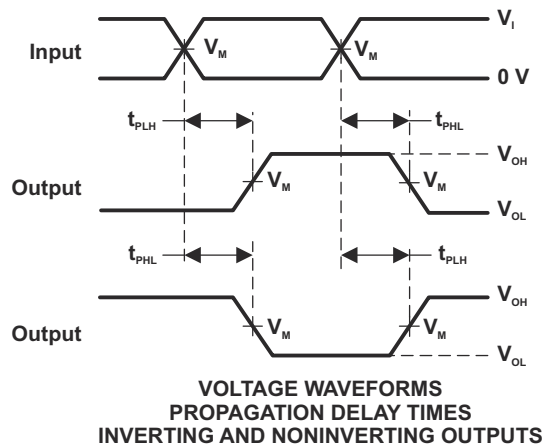
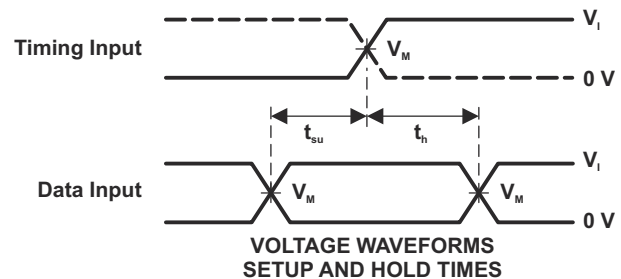
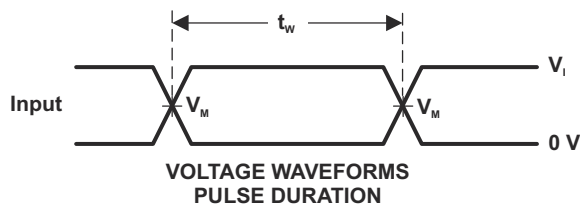
Figure 6-1. Load Circuit and Voltage Waveforms



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1G08-Q1 device contains one 2-input positive AND gate device and performs the Boolean function $Y = A \cdot B$ or $Y = \overline{A + B}$. SN74LVC1G08-Q1 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range from 1.65V to 5.5V
- Allows down voltage translation
- Inputs accept voltages to 5.5V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0V

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G08-Q1 is a high-drive CMOS device used for implementing AND logic with a high output drive, such as LED applications. The device produces 24mA of drive current at 3.3V making SN74LVC1G08-Q1 prime for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing the device to translate down to V_{CC} .

8.2 Typical Application

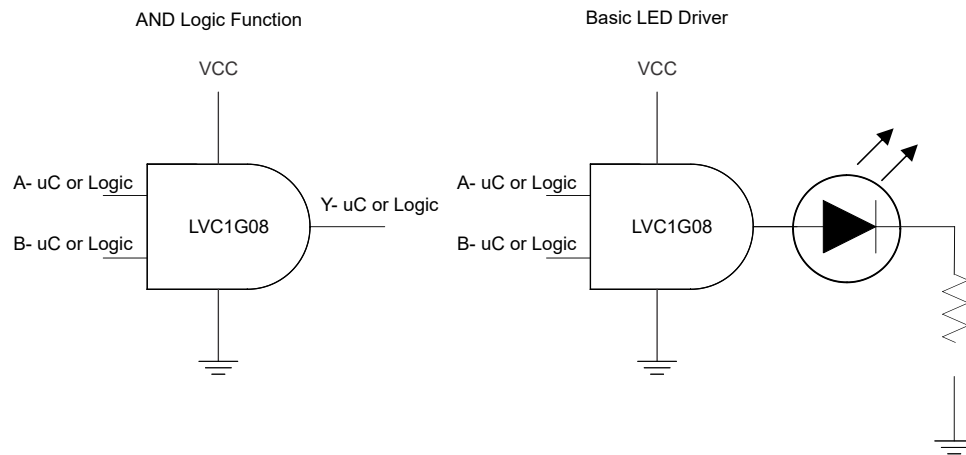


Figure 8-1. Typical Application Example

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents must not exceed (I_O max) per output and must not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - Outputs must not be pulled above V_{CC} .

8.2.3 Application Curves

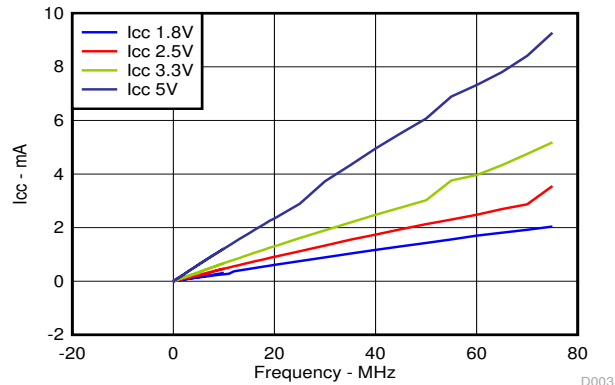


Figure 8-2. Icc vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

To prevent power disturbances, verify that each Vcc pin has a good bypass capacitor. For devices with a single supply, a 0.1μF capacitor is recommended and if there are multiple Vcc pins then 0.01μF or 0.022μF capacitor is recommended for each power pin. Parallel multiple bypass capacitors can reject different frequencies of noise. 0.1μF and 1μF capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, verify that the inputs do not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Do not leave such input pins unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level applicable to any particular unused input depends on the function of the device. Generally the level is be tied to Gnd or Vcc, whichever make more sense or is more convenient.

8.4.2 Layout Example

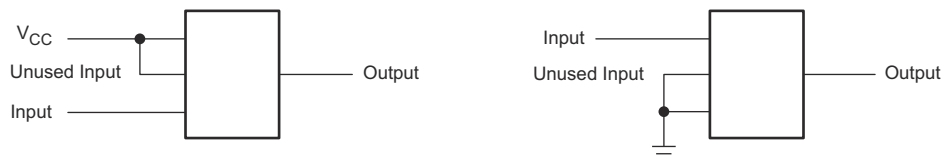


Figure 8-3. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 20, 2019 to August 14, 2026 (from Revision G (May 2019) to Revision H (August 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 209.4°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 132.5°C/W to: 263.7°C/W..	5
• Changed Junction-to-board characterization value for DBV package from: 118.1°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 48.8°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 117.4°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 244.2°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 156.1°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 130°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 47.2°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 130°C/W to: 256.2°C/W.....	5

Changes from Revision F (April 2008) to Revision G (June 2019)

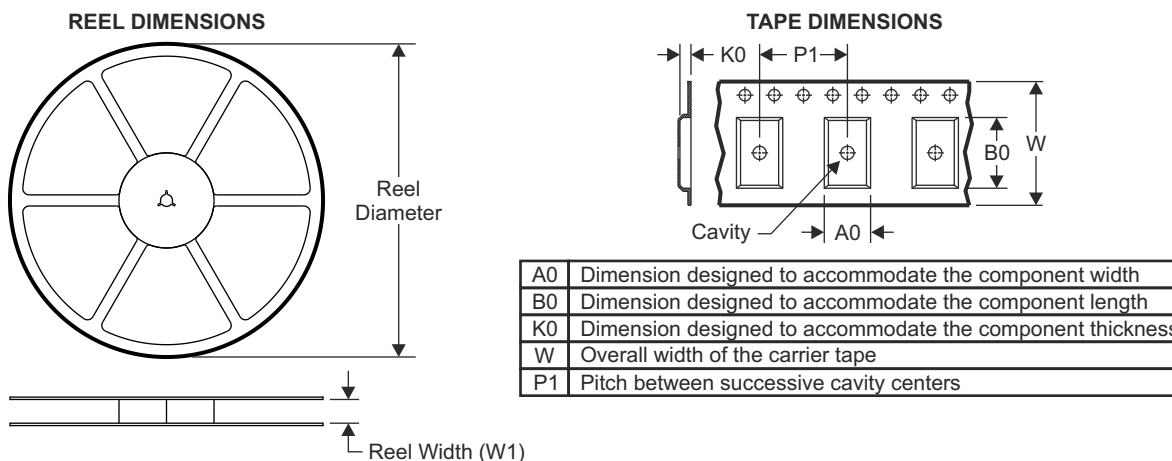
	Page
• Changed data sheet to new TI format	1
• Added DRY package to <i>Device Information</i> table.....	1
• Added <i>Thermal Information</i> table.	5
• Added <i>Typical Characteristics</i>	7
• Added <i>Detailed Description</i> section.	10
• Added <i>Application and Implementation</i> section.	11

- Added *Power Supply Recommendations* section. 12
- Added *Layout* section. 12

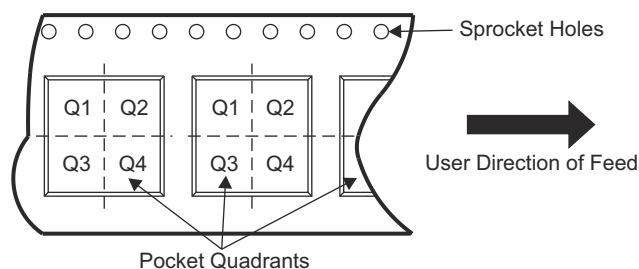
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

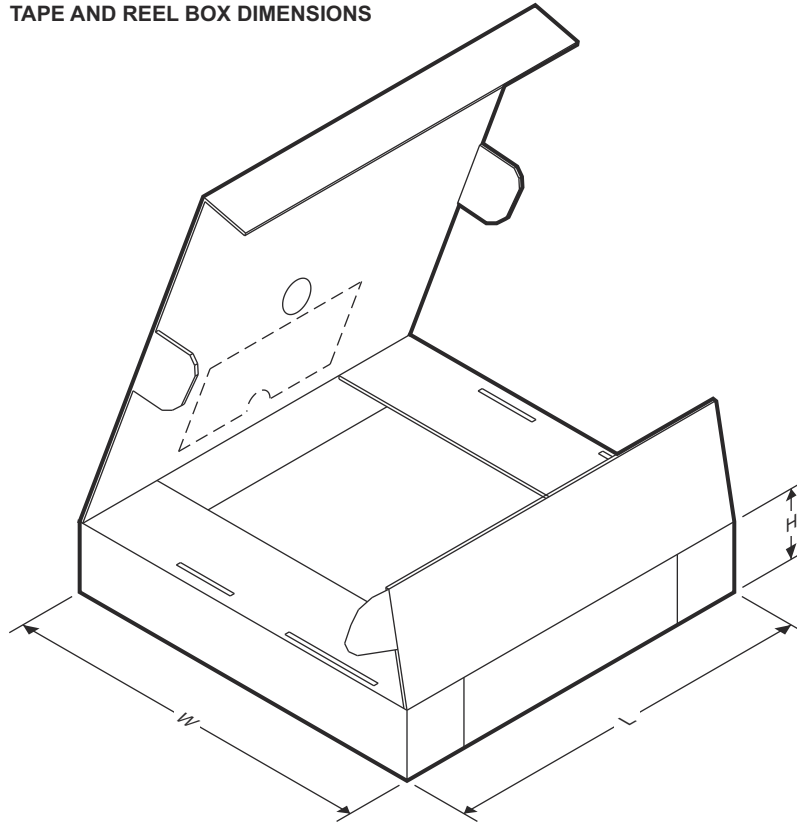


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G08-Q1	X2SON	DTX	5	3000	180	8.4	1	1.25	0.48	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G08-Q1	X2SON	DTX	5	3000	210	185	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G08QDBVRQ1G4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
74LVC1G08QDBVRQ1G4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
74LVC1G08QDCKRQ1G4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEO
74LVC1G08QDCKRQ1G4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEO
SN74LVC1G08IDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08IDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08IDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CEO
SN74LVC1G08QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(33H5, C08O)
SN74LVC1G08QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CEJ, CEO)
SN74LVC1G08QDRYRQ1	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EM
SN74LVC1G08QDRYRQ1.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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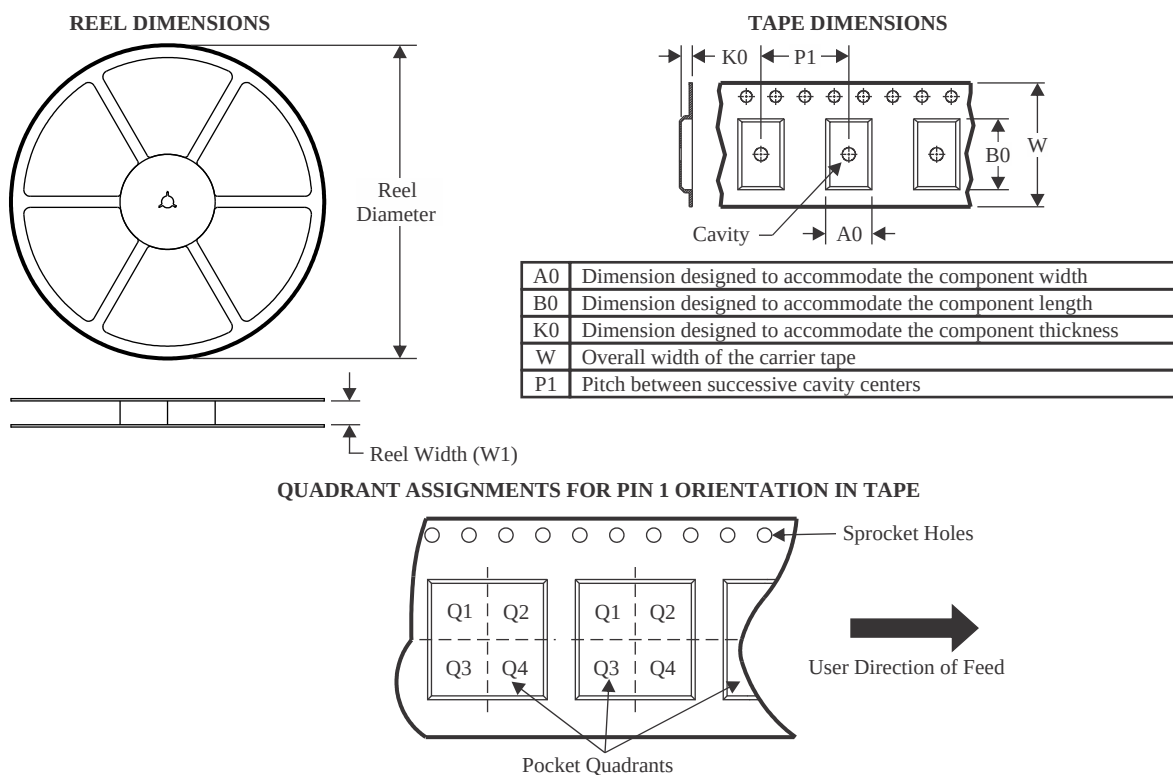
OTHER QUALIFIED VERSIONS OF SN74LVC1G08-Q1 :

- Catalog : [SN74LVC1G08](#)
- Enhanced Product : [SN74LVC1G08-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

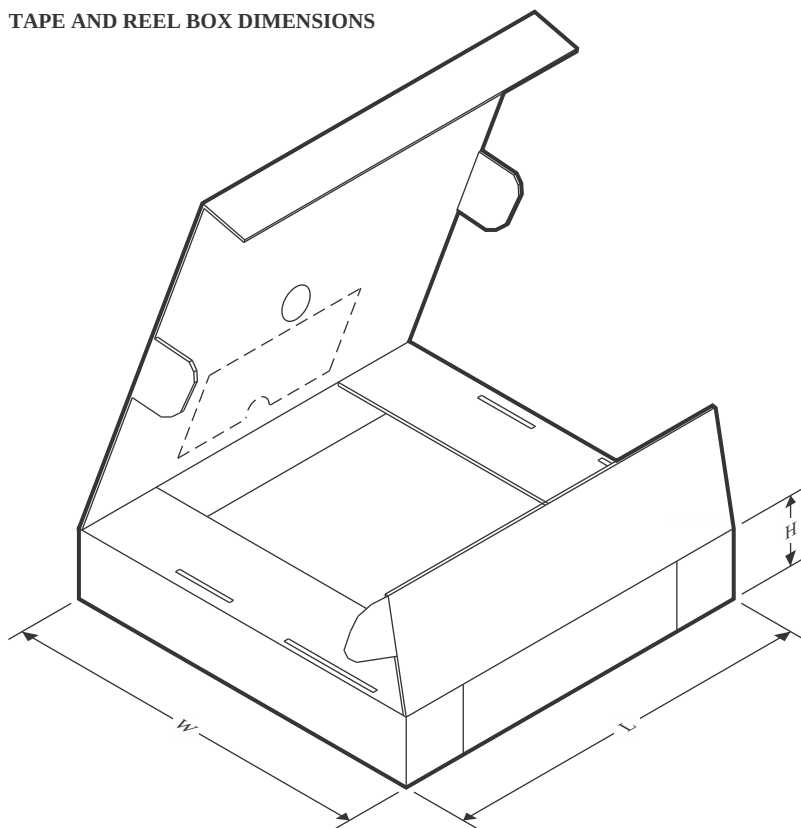
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
74LVC1G08QDCKRQ1G4	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
SN74LVC1G08QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



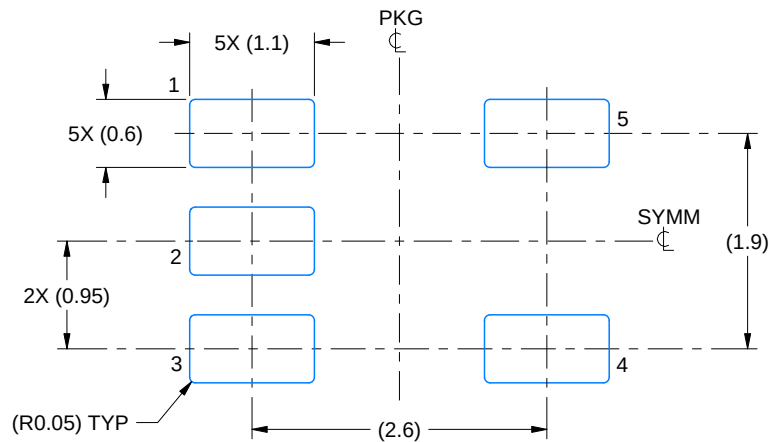
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	200.0	183.0	25.0
74LVC1G08QDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74LVC1G08QDCKRQ1G4	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G08IDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G08QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G08QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
SN74LVC1G08QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

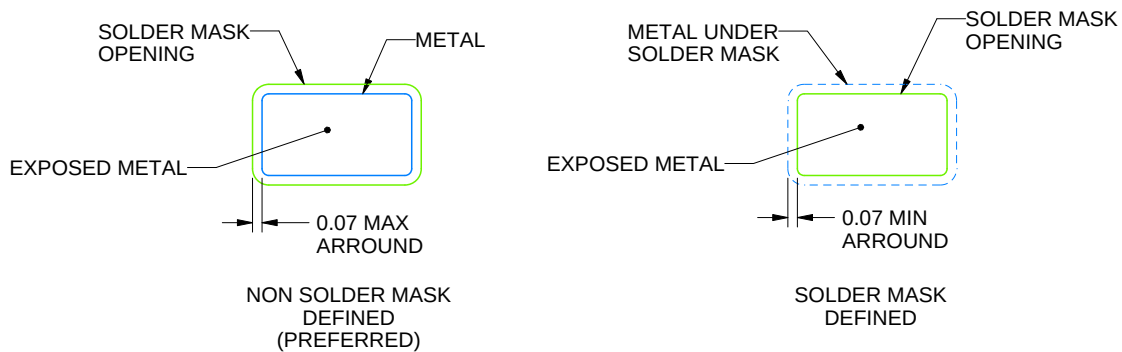
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

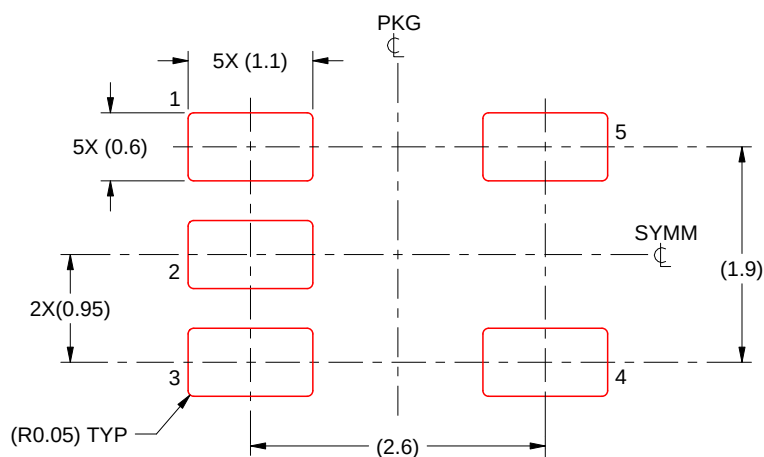
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

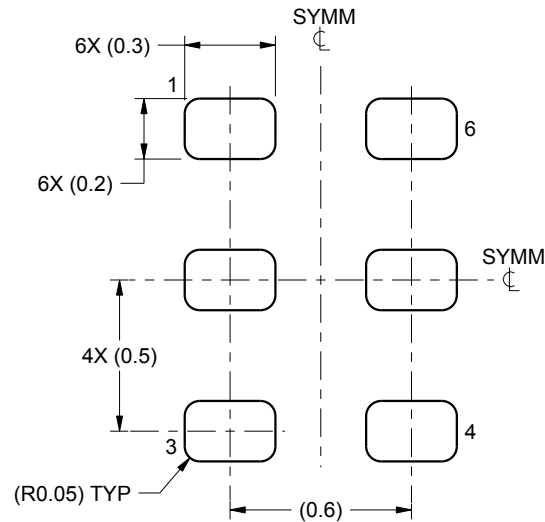
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

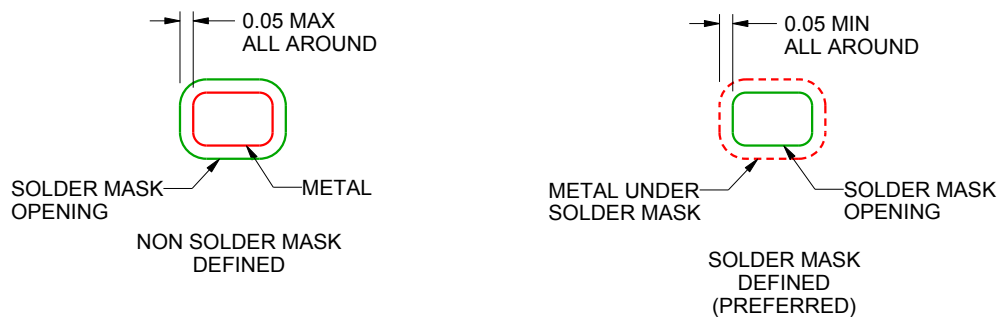
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

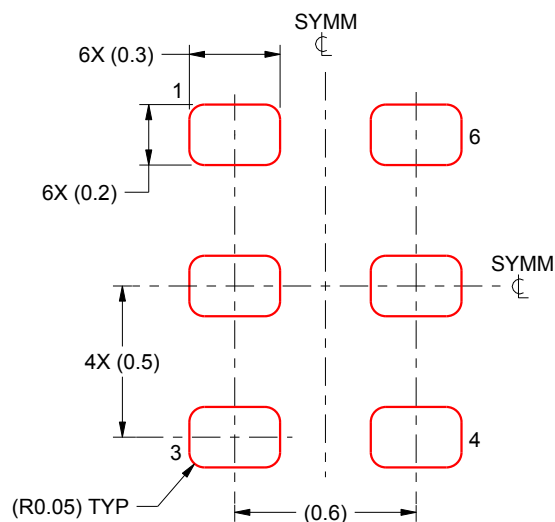
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

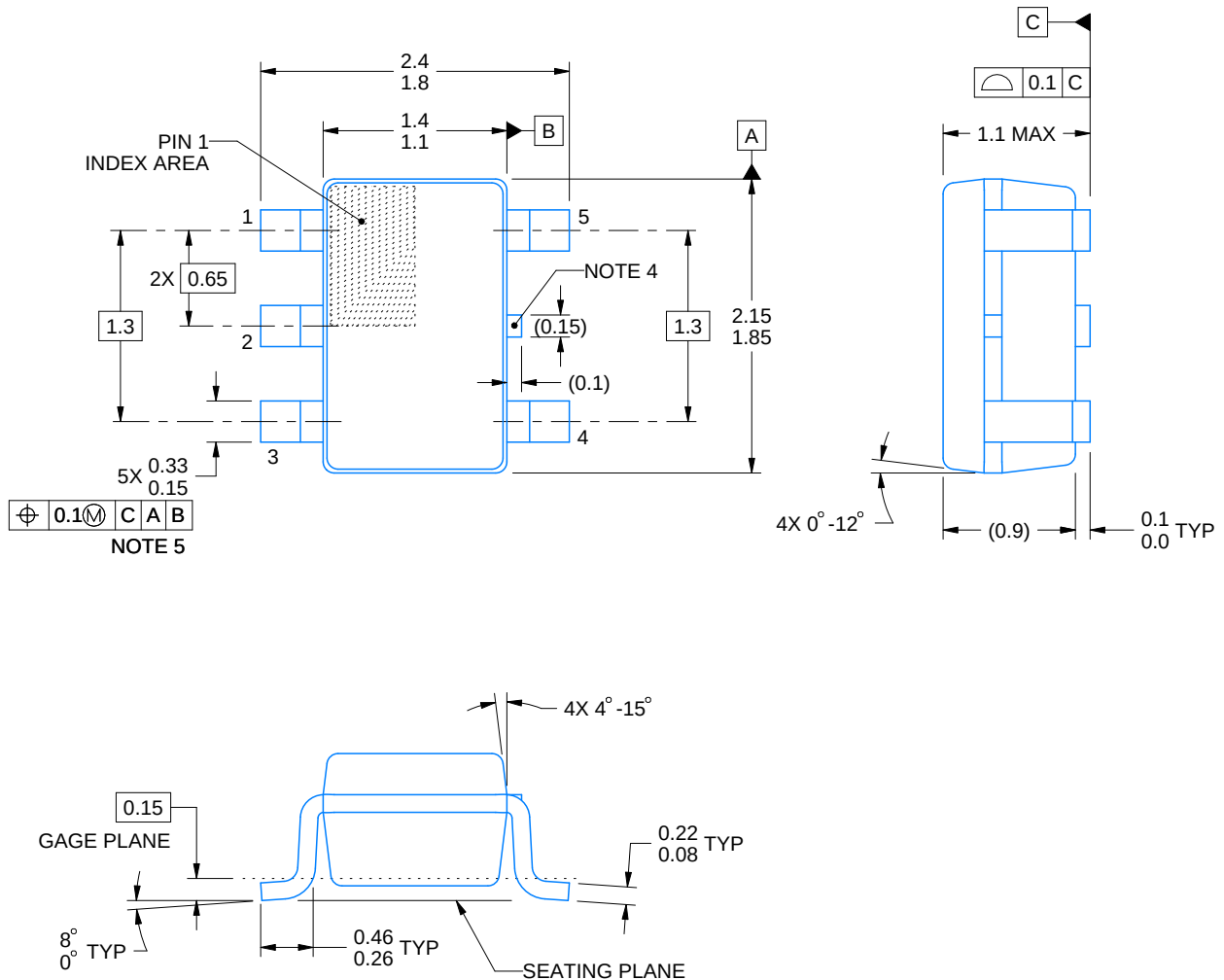


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

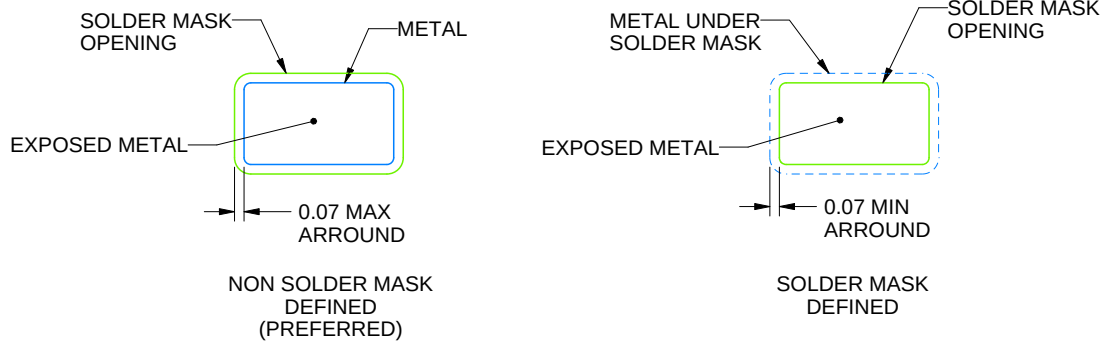
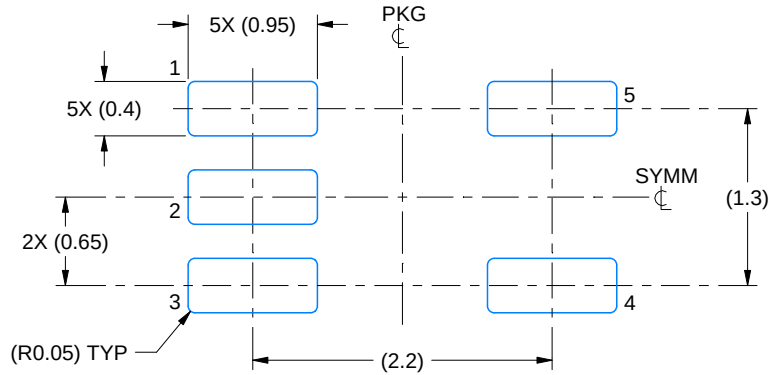
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4214834/G 11/2024

NOTES:

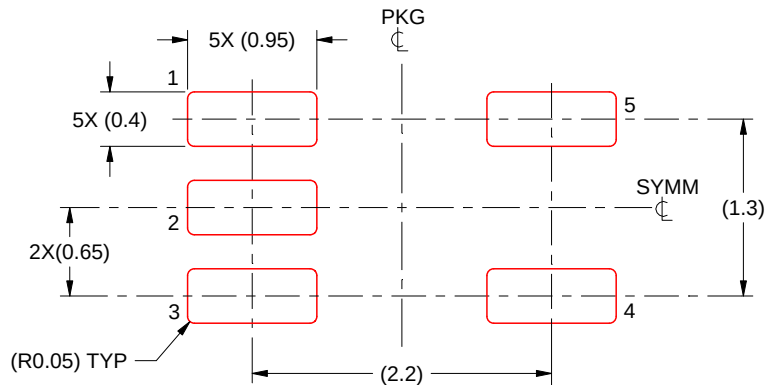
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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