

3-1/2 Digit Analog-to-Digital Converters

Features:

- Internal Reference with Low Temperature Drift:
 - TC7126: 80 ppm/°C, Typical
 - TC7126A: 35 ppm/°C, Typical
- Zero Reading with Zero Input
- Low Noise: 15 $\mu\text{V}_{\text{P-P}}$
- High Resolution: 0.05%
- Low Input Leakage Current: 1 pA Typ., 10 pA Max.
- Precision Null Detectors with True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation with Low-Power Dissipation: 500 μW Typ., 900 μW Max.

Applications:

- Thermometry
- Bridge Readouts: Strain Gauges, Load Cells, Null Detectors
- Digital Meters and Panel Meters:
 - Voltage/Current/Ohms/Power, pH
- Digital Scales, Process Monitors

Device Selection Table

Package Code	Package	Temperature Range
CPL	40-Pin PDIP	0°C to +70°C
IPL	40-Pin PDIP (TC7126 only)	-25°C to +85°C
CKW	44-Pin MQFP	0°C to +70°C

General Description:

The TC7126A is a 3-1/2 digit CMOS Analog-to-Digital Converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, a voltage reference, and a clock circuit are integrated on-chip. The TC7126A directly drives a Liquid Crystal Display (LCD) and includes a backplane driver.

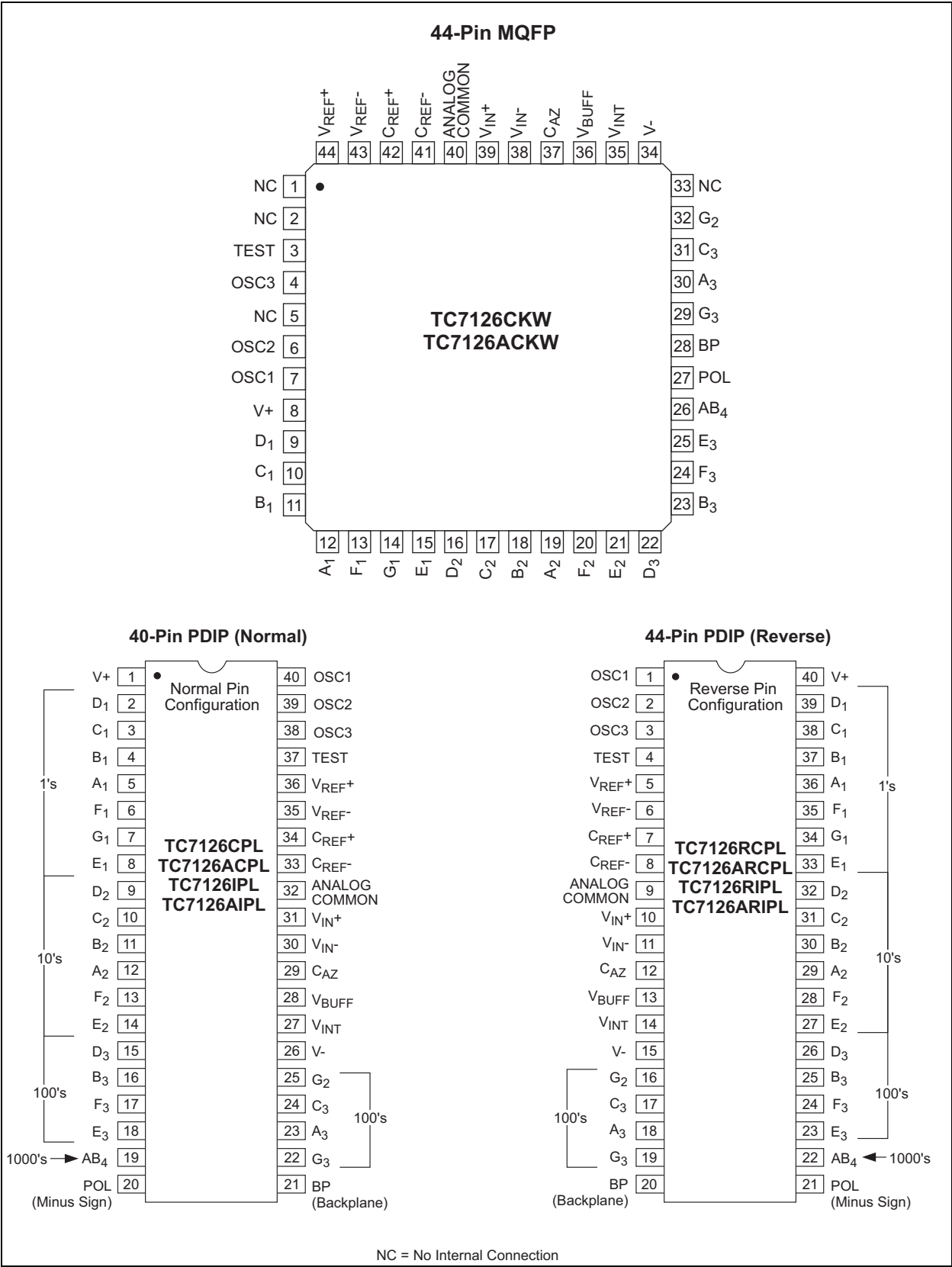
A cost-effective, high-resolution indicator meter needs just a display, four resistors, and four capacitors. The TC7126A's very low-power consumption and 9V battery operation make it ideal for portable applications.

The TC7126A reduces linearity error to less than 1 count. Rollover error (the difference in readings for equal magnitude but opposite polarity input signals) is below ± 1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 $\mu\text{V}_{\text{P-P}}$ noise performance ensures a "rock solid" reading, and the auto-zero cycle ensures a zero display reading with a 0V input.

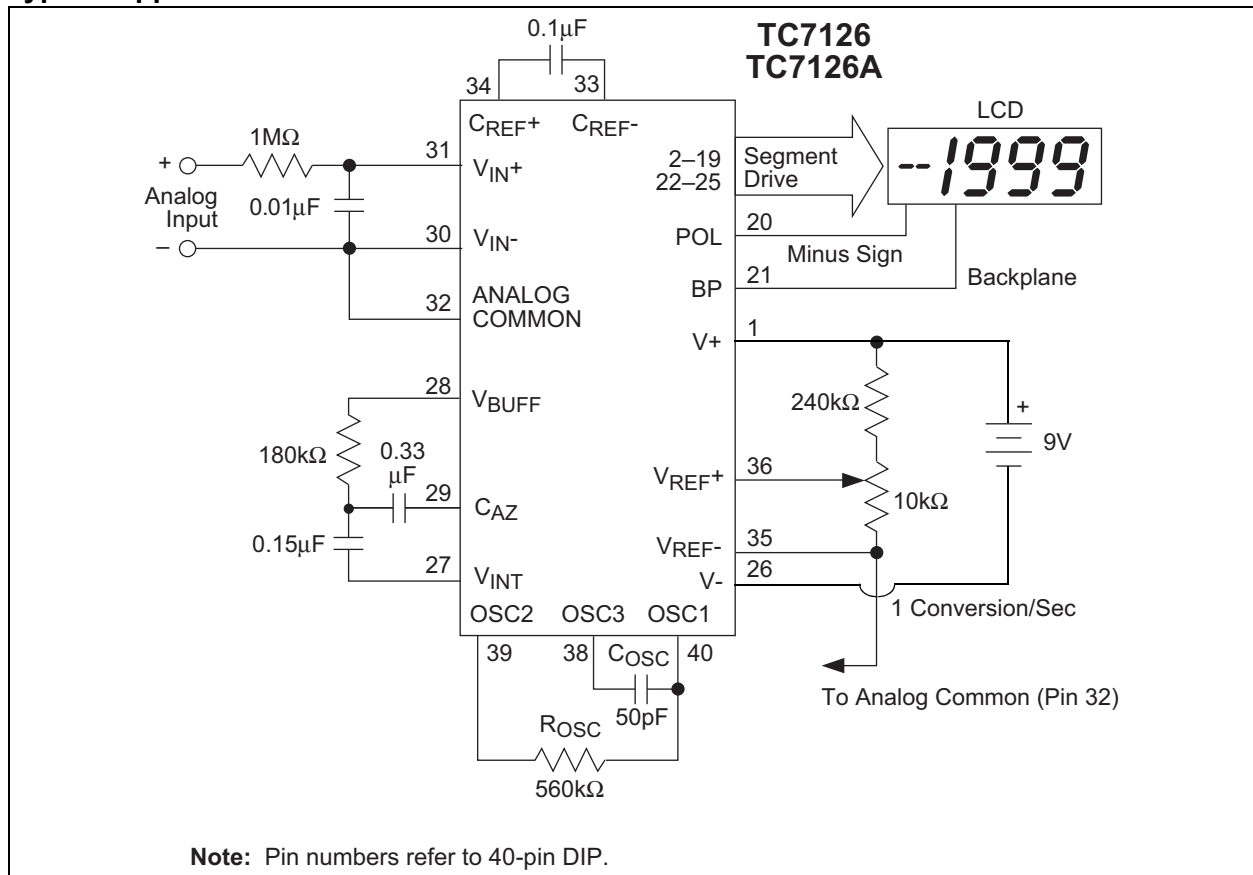
The TC7126A features a precision, low-drift internal voltage reference and is functionally identical to the TC7126. A low-drift external reference is not normally required with the TC7126A.

TC7126/A

Package Type

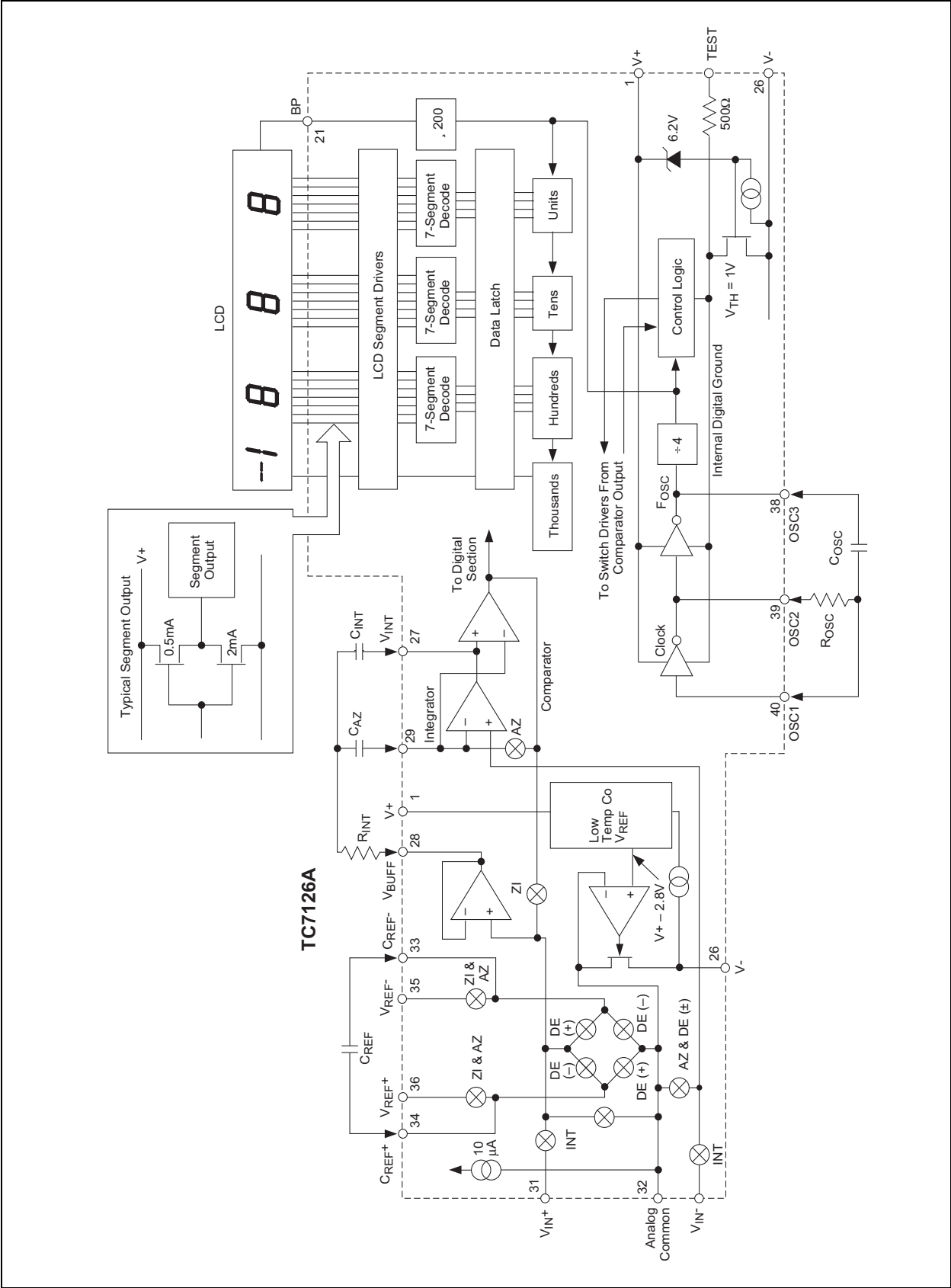


Typical Application



TC7126/A

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V+ to V-)..... 15V
 Analog Input Voltage (either Input) (**Note 1**) ... V+ to V-
 Reference Input Voltage (either Input)..... V+ to V-
 Clock Input Test to V+
 Package Power Dissipation ($T_A \leq +70^\circ\text{C}$) (**Note 2**):
 44-Pin MQFP 1.00W
 44-Pin PDIP 1.23W
 Operating Temperature Range:
 C (Commercial) Devices 0°C to $+70^\circ\text{C}$
 I (Industrial) Devices -25°C to $+85^\circ\text{C}$
 Storage Temperature Range..... -65°C to $+150^\circ\text{C}$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: TC7126/A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $V_S = +9\text{V}$, $f_{\text{CLK}} = 16\text{kHz}$, and $T_A = +25^\circ\text{C}$, unless otherwise noted.						
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Input						
Z_{IR}	Zero Input Reading	-000.0	± 000.0	+000.0	Digital Reading	$V_{\text{IN}} = 0\text{V}$ Full Scale = 200 mV
Z_{RD}	Zero Reading Drift	—	0.2	1	$\mu\text{V}/^\circ\text{C}$	$V_{\text{IN}} = 0\text{V}$, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
	Ratiometric Reading	999	999/1000	1000	Digital Reading	$V_{\text{IN}} = V_{\text{REF}}$, $V_{\text{REF}} = 100\text{ mV}$
NL	Linearity Error	-1	± 0.2	1	Count	Full Scale = 200 mV or 2V Max Deviation From Best Fit Straight Line
	Rollover Error	-1	± 0.2	1	Count	$V_{\text{IN}} = V_{\text{IN}+} \approx 200\text{ mV}$
e_{N}	Noise	—	15	—	$\mu\text{V}_{\text{P-P}}$	$V_{\text{IN}} = 0\text{V}$, Full Scale = 200 mV
I_{L}	Input Leakage Current	—	1	10	pA	$V_{\text{IN}} = 0\text{V}$
CMRR	Common-Mode Rejection Ratio	—	50	—	$\mu\text{V}/\text{V}$	$V_{\text{CM}} = \pm 1\text{V}$, $V_{\text{IN}} = 0\text{V}$ Full Scale = 200 mV
	Scale Factor Temperature Coefficient	—	1	5	ppm/ $^\circ\text{C}$	$V_{\text{IN}} = 199\text{ mV}$, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ Ext. Ref. Temp Coeff. = 0ppm/ $^\circ\text{C}$
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	—	80	—	ppm/ $^\circ\text{C}$	TC7126 (Note 7 , Note 8)
		—	35	75	ppm/ $^\circ\text{C}$	TC7126A (Note 7 , Note 8)
		—	35	100	ppm/ $^\circ\text{C}$	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ (“I” Device) (TC7126A)
V_{C}	Analog Common Voltage	2.7	3.05	3.35	V	(Note 7)

- Note 1:** Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 100\text{ }\mu\text{A}$.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
Note 3: Refer to “Differential Input” discussion.
Note 4: Backplane drive is in phase with segment drive for “OFF” segment, 180° out of phase for “ON” segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
Note 5: See “Typical Application”.
Note 6: During Auto-Zero phase, current is 10-20 μA higher. A 48 kHz oscillator increases current by 8 μA (Typical). Common current is not included.
Note 7: $250\text{ k}\Omega$ Between Common and V+
Note 8: $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (“C” Devices)

TC7126/A

TABLE 1-1: TC7126/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: $V_S = +9V$, $f_{CLK} = 16kHz$, and $T_A = +25^\circ C$, unless otherwise noted.						
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	4	5	6	V_{P-P}	V_+ to $V_- = 9V$
V_{BD}	LCD Backplane Drive Voltage	4	5	6	V_{P-P}	V_+ to $V_- = 9V$
Power Supply						
I_S	Power Supply Current	—	55	100	μA	$V_{IN} = 0V$, V_+ to $V_- = 9V$ (Note 6)

- Note**
- 1: Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 100 \mu A$.
 - 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
 - 3: Refer to "Differential Input" discussion.
 - 4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
 - 5: See "Typical Application".
 - 6: During Auto-Zero phase, current is 10-20 μA higher. A 48 kHz oscillator increases current by 8 μA (Typical). Common current is not included.
 - 7: 250 k Ω Between Common and V_+
 - 8: $0^\circ C \leq T_A \leq +70^\circ C$ ("C" Devices)

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP) Normal	(Reversed)	Symbol	Description
1	(40)	V+	Positive supply voltage.
2	(39)	D ₁	Activates the D section of the units display.
3	(38)	C ₁	Activates the C section of the units display.
4	(37)	B ₁	Activates the B section of the units display.
5	(36)	A ₁	Activates the A section of the units display.
6	(35)	F ₁	Activates the F section of the units display.
7	(34)	G ₁	Activates the G section of the units display.
8	(33)	E ₁	Activates the E section of the units display.
9	(32)	D ₂	Activates the D section of the tens display.
10	(31)	C ₂	Activates the C section of the tens display.
11	(30)	B ₂	Activates the B section of the tens display.
12	(29)	A ₂	Activates the A section of the tens display.
13	(28)	F ₂	Activates the F section of the tens display.
14	(27)	E ₂	Activates the E section of the tens display.
15	(26)	D ₃	Activates the D section of the hundreds display.
16	(25)	B ₃	Activates the B section of the hundreds display.
17	(24)	F ₃	Activates the F section of the hundreds display.
18	(23)	E ₃	Activates the E section of the hundreds display.
19	(22)	AB ₄	Activates both halves of the “1” in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	LCD backplane drive output (TC7106A). Digital Ground (TC7107A).
22	(19)	G ₃	Activates the G section of the hundreds display.
23	(18)	A ₃	Activates the A section of the hundreds display.
24	(17)	C ₃	Activates the C section of the hundreds display.
25	(16)	G ₂	Activates the G section of the tens display.
26	(15)	V-	Negative power supply voltage.
27	(14)	V _{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance buildup will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent rollover errors. See Section 6.3 “Integrating Capacitor (CINT)” for additional details.
28	(13)	V _{BUFF}	Integration resistor connection. Use a 180 kΩ resistor for a 200 mV full-scale range and a 1.8 MΩ resistor for a 2V full scale range.
29	(12)	C _{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.33 μF capacitor for 200 mV full scale, and a 0.033 μF capacitor for 2V full scale. See Section 6.1 “Auto-Zero Capacitor (CAZ)” for additional details.
30	(11)	V _{IN-}	The analog LOW input is connected to this pin.
31	(10)	V _{IN+}	The analog HIGH input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the Analog Common-mode voltage for battery operation, or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See Section 7.3 “Analog Common (Pin 32)” for additional details.
33	(8)	C _{REF-}	See Pin 34.

TC7126/A

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP) Normal	(Reversed)	Symbol	Description
34	(7)	C _{REF} ⁺	A 0.1 μ F capacitor is used in most applications. If a large Common-mode voltage exists (for example, the V _{IN} ⁻ pin is not at analog common) and a 200 mV scale is used, a 1 μ F capacitor is recommended and will hold the rollover error to 0.5 count.
35	(6)	V _{REF} ⁻	See Pin 36.
36	(5)	V _{REF} ⁺	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between Pins 35 and 36 for 199.9 mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See Section 6.6 "Reference Voltage Selection" for additional information.
37	(4)	TEST	Lamp test. When pulled HIGH (to V ₊), all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See Section 7.4 "TEST (Pin 37)" for additional information.
38	(3)	OSC3	See Pin 40.
39	(2)	OSC2	See Pin 40.
40	(1)	OSC1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings, 39 per second), connect Pin 40 to the junction of a 180 k Ω resistor and a 50 pF capacitor. The 180 k Ω resistor is tied to Pin 39, and the 50 pF capacitor is tied to Pin 38.

3.0 DETAILED DESCRIPTION

(All pin designations refer to 40-pin PDIP.)

3.1 Dual-Slope Conversion Principles

The TC7126A is a dual-slope, integrating analog-to-digital converter. This section describes the operating theory of the TC7126/A.

The conventional dual-slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (De-integration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An oppositely polarized, constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}) (see Figure 3-1).

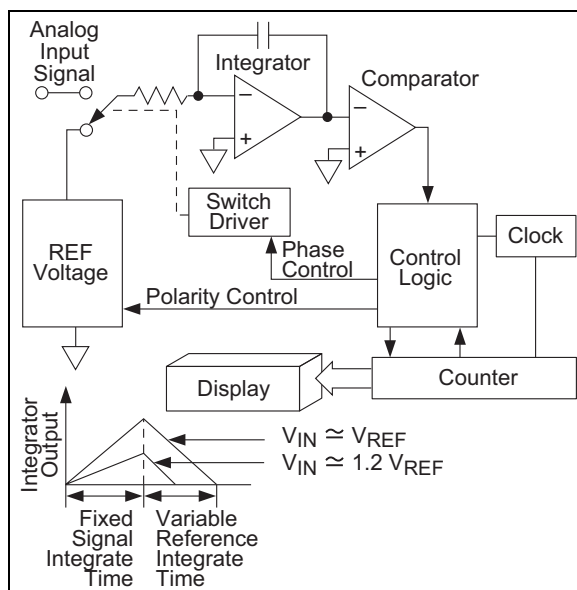


FIGURE 3-1: Basic Dual-Slope Converter.

In a simple dual-slope converter, a complete conversion requires the integrator output to “ramp-up” and “ramp-down.”

A simple mathematical equation relates the input signal, reference voltage and integration time:

EQUATION 3-1:

$$\frac{1}{RC} \int_0^{T_{SI}} V_{IN}(t) dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference voltage

T_{SI} = Signal integration time (fixed)

T_{RI} = Reference voltage integration time (variable)

For a constant V_{IN} :

EQUATION 3-2:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The accuracy of a dual-slope converter is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated or averaged to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period (see Figure 3-2).

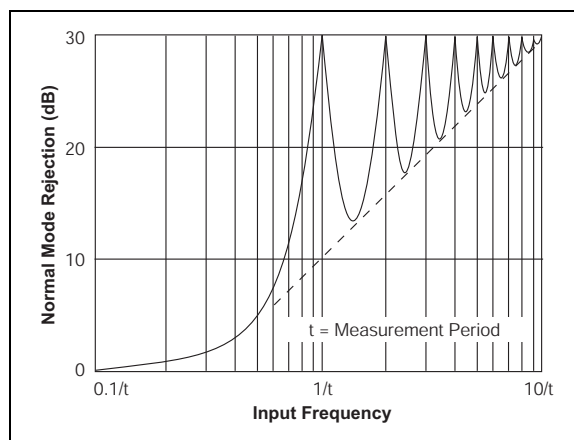


FIGURE 3-2: Normal Mode Rejection of Dual-Slope Converter.

4.0 ANALOG SECTION

In addition to the basic integrate and de-integrate dual-slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle eliminates offset voltage errors from the buffer amplifier, integrator, and comparator during the conversion. As a result, a true digital zero reading is achieved without external adjustment potentiometers. A complete conversion consists of three phases:

1. Auto-Zero phase
2. Signal Integrate phase
3. Reference Integrate phase

4.1 Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 μ V to 15 μ V. The auto-zero cycle length is 1000 to 3000 clock periods.

4.2 Signal Integrate Phase

The auto-zero loop is entered, and the internal differential inputs connect to V_{IN+} and V_{IN-} . The differential input signal is integrated for a fixed time period. The TC7126/A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

EQUATION 4-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where: F_{OSC} = external clock frequency.

The differential input voltage must be within the device Common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN-} should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

4.3 Reference Integrate Phase

The third phase is reference integrate, or de-integrate. V_{IN-} is internally connected to analog common, and V_{IN+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

EQUATION 4-2:

$$1000 \frac{V_{IN}}{V_{REF}}$$

5.0 DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD, including an LCD backplane driver. The backplane frequency is the external clock frequency divided by 800. For 3 conversions per second, the backplane frequency is 60 Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is OFF. An out-of-phase segment drive signal causes the segment to be ON (visible). This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN+} and V_{IN-} are reversed, this indicator reverses.

On the TC7126A, when the TEST pin is pulled to V+, all segments are turned ON and the display reads -1888. During this mode, LCD segments have a constant DC voltage impressed.

Note: Do not leave the display in this mode for more than several minutes. LCDs may be destroyed if operated with DC levels for extended periods.

The display font and segment drive assignment are shown in Figure 5-1.

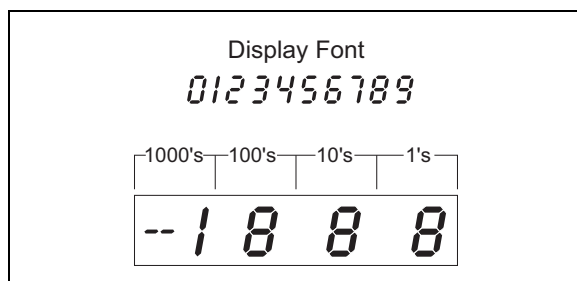


FIGURE 5-1: Display Font and Segment Assignment.

5.1 System Timing

The oscillator frequency is divided by four prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

1. Auto-Zero Phase: 1000 to 3000 counts (4000 to 12,000 clock pulses).

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

2. Signal Integrate: 1000 counts (4000 clock pulses).

This time period is fixed. The integration period is:

EQUATION 5-1:

$$T_{SI} = 4000 \frac{1}{F_{OSC}}$$

Where: F_{OSC} is the externally set clock frequency.

3. Reference Integrate: 0 to 2000 counts (0 to 8000 clock pulses).

The TC7126A is a drop-in replacement for the TC7126 and ICL7126, offering a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

6.0 COMPONENT VALUE SELECTION

6.1 Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.33 μF capacitor is recommended for 200 mV full-scale applications, where 1 LSB is 100 μV . A 0.033 μF capacitor is adequate for 2.0V full-scale applications. A Mylar-type dielectric capacitor is adequate.

6.2 Reference Voltage Capacitor (C_{REF})

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on C_{REF} . A 0.1 μF capacitor is acceptable when V_{REF-} is tied to analog common. If a large Common-mode voltage exists ($V_{REF-} \neq$ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 μF . Rollover error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

6.3 Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize the integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a $\pm 2\text{V}$ full scale integrator output swing is satisfactory. For 3 readings per second ($F_{OSC} = 48 \text{ kHz}$), a 0.047 μF value is suggested. For 1 reading per second, 0.15 μF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal $\pm 2\text{V}$ integrator swing.

An exact expression for C_{INT} is:

EQUATION 6-1:

$$C_{INT} = \frac{(4000) \left(\frac{1}{F_{OSC}} \right) \left(\frac{V_{FS}}{R_{INT}} \right)}{V_{INT}}$$

Where:

F_{OSC} = Clock frequency at Pin 38

V_{FS} = Full scale input voltage

R_{INT} = Integrating resistor

V_{INT} = Desired full scale integrator output swing

At 3 readings per second, a 750 Ω resistor should be placed in series with C_{INT} . This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

6.4 Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 μA . The integrator and buffer can supply 1 μA drive current with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PCB leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 k Ω . A 2V full scale requires 1.8 M Ω .

TABLE 6-1: RECOMMENDED COMPONENT VALUE VS. NOMINAL FULL SCALE VALUE

Component Value	Nominal Full Scale Voltage	
	200 mV	2V
C_{AZ}	0.33 μF	0.033 μF
R_{INT}	180 k Ω	1.8 M Ω
C_{INT}	0.047 μF	0.047 μF

Note: $F_{OSC} = 48 \text{ kHz}$ (3 readings per sec).

6.5 Oscillator Components

C_{OSC} should be 50 pF; R_{OSC} is selected from the equation:

EQUATION 6-2:

$$F_{OSC} = \frac{0.45}{RC}$$

For a 48 kHz clock (3 conversions per second), $R = 180 \text{ k}\Omega$.

Note that F_{OSC} is divided by 4 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing F_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60Hz. Oscillator frequencies of 24 kHz, 12 kHz, 80 kHz, 60 kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 20 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz.

6.6 Reference Voltage Selection

A full scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full Scale Voltage*	V_{REF}
20 mV	100 mV
2V	1V

Note: $V_{FS} = 2V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in² is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN-} . The transducer output is connected between V_{IN+} and analog common.

7.3 Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below $V+$. The potential is between 2.7V and 3.35V below $V+$. Analog common is tied internally to an N-channel FET capable of sinking 100 μ A. This FET will hold the common line at 3V should an external load attempt to pull the common line toward $V+$. Analog common source current is limited to 1 μ A. Therefore, analog common can easily be pulled to a more negative voltage (i.e., below $V+ - 3V$).

The TC7126A connects the internal V_{IN+} and V_{IN-} inputs to analog common during the auto-zero phase. During the reference integrate phase, V_{IN-} is connected to analog common. If V_{IN-} is not externally connected to analog common, a Common-mode voltage exists, but is rejected by the converter's 86 dB Common-mode rejection ratio. In battery operation, analog common and V_{IN-} are usually connected, removing Common-mode voltage concerns. In systems where V_{IN-} is connected to power supply ground or to a given voltage, analog common should be connected to V_{IN-} .

The analog common pin serves to set the analog section reference, or common point. The TC7126A is specifically designed to operate from a battery, or in any measurement system where input signals are not referenced (float) with respect to the TC7126A's power source. The analog common potential of $V+ - 3V$ gives a 7V end-of-battery-life voltage. The common potential has a 0.001%/° voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V+ - V- > 7V$), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°C). This potential can be used to generate the TC7126A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See [Section 7.5 "TC7126A Internal Voltage Reference"](#), for additional details.

7.4 TEST (Pin 37)

The TEST pin potential is 5V less than $V+$. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500 Ω resistor. The TEST pin load should be no more than 1mA. See [Section 5.0 "DIGITAL SECTION"](#), for additional information on using TEST as a negative digital logic supply.

If TEST is pulled HIGH (to $V+$), all segments plus the minus sign will be activated.

Note: Do not operate in this mode for more than several minutes. With $TEST = V+$, the LCD segments are impressed with a DC voltage, which will destroy the LCD.

7.5 TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved ([Figure 7-3](#)). The "A" version of the industry-standard TC7126 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. [Figure 7-4](#) shows analog common supplying the necessary voltage reference for the TC7126A.

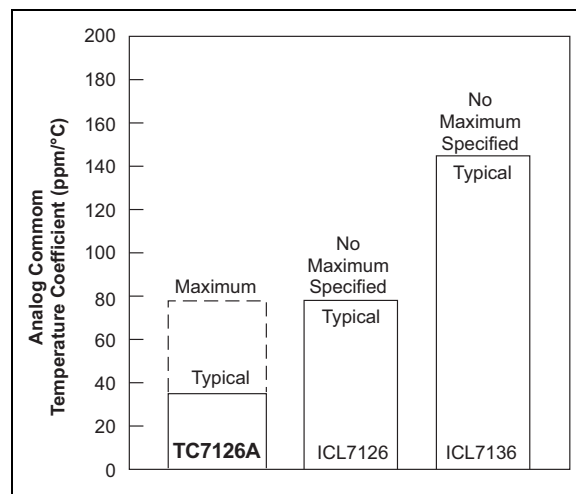


FIGURE 7-3: Analog Common Temp. Coefficient.

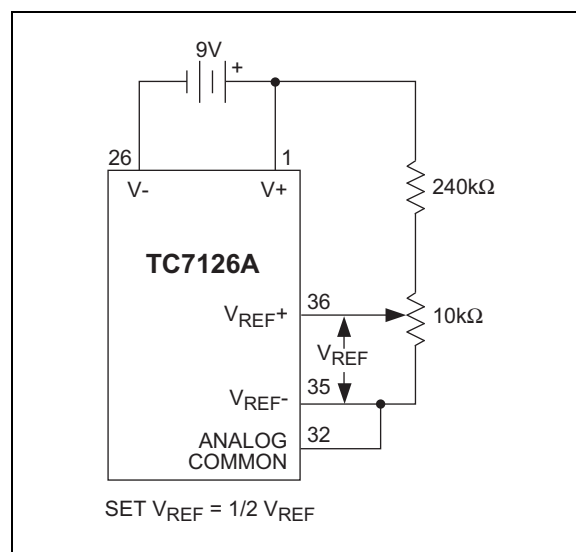


FIGURE 7-4: TC7126A Internal Voltage Reference Connection.

TC7126/A

8.0 TYPICAL APPLICATIONS

8.1 Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin; its potential is approximately 5V below V+ (see Figure 8-1).

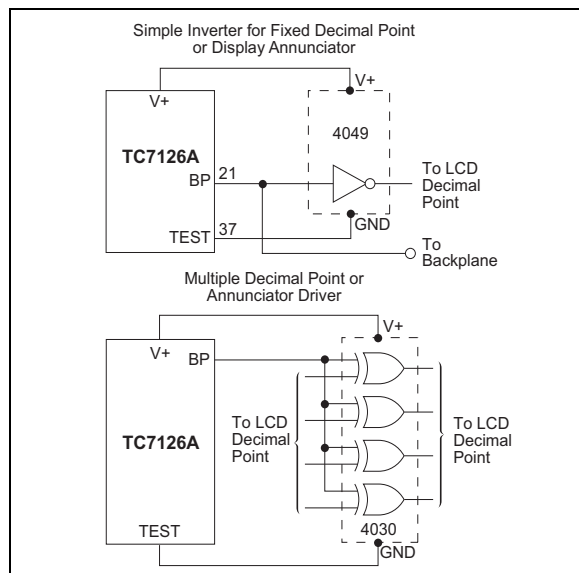


FIGURE 8-1: Decimal Point and Annunciator Drives.

8.2 Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric reading possible. In a ratio-metric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is placed in series with a known standard, and a current is passed through the pair. The voltage developed across the unknown is applied to the input, and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

EQUATION 8-1:

$$\text{Displayed (Reading)} = \frac{R_{\text{UNKNOWN}}}{R_{\text{STANDARD}}} \times 1000$$

The display will overrange for $R_{\text{UNKNOWN}} \geq 2 \times R_{\text{STANDARD}}$ (see Figure 8-2).

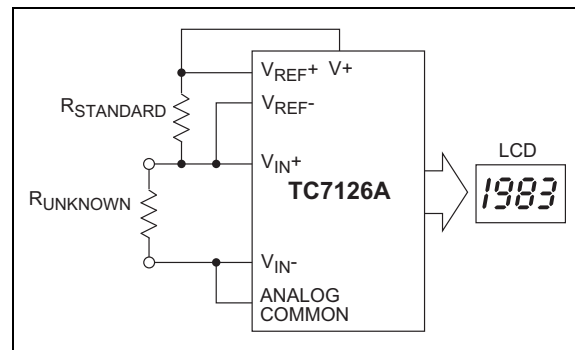


FIGURE 8-2: Low Parts Count Ratiometric Resistance Measurement.

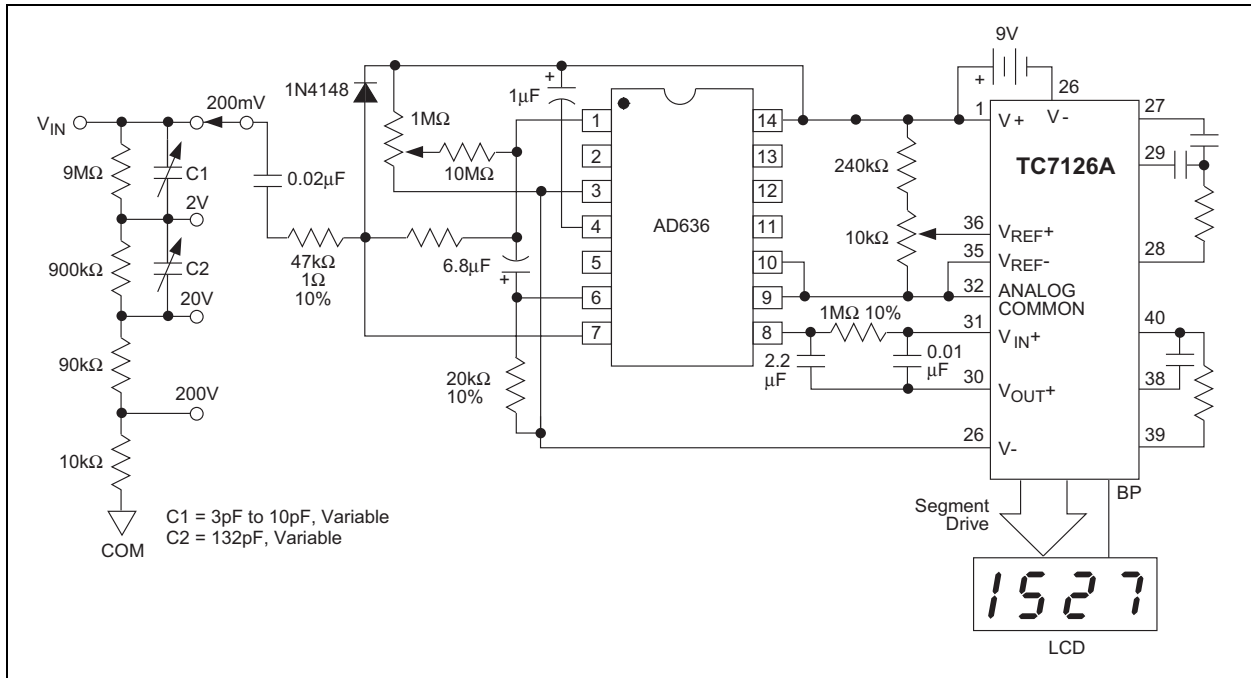


FIGURE 8-3: 3-1/2 Digit True RMS AC DMM.

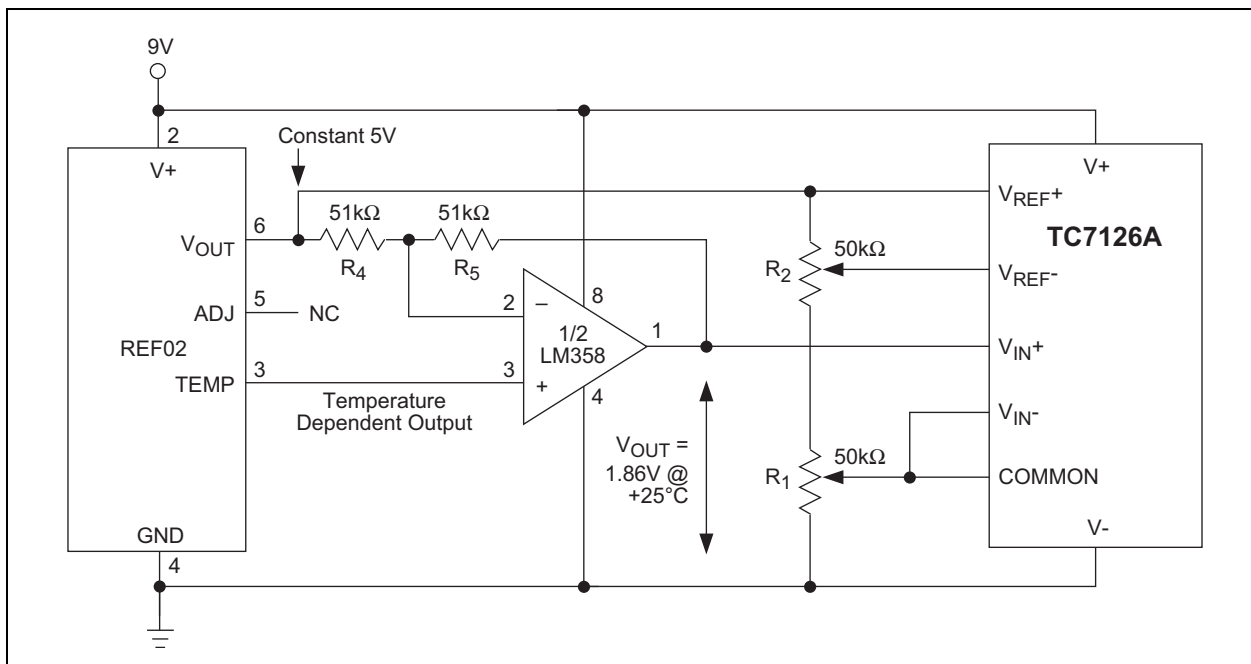


FIGURE 8-4: Integrated Circuit Temperature Sensor.

TC7126/A

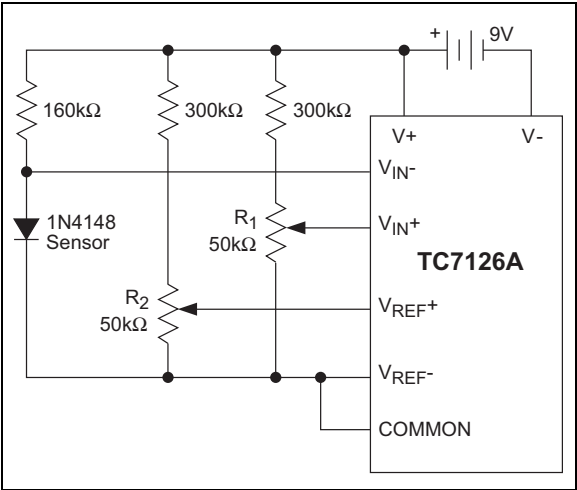


FIGURE 8-5: *Temperature Sensor.*

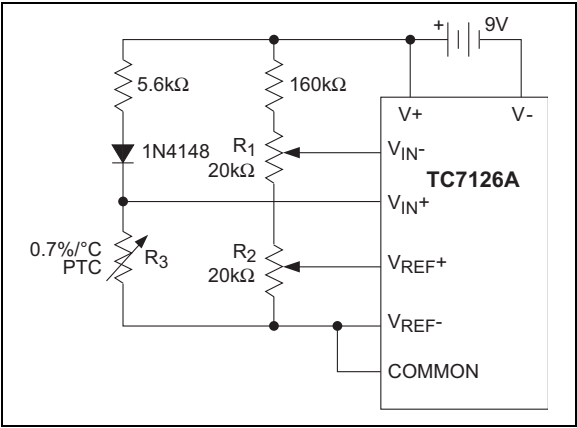
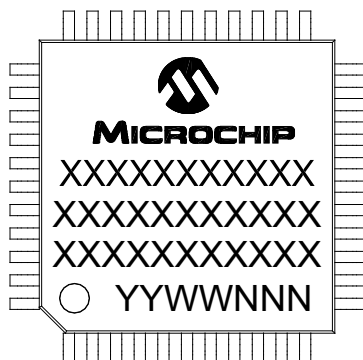


FIGURE 8-6: *Positive Temperature Coefficient Resistor Temperature Sensor.*

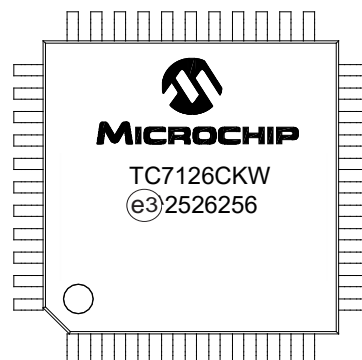
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

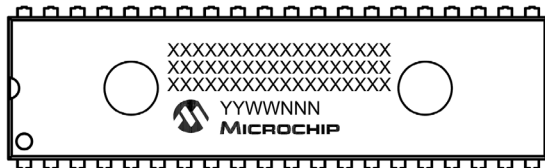
44-Lead MQFP (4x4x0.9 mm)



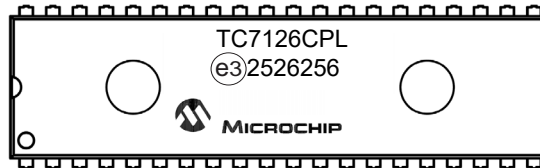
Example



40-Lead PDIP (5.30 mm)



Example



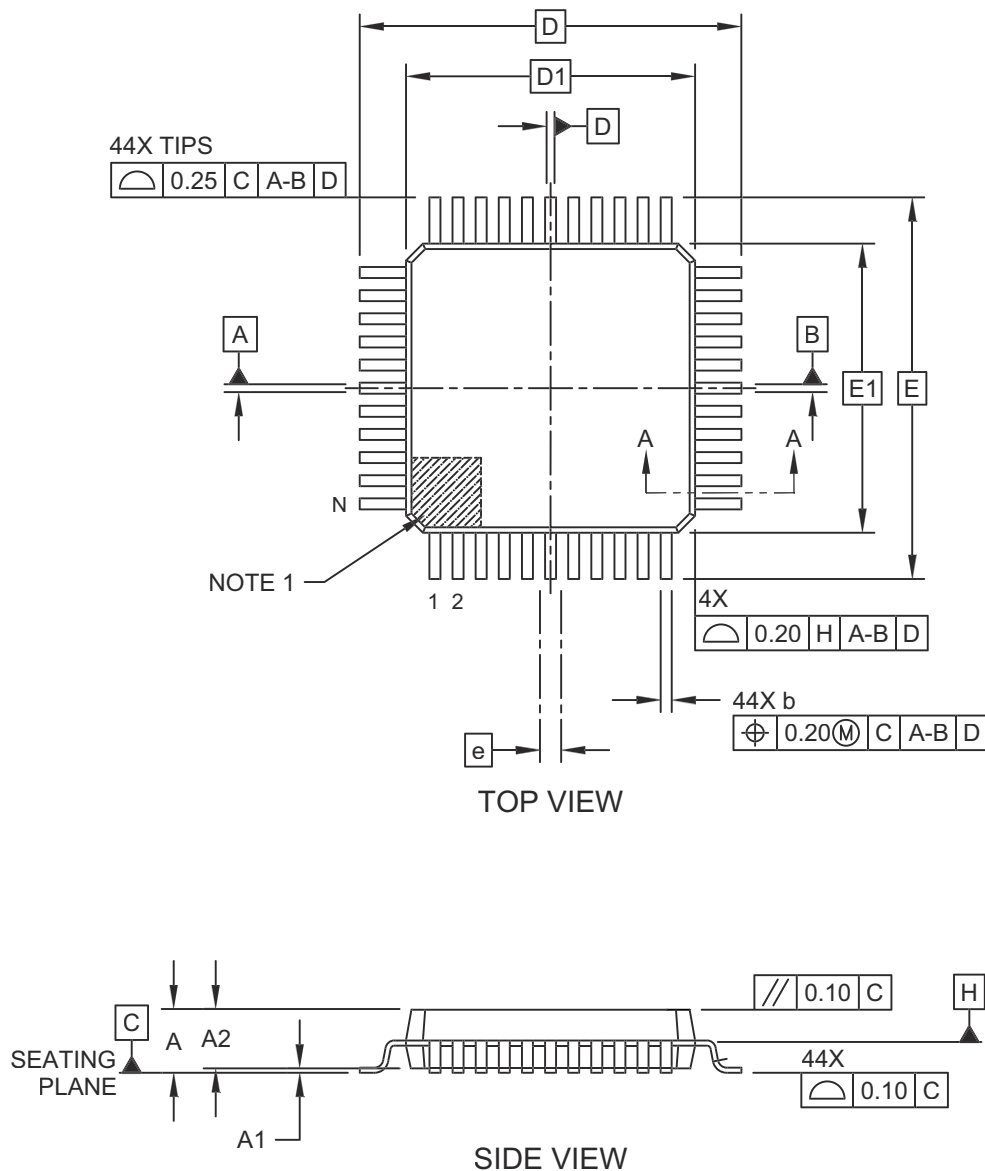
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

TC7126/A

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body [MQFP] 3.20 mm Footprint

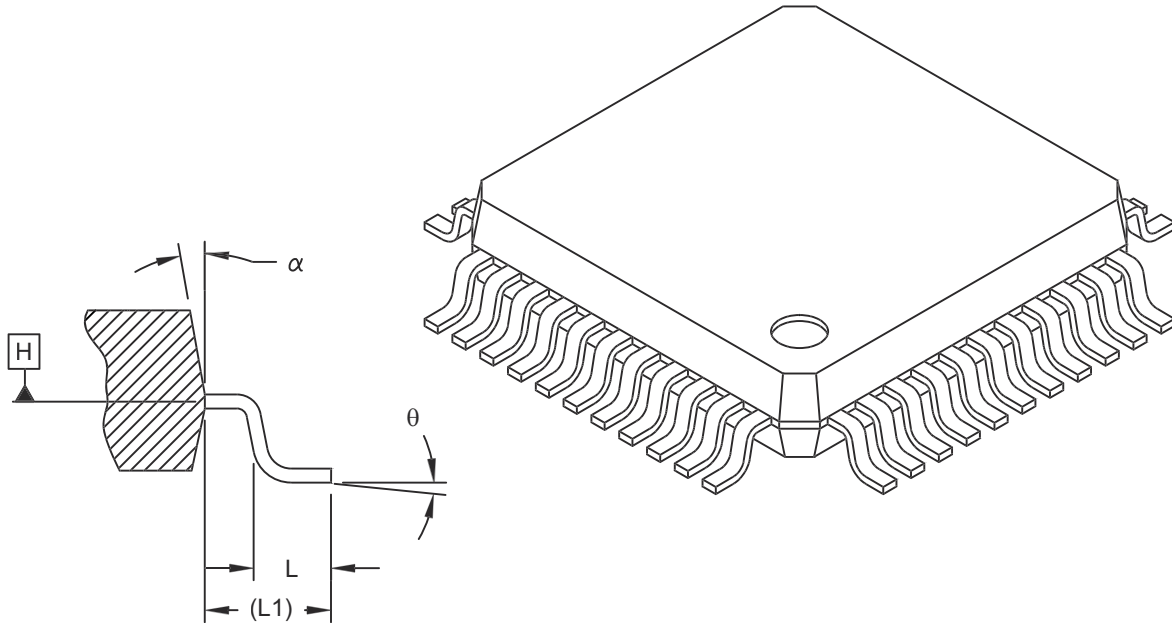
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-00071 Rev C Sheet 1 of 2

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body [MQFP] 3.20 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	-	-	2.45
Standoff	A1	0.00	-	0.25
Molded Package Thickness	A2	1.80	2.00	2.20
Foot Length	L	0.73	0.88	1.03
Footprint	L1	1.60 REF		
Foot Angle	θ	0°	-	7°
Overall Width	E	13.20 BSC		
Overall Length	D	13.20 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Width	b	0.29	-	0.45
Mold Draft Angle Top	α	5°	-	16°

Notes:

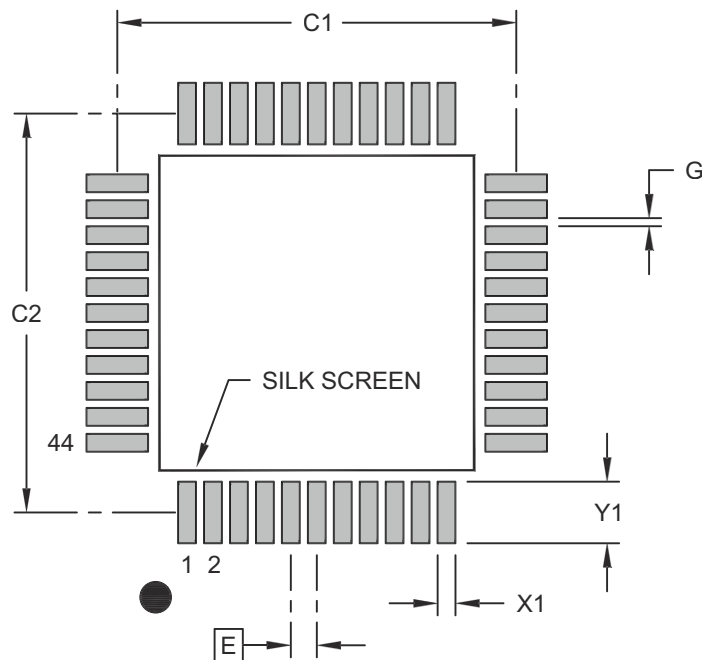
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00071 Rev C Sheet 2 of 2

TC7126/A

44-Lead Plastic Metric Quad Flatpack (KW) - 10x10x2.0 mm Body [MQFP] 3.20 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		12.30	
Contact Pad Spacing	C2		12.30	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.90
Contact Pad to Contact Pad (X40)	G	0.20		

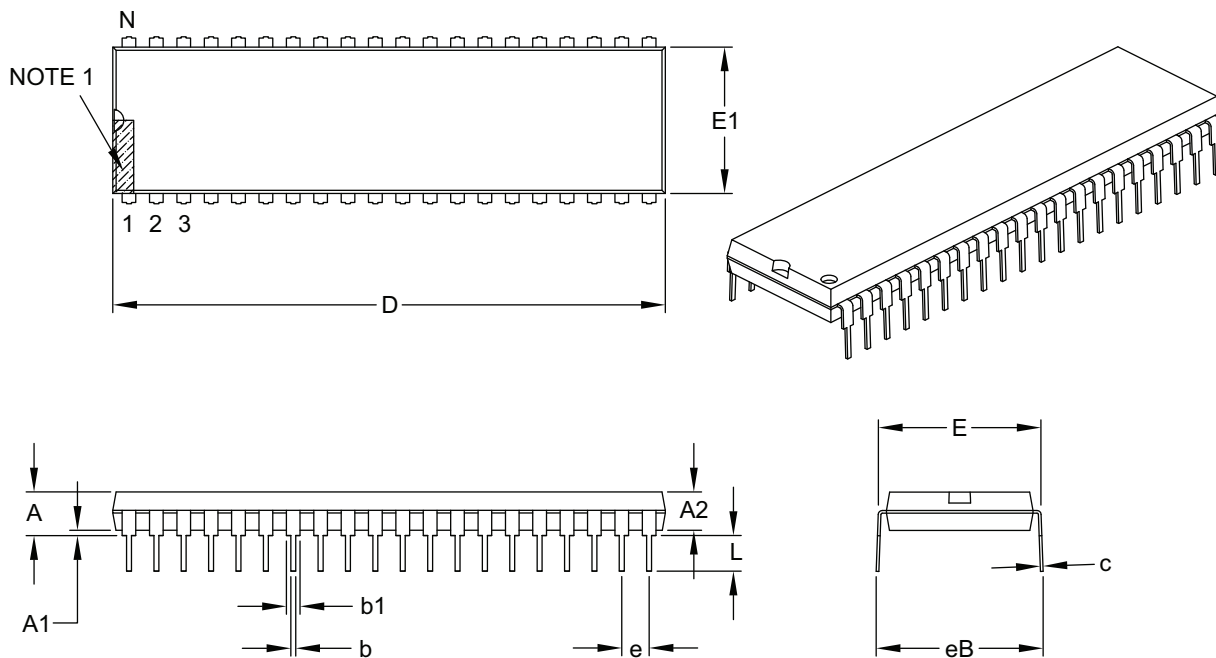
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02071 Rev C

40-Lead Plastic Dual In-Line (PL) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	40		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

APPENDIX A: REVISION HISTORY

Revision E (August 2025)

- Removed the 44-pin PLCC package option due to end-of-life status. The affected product part numbers are: TC7126CLW and TC7126SCLW.
- Removed Section 8.1, Liquid Crystal Display Sources, and Section 8.3, Flat Package, as they are not longer applicable.
- Minor editorial changes throughout.

Revision D (December 2012)

- Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	Examples:
Device	Temperature Range	Package	
Device: TC7126 CMOS ADC (PDIP, MQFP) TC7126A CMOS ADC (PDIP, MQFP) Temperature Range: C = 0°C to +70°C I = -25°C to +85°C (TC7126 only) Package: PL = 40-Lead Plastic Dual In-Line - 600 mil Body (PDIP) KW = 44-Lead Plastic Metric Quad Flatpack (MQFP)			a) TC7126CPL: Commercial Temperature PDIP Package b) TC7126CKW: Commercial Temperature MQFP Package c) TC7126IPL: Industrial Temperature PDIP Package d) TC7126ACPL: Commercial Temperature PDIP Package e) TC7126ACKW: Commercial Temperature MQFP Package

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

ISBN: 979-8-3371-1659-4

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.