SNx4AHC14 Hex Schmitt-Trigger Inverters

1 Features

- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)
- Operating range: 2V to 5.5V
- ±8mA output drive at 5V
- Schmitt-Trigger inputs enable input noise resistance
- Low power consumption: 20µA maximum I_{CC}
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- UPS
- White goods
- Computer peripherals
- Printers
- AC servo drives
- Desktop computers

3 Description

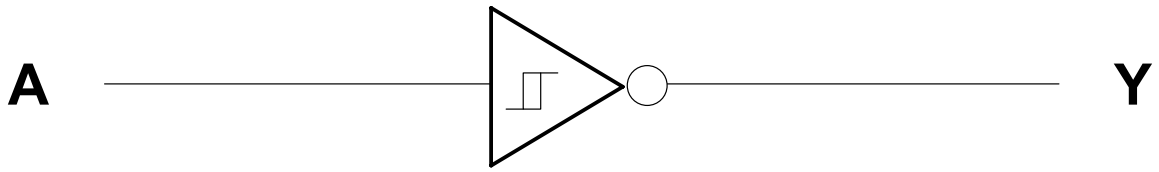
The SNx4AHC14 devices contain six independent inverters. These devices perform the boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but, because of the Schmitt-Trigger action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

Device Information

PART NUMBER	RATING	PACKAGE(1)
SN54AHC14	Military	J (CDIP, 14)
		W (CFP, 14)
		FK (LCCC, 20)
		BQA (WQFN, 14)
SN74AHC14	Commercial	D (SOIC, 14)
		DB (SSOP, 14)
		N (PDIP, 14)
		NS (SO, 14)
		PW (TSSOP, 14)
		DGV (TVSOP, 14)
		RGY (VQFN, 14)
		BQA (WQFN, 14)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

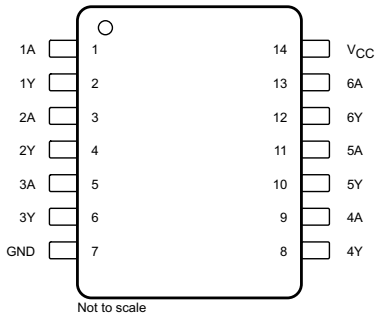

Figure 4-1. D, DB, DGV, J, N, NS, PW, or W Package, 14-Pin SOIC, SSOP, TVSOP, CDIP, PDIP, SO, TSSOP, or CFP (Top View)

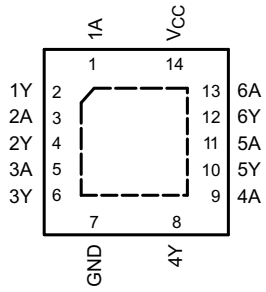

Figure 4-2. RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)

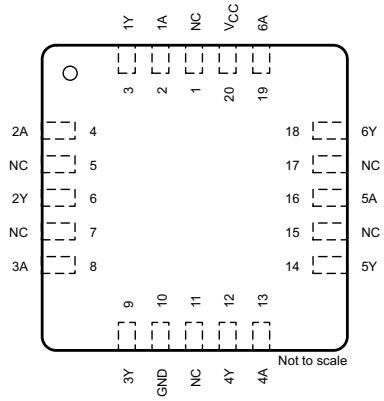

Figure 4-3. FK Package, 20-Pin LCCC (Top View)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, CDIP, PDIP, SO, TSSOP, CFP, VQFN	LCCC		
1A	1	2	I	Channel 1 Input
1Y	2	3	O	Channel 1 Output
2A	3	4	I	Channel 2 Input
2Y	4	6	O	Channel 2 Output
3A	5	8	I	Channel 3 Input
3Y	6	9	O	Channel 3 Output
4A	9	13	I	Channel 4 Input
4Y	8	12	O	Channel 4 Output
5A	11	16	I	Channel 5 Input
5Y	10	14	O	Channel 5 Output
6A	13	19	I	Channel 6 Input
6Y	12	18	O	Channel 6 Output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I (2)	Input voltage		–0.5	7	V
V_O (2)	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Virtual operating junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature	SN54AHC14	–55	125	°C
		SN74AHC14	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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5.4 Thermal Information

THERMAL METRIC[1]		SN74AHC14								UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	137.8	141.9	61.9	94.7	147.7	87.1	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	90	61.1	49.5	52.5	77.4	92.6	90.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81	98.3	71.3	41.7	53.4	90.9	62.5	56.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37	42.7	9.7	34.7	21.3	27.2	22.8	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.6	97	70.6	41.7	53.1	90.2	61.7	56.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	45.1	33.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{T+}	Positive-going input threshold voltage		V_{CC} = 3 V	1.2		2.2	V
			V_{CC} = 4.5 V	1.75		3.15	
			V_{CC} = 5.5 V	2.15		3.85	
V_{T-}	Negative-going input threshold voltage		V_{CC} = 3 V	0.9		1.9	V
			V_{CC} = 4.5 V	1.35		2.75	
			V_{CC} = 5.5 V	1.65		3.35	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 3 V	0.3		1.2	V
			V_{CC} = 4.5 V	0.4		1.4	
			V_{CC} = 5.5 V	0.5		1.6	
V_{OH}		I_{OH} = –50 µA	V_{CC} = 2 V	1.9	2		V
			V_{CC} = 3 V	2.9	3		
			V_{CC} = 4.5 V	4.4	4.5		
		I_{OH} = –4 mA, V_{CC} = 3 V	T_A = 25°C	2.58			
			SNx4AHC14	2.48			
		I_{OL} = –8 mA, V_{CC} = 4.5 V	T_A = 25°C	3.94			
			SNx4AHC14	3.8			

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}		I_{OH} = 50 µA	V_{CC} = 2 V				0.1	V
			V_{CC} = 3 V				0.1	
			V_{CC} = 4.5 V				0.1	
		I_{OH} = 4 mA, V_{CC} = 3 V	T_A = 25°C				0.36	
			SN54AHC14				0.5	
			SN74AHC14	T_A = –40°C to 85°C			0.44	
				T_A = –40°C to 125°C			0.5	
		I_{OL} = 8 mA, V_{CC} = 4.5 V	T_A = 25°C				0.36	
			SN54AHC14				0.5	
			SN74AHC14	T_A = –40°C to 85°C			0.44	
				T_A = –40°C to 125°C			0.5	
I_I		V_I = 5.5 V or GND, V_{CC} = 0 V to 5.5 V	T_A = 25°C				±0.1	µA
			SNx4AHC14				±1[1]	
I_{CC}		V_I = V_{CC} or GND, I_O = 0, V_{CC} = 5.5 V	T_A = 25°C				1	µA
			SNx4AHC14				20	
C_I		V_I = V_{CC} or GND, V_{CC} = 5 V	T_A = 25°C			2	10	pF
			SN74AHC14				10	
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz, V_{CC} = 5 V				9		pF
NOISE[2]								
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C				0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C				–0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C				4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C					1.5	V

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) Characteristics are for surface-mount packages only.

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5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

V_{CC} = 3.3 V ± 0.3 V and over operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to Y (output), C_L = 15 pF	T_A = 25°C	8.3[1]		12.8[1]	ns
		SN54AHC14	1[1]		15[1]	
		SN74AHC14	1		16	
t_{PHL}	From A (input) to Y (output), C_L = 15 pF	T_A = 25°C	8.3[1]		12.8[1]	ns
		SN54AHC14	1[1]		15[1]	
		SN74AHC14	1		16	
t_{PLH}	From A (input) to Y (output), C_L = 50 pF	T_A = 25°C	10.8		16.3	ns
		SN54AHC14	1		18.5	
		SN74AHC14	1		19.5	
t_{PHL}	From A (input) to Y (output), C_L = 50 pF	T_A = 25°C	10.8		16.3	ns
		SN54AHC14	1		18.5	
		SN74AHC14	1		19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

V_{CC} = 5 V ± 0.5 V and over operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to Y (output), C_L = 15 pF	T_A = 25°C	5.5[1]		8.6[1]	ns
		SN54AHC14	1[1]		10[1]	
		SN74AHC14	1		10	
t_{PHL}	From A (input) to Y (output), C_L = 15 pF	T_A = 25°C	5.5[1]		8.6[1]	ns
		SN54AHC14	1[1]		10[1]	
		SN74AHC14	1		10	
t_{PLH}	From A (input) to Y (output), C_L = 50 pF	T_A = 25°C	7		10.6	ns
		SNx4AHC14	1		12	
t_{PHL}	From A (input) to Y (output), C_L = 50 pF	T_A = 25°C	7		10.6	ns
		SNx4AHC14	1		12	

5.8 Typical Characteristics

C_L = 50 pF (unless otherwise noted)

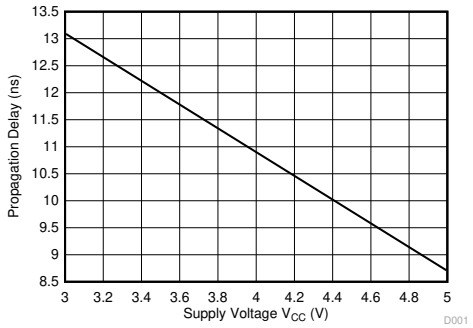

Figure 5-1. Propagation Delay vs Supply Voltage

6 Parameter Measurement Information

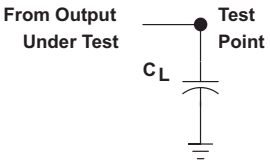

Figure 6-1. Load Circuit For Totem-Pole Outputs

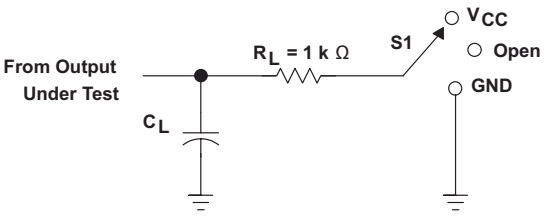

Figure 6-2. Load Circuit For 3-State and Open-Drain Outputs

Table 6-1. Measurement Information

TEST	S1
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	V_{CC}
t_{PHZ}, t_{PZH}	GND
Open drain	V_{CC}

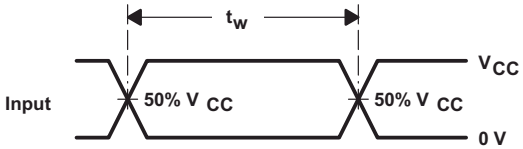

Figure 6-3. Voltage Waveforms Pulse Duration

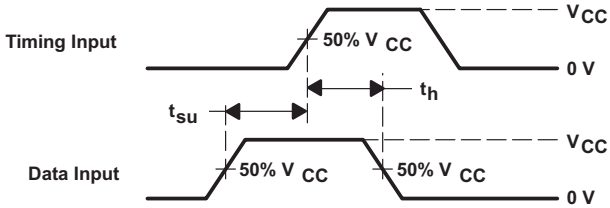

Figure 6-4. Voltage Waveforms Setup and Hold Times

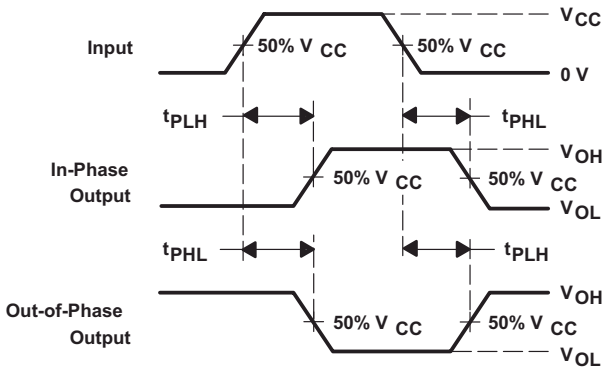

Figure 6-5. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

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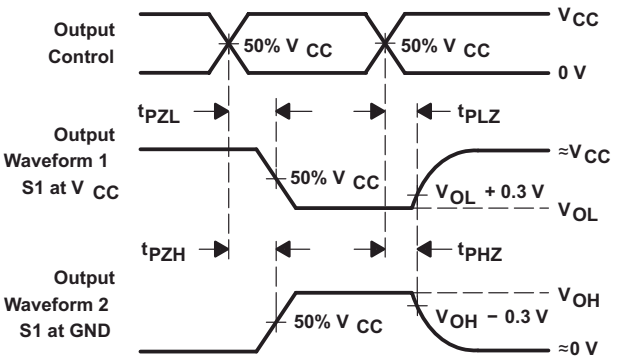

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-6. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

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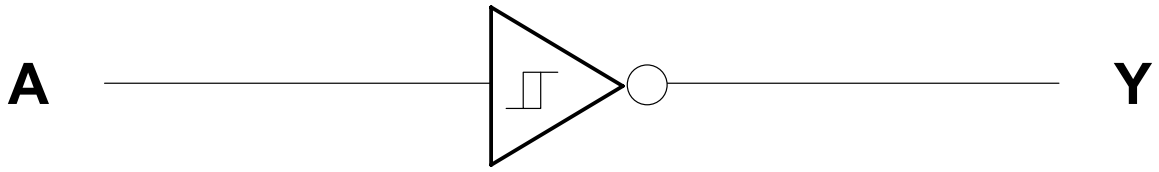
7 Detailed Description

7.1 Overview

The SNx4AHC14 Schmitt-Trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

7.2 Functional Block Diagram



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7.3 Feature Description

The wide operating range of the device allows it to be used in a variety of systems that use different logic levels. The outpus can drive up to 10 LSTTL loads each. The balanced drive outputs can source or sink 8 mA at 5-V V_{CC}.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4AHC14.

Table 7-1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC14 device is a Schmitt-Trigger input CMOS device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a delay for a logic input.

8.2 Typical Application

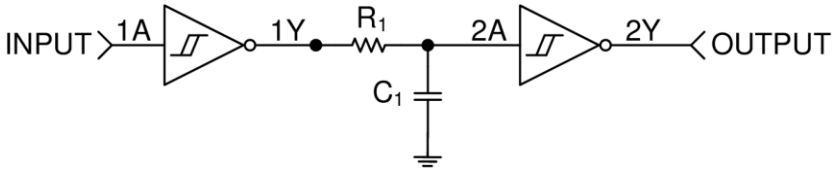

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Figure 8-1. Simplified Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant, τ, is calculated from: $\tau = RC$.

The delay time for this circuit is from $t_{delay(min)} = -\ln |1 - V_{T+(min)} / V_{CC}| \tau$ to $t_{delay(max)} = -\ln |1 - V_{T+(max)} / V_{CC}| \tau$. It must be noted that the delay is consistent for each device, but because the switching threshold is only ensured between the minimum and maximum value, the output pulse length varies between devices. These values must be calculated by using the minimum and maximum V_{T+} values in the *Electrical Characteristics*.

The resistor value must be chosen such that the maximum current to and from the SN74AHC14 is 8 mA at 5-V V_{CC}.

8.2.3 Application Curve

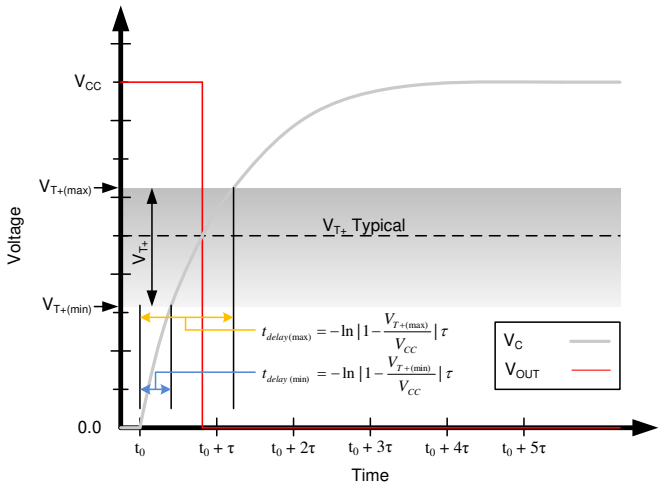

Figure 8-2. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1-µF capacitor on the V_{CC} terminal, and must be placed as close as possible to the pin for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

8.4.2 Layout Example

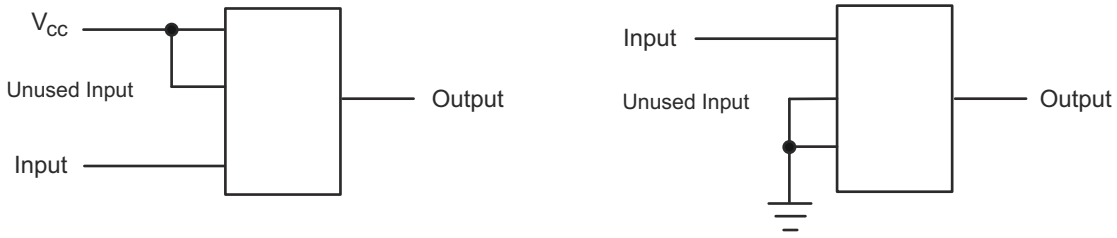

Figure 8-3. Layout Diagram

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (October 2023) to Revision P (February 2024)	Page
• Updated RθJA values: DB = 112.4 to 137.8, RGY = 63.8 to 87.1; Updated DB and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	5

Changes from Revision N (June 2023) to Revision O (October 2023)	Page
• Deleted machine model	4
• Updated RθJA values: D = 99.3 to 124.5, PW = 128.8 to 147.7; Updated D and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9680201Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201Q2A SNJ54AHC14FK
5962-9680201QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QCA SNJ54AHC14J
5962-9680201QDA	NRND	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QDA SNJ54AHC14W
5962-9682001QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001QCA SNJ54AHC08J
5962-9682001QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001QDA SNJ54AHC08W
SN74AHC14BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	AHC14
SN74AHC14DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14DGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14DGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DRG3	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DRG3.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC14N
SN74AHC14N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC14N

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC14NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14
SN74AHC14PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14PWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14PWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14RGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14RGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SN74AHC14RGYRG4.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14
SNJ54AHC08J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001QCA SNJ54AHC08J
SNJ54AHC08W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682001QDA SNJ54AHC08W
SNJ54AHC14FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201Q2A SNJ54AHC 14FK
SNJ54AHC14FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201Q2A SNJ54AHC 14FK
SNJ54AHC14J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QCA SNJ54AHC14J
SNJ54AHC14J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QCA SNJ54AHC14J
SNJ54AHC14W	NRND	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QDA SNJ54AHC14W

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHC14W.A	NRND	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680201QDA SNJ54AHC14W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC14, SN74AHC14 :

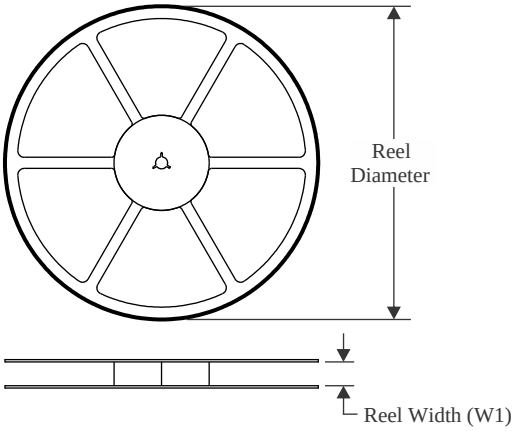
- Catalog : SN74AHC14
- Military : SN54AHC14

NOTE: Qualified Version Definitions:

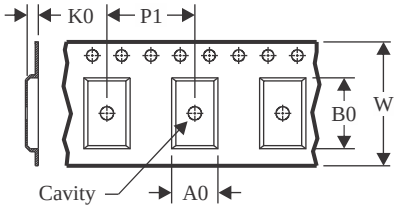
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

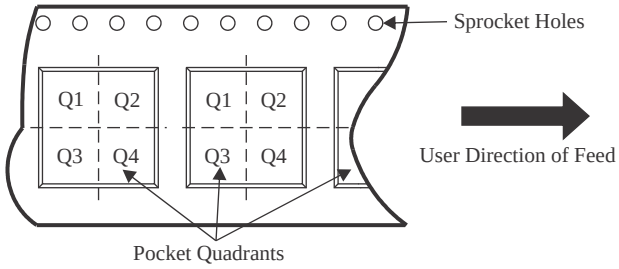


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

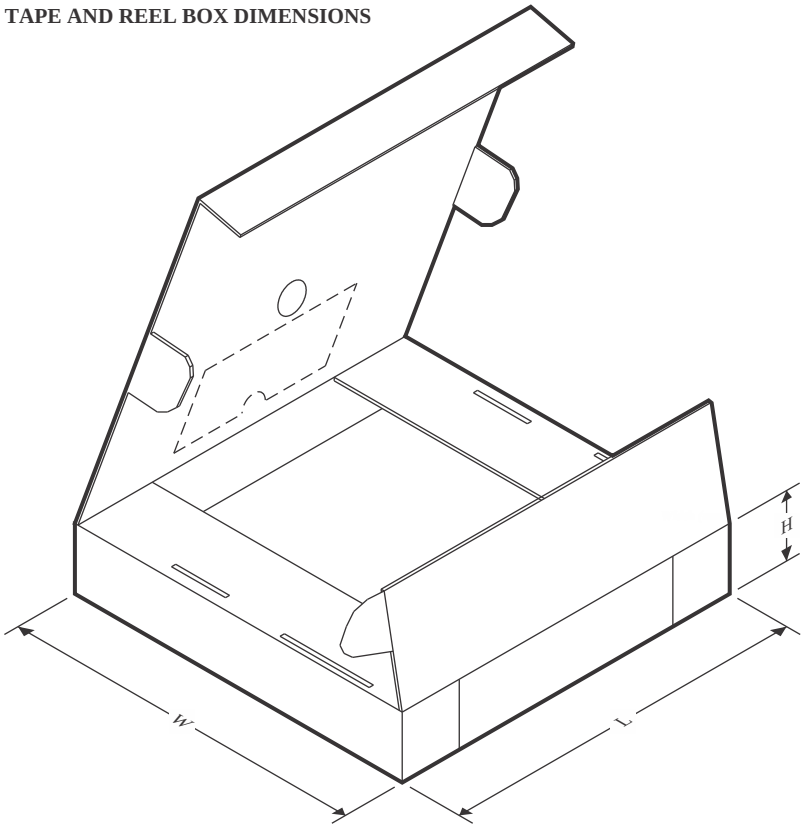
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC14BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC14DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC14DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74AHC14DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74AHC14PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74AHC14RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC14RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

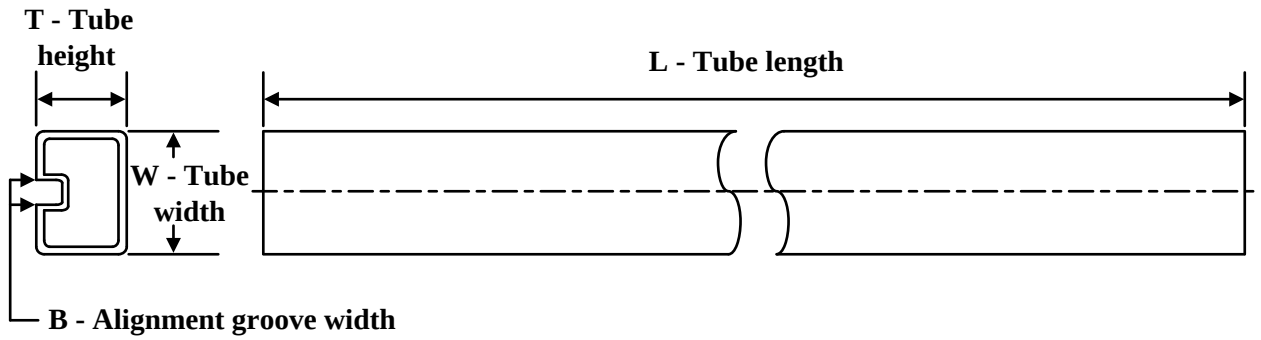
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

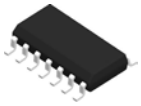
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC14BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC14DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC14DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC14DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC14DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74AHC14DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC14NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC14PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC14PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC14PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC14PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC14PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74AHC14PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC14PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC14RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74AHC14RGYRG4	VQFN	RGY	14	3000	360.0	360.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9680201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9680201QDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-9682001QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC14N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC14N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC08W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHC14FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC14FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC14W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHC14W.A	W	CFP	14	25	506.98	26.16	6220	NA

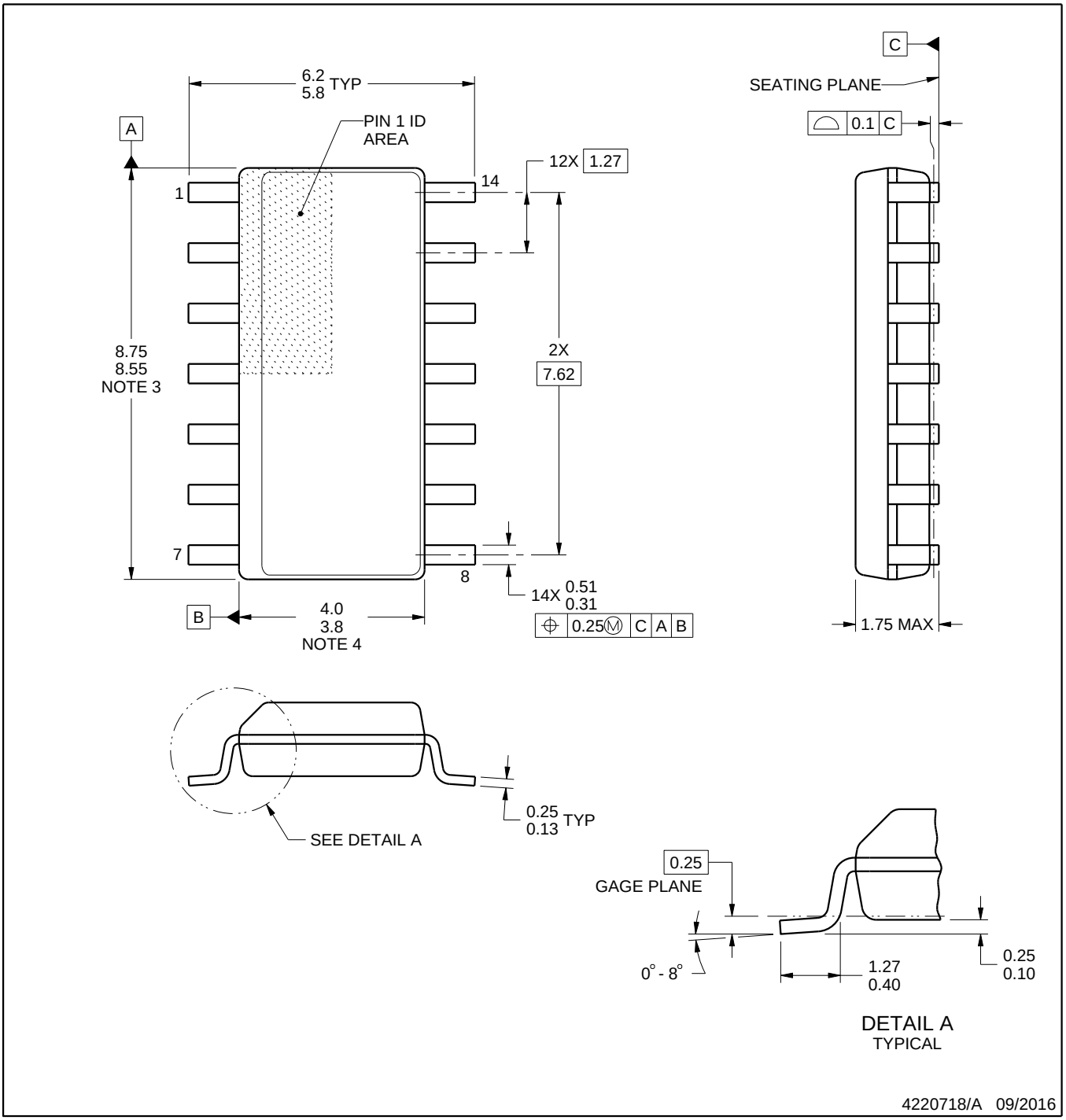


PACKAGE OUTLINE

D0014A

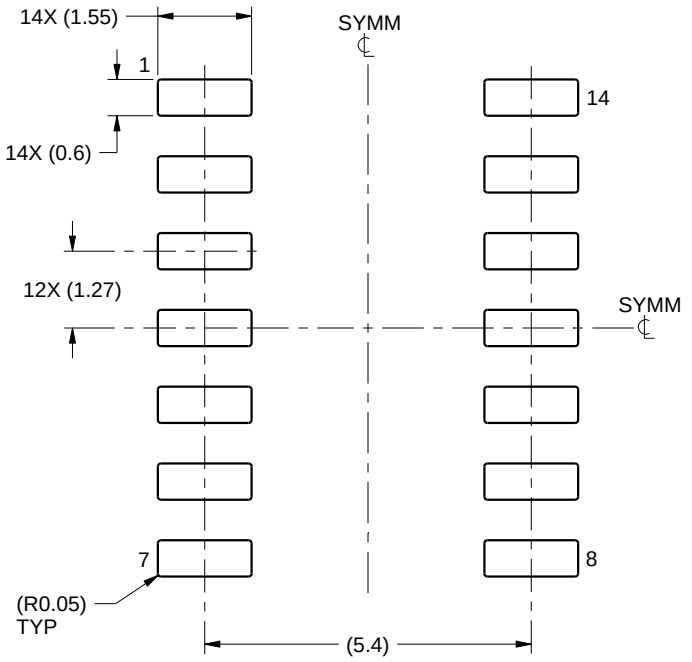
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

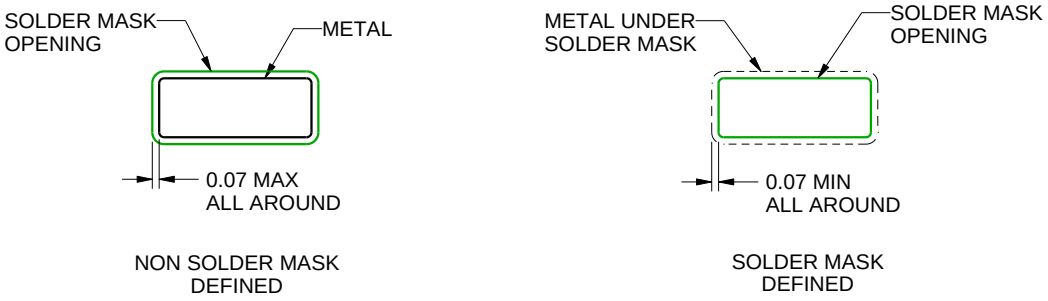


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

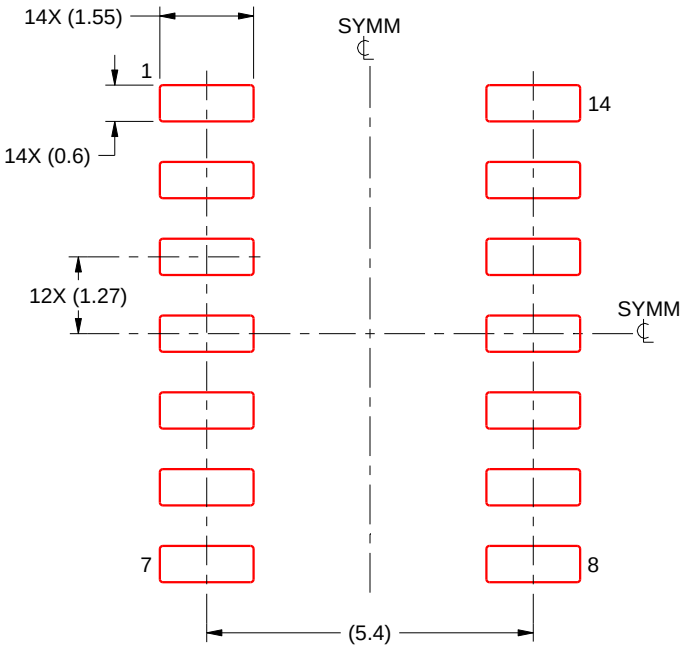
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

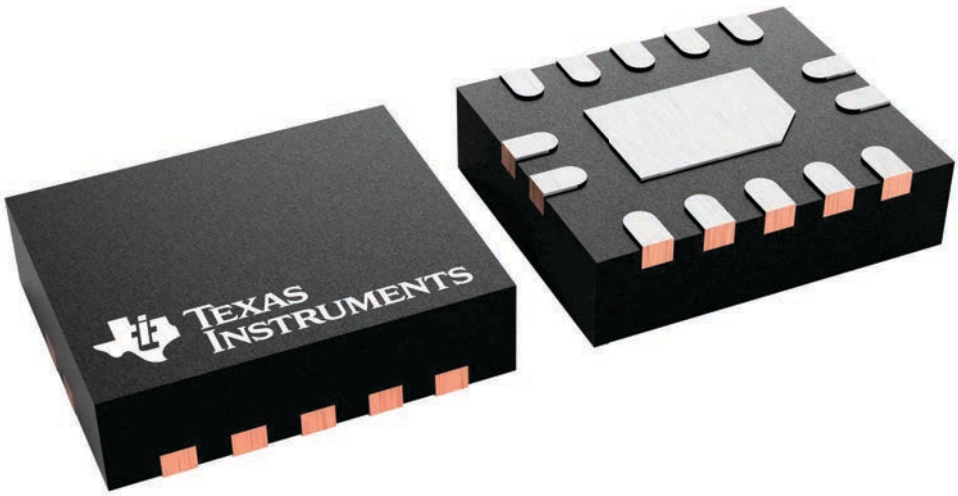
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



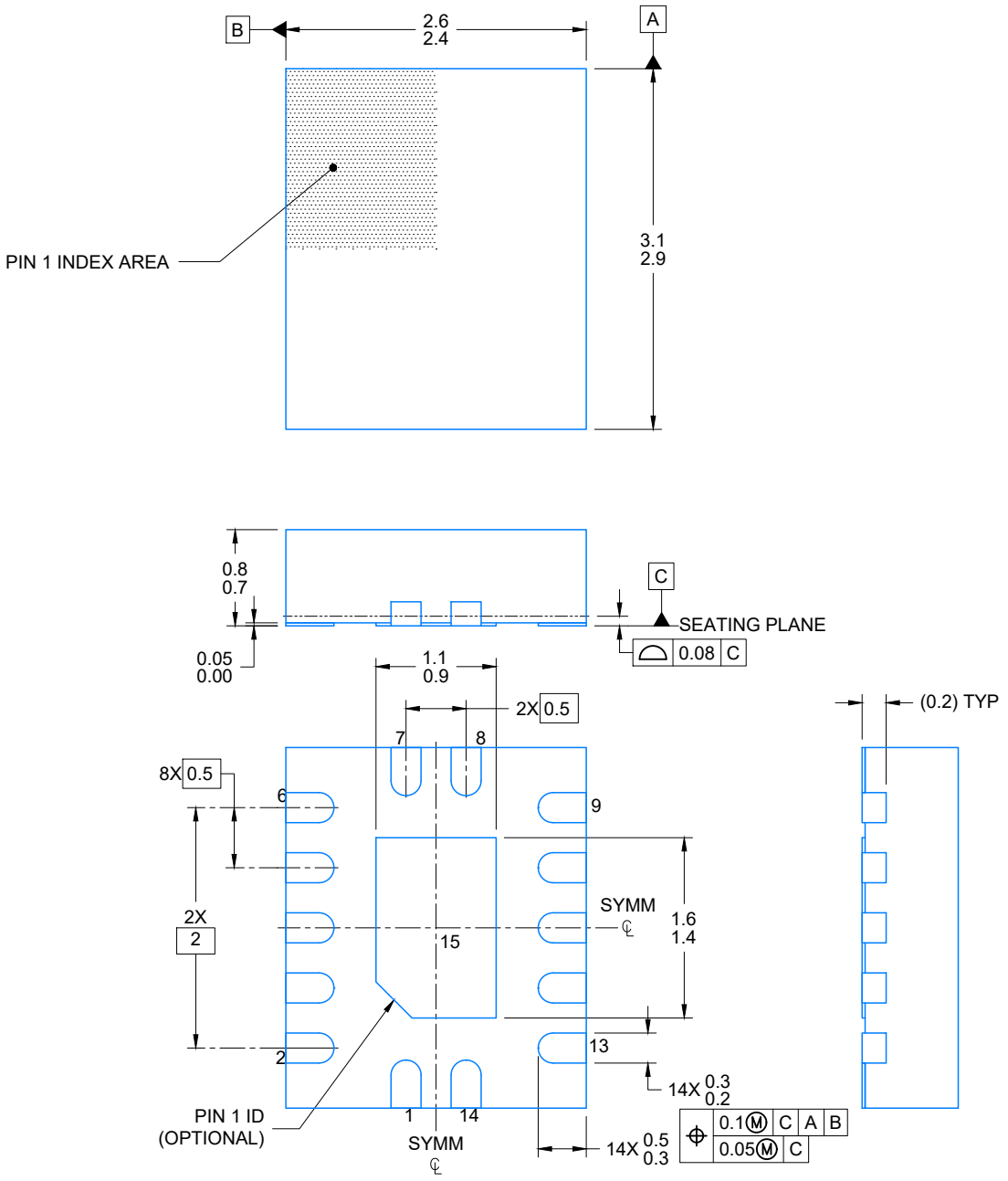
4227145/A

PACKAGE OUTLINE

BQA0014A

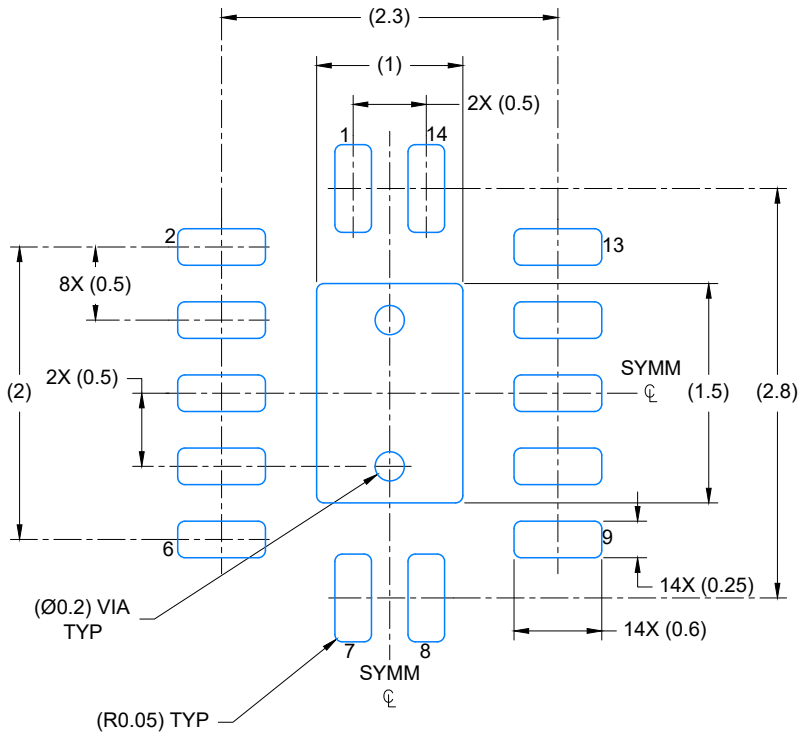
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

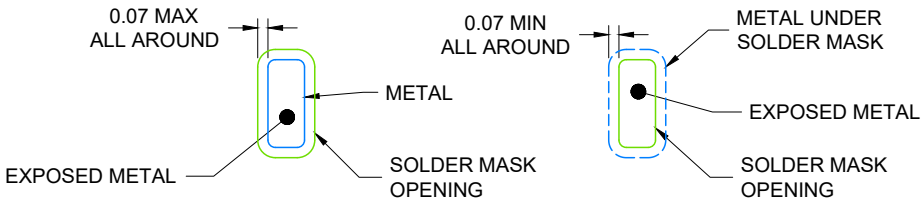


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



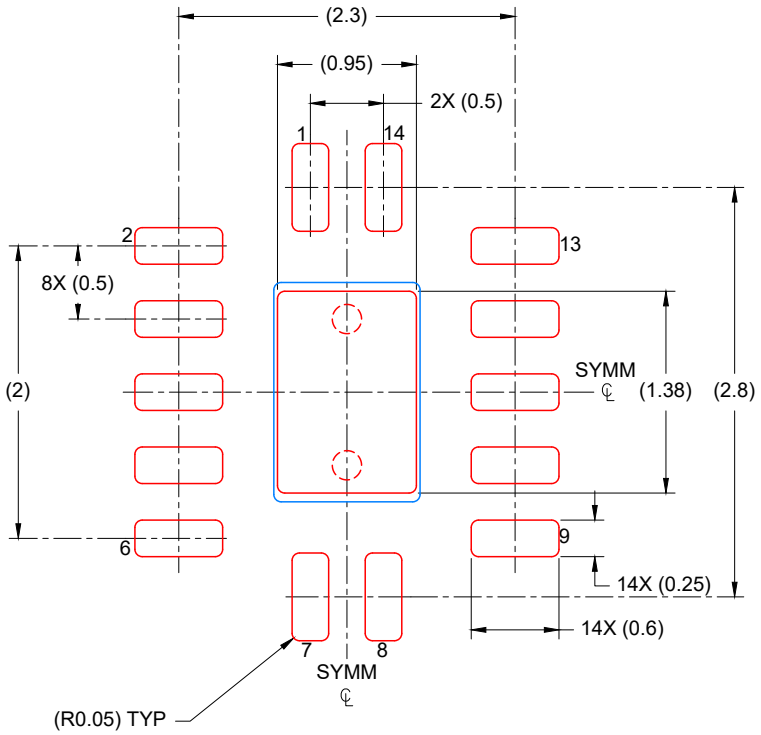
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

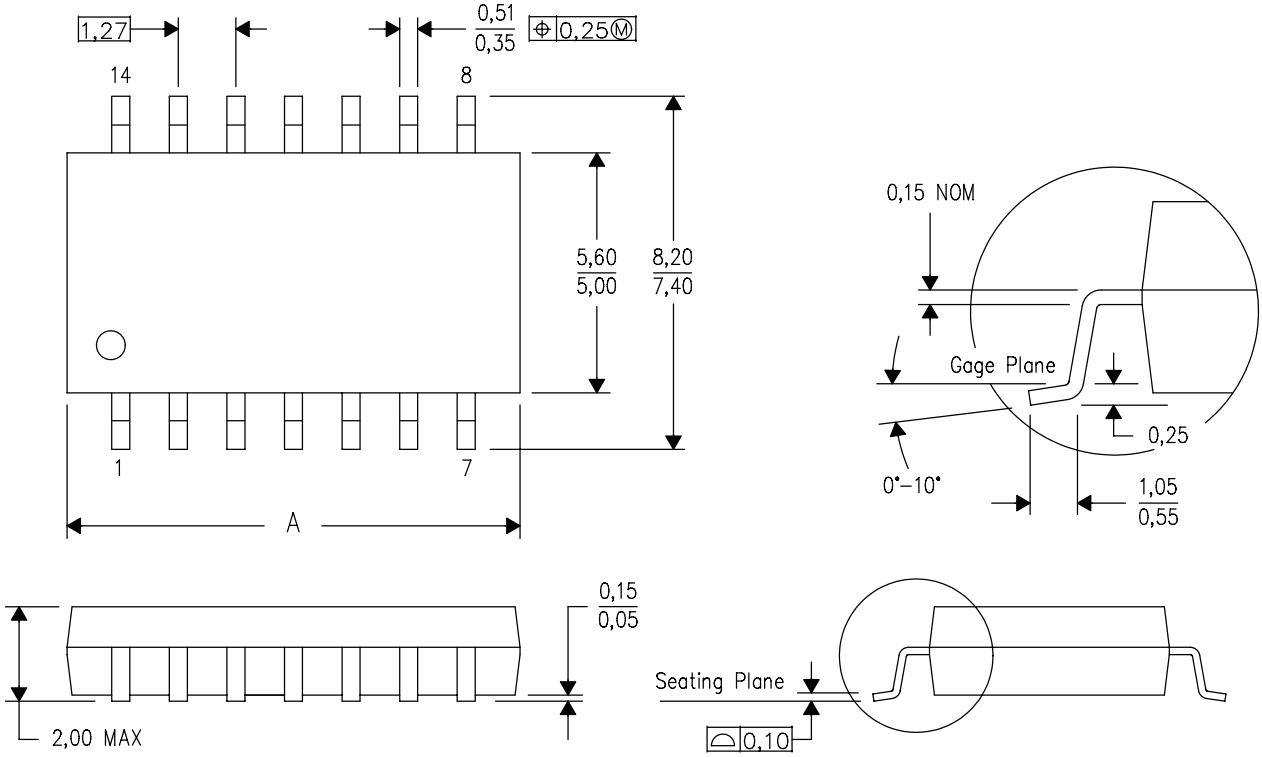
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

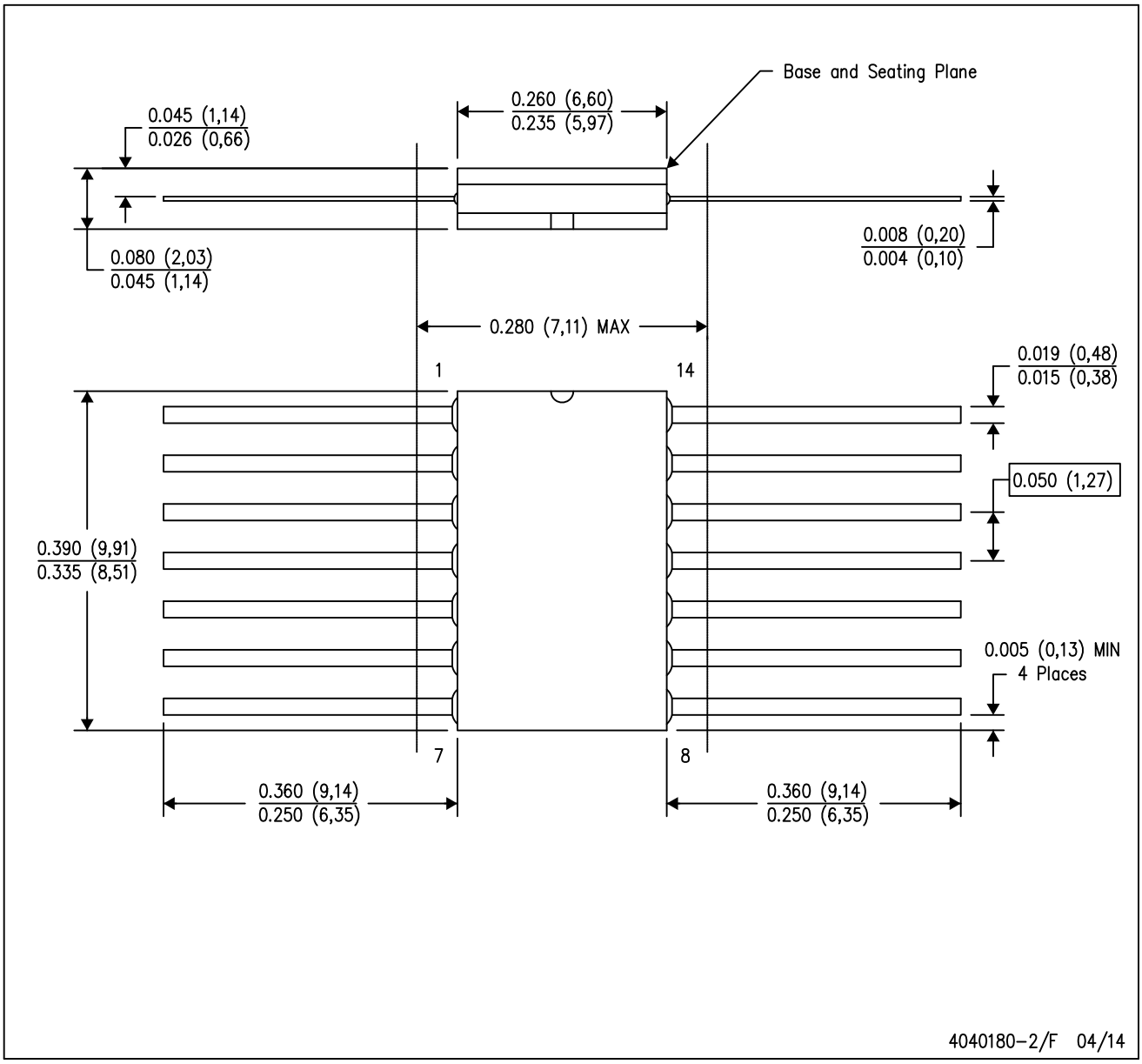


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

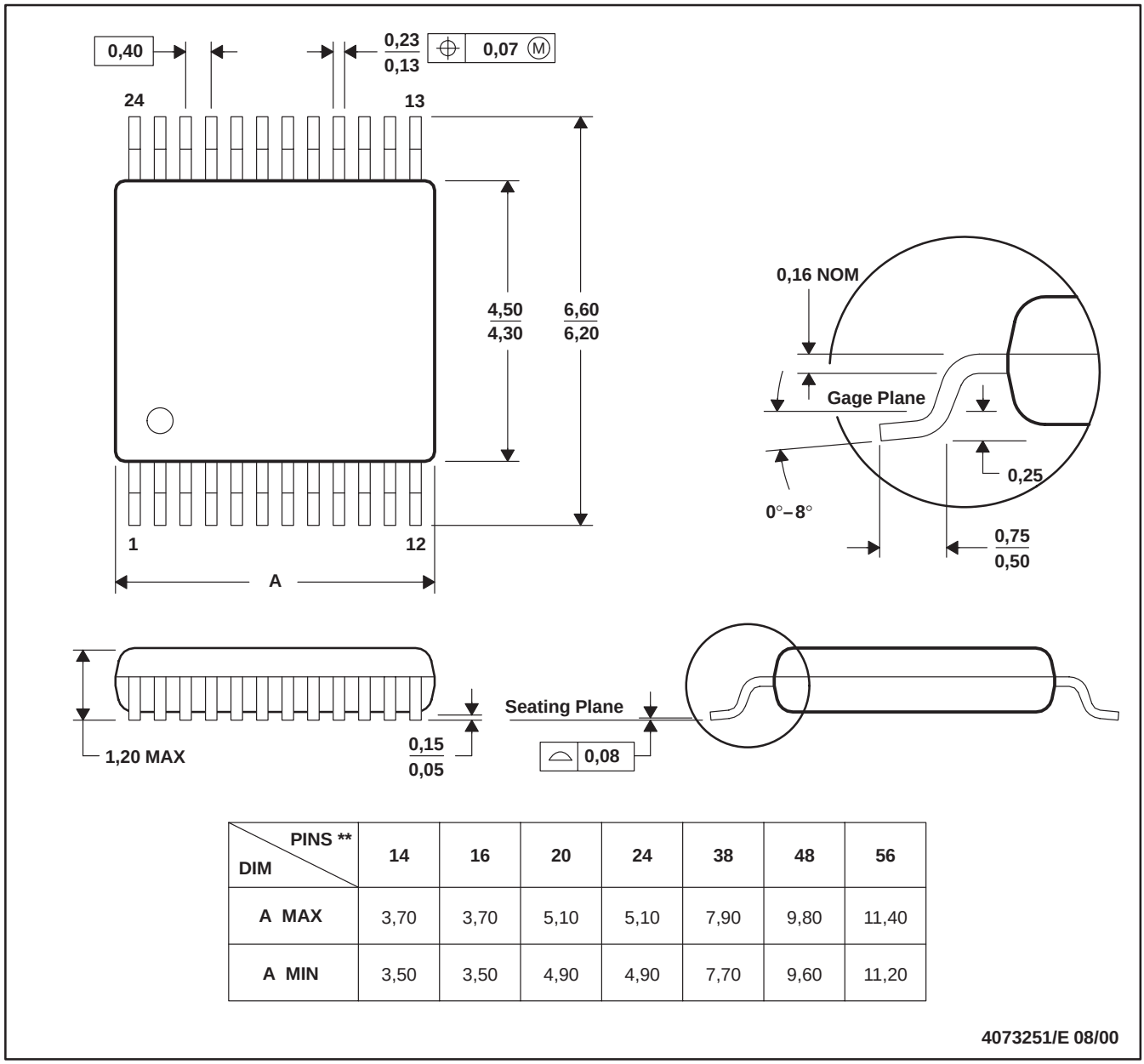
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

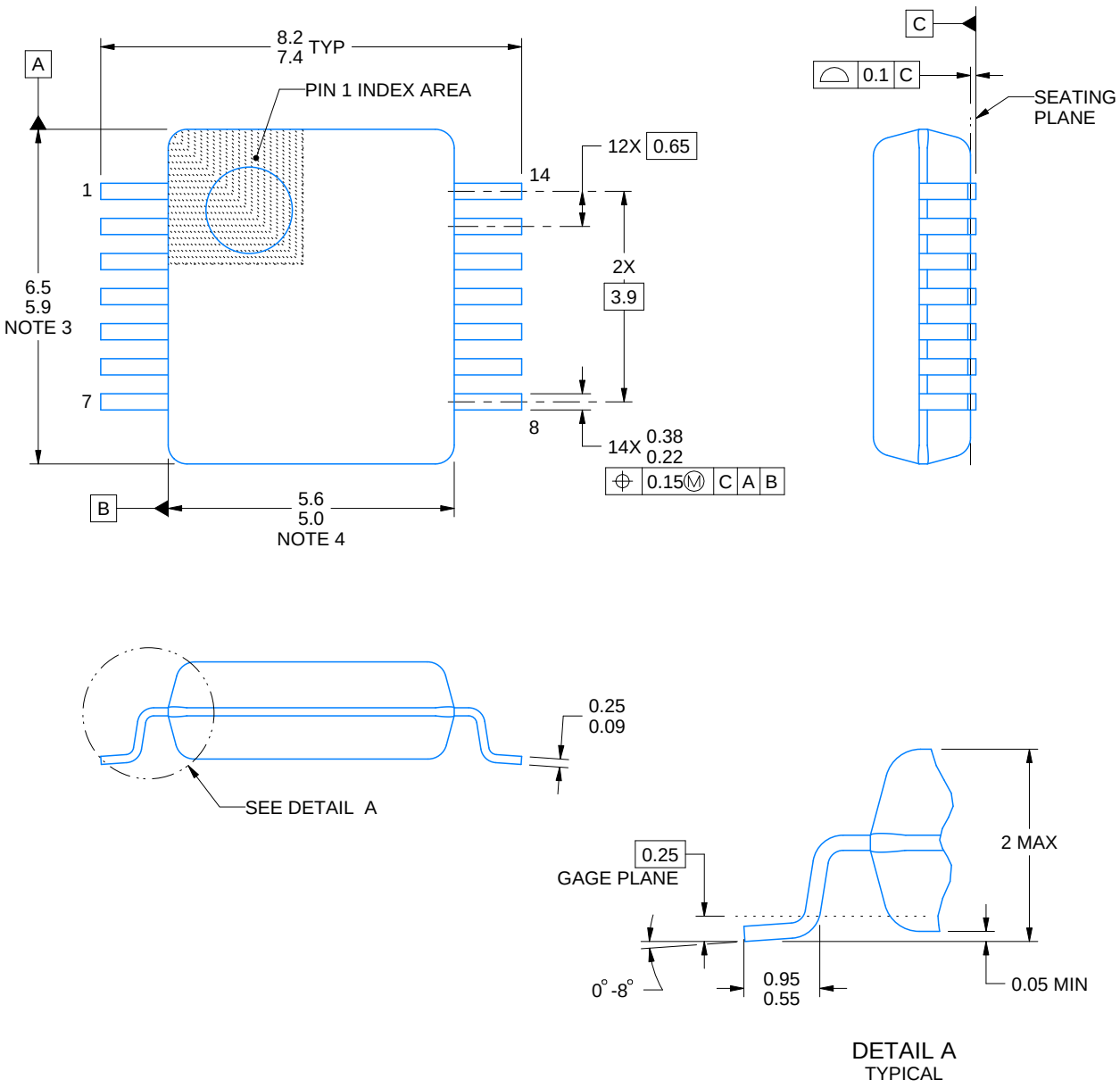
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

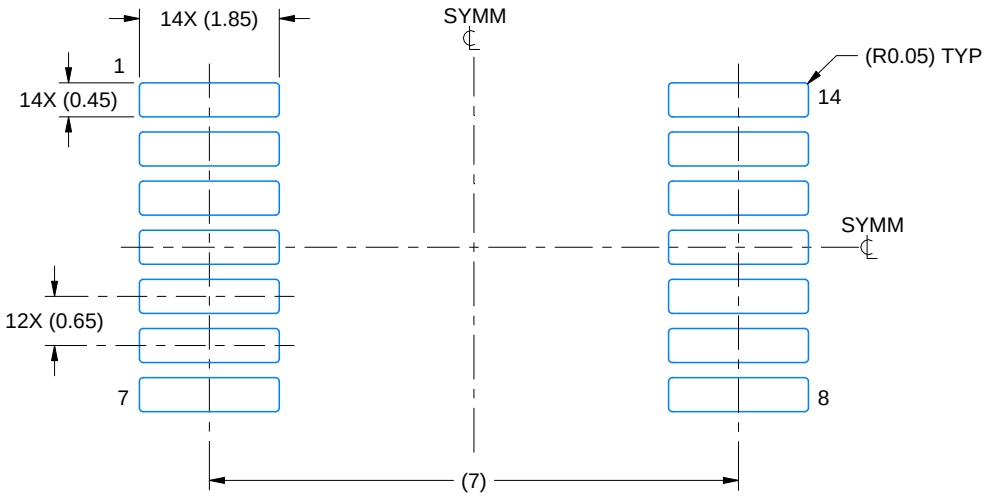
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

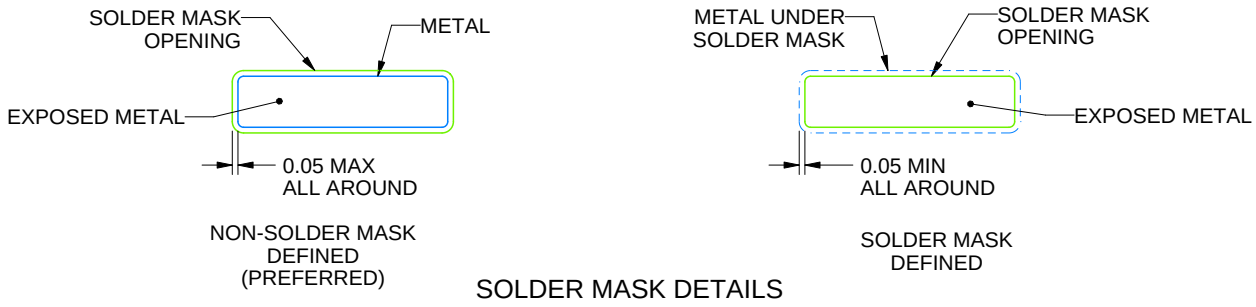


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

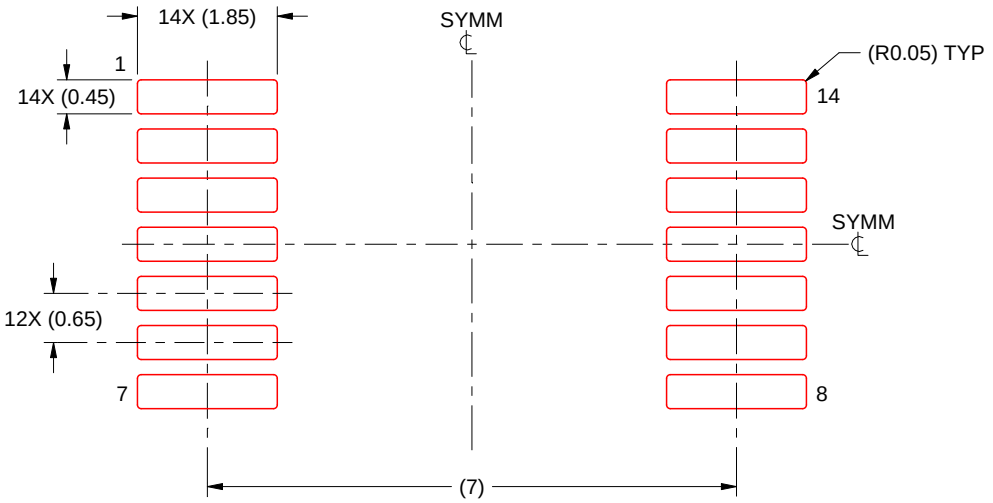


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

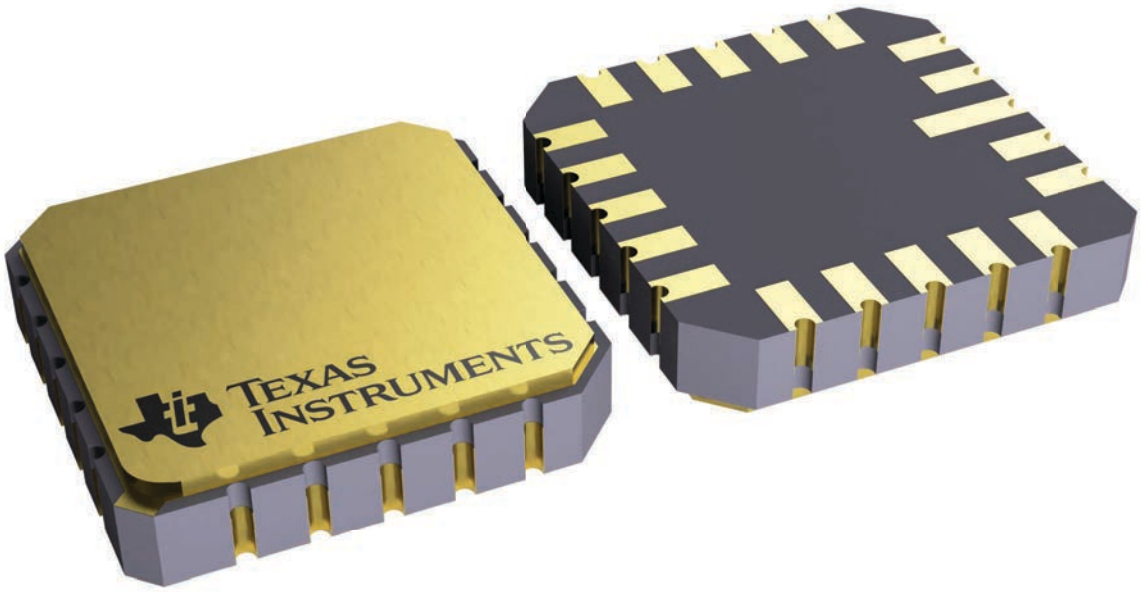
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

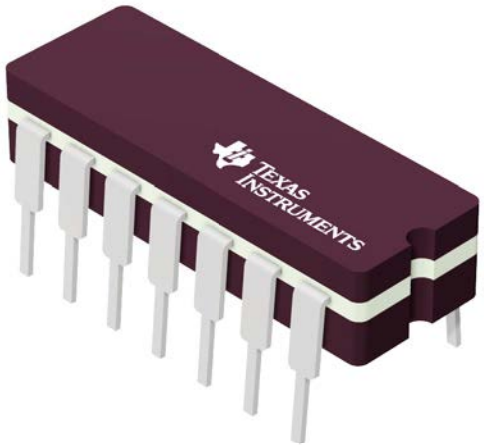


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

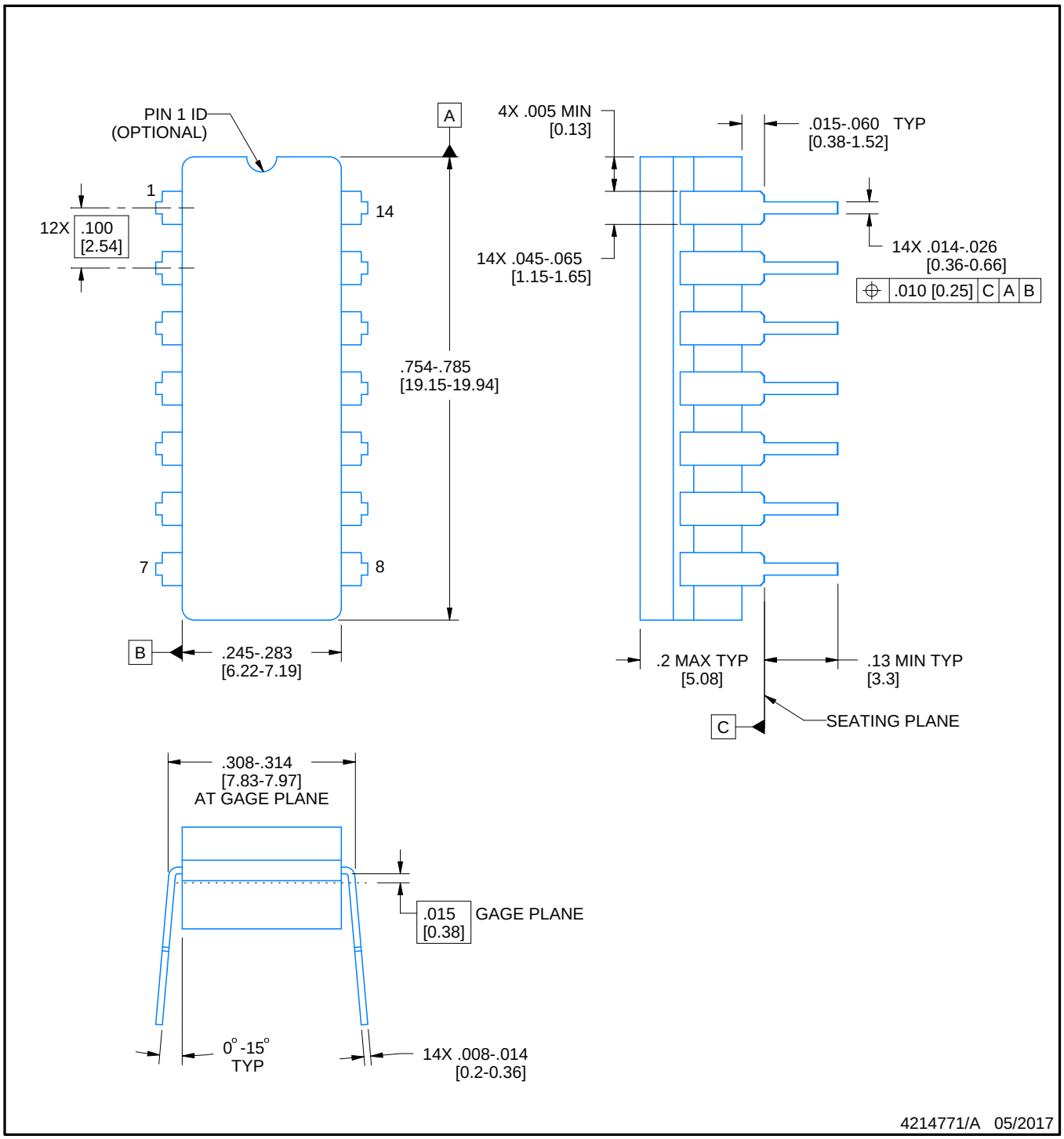
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

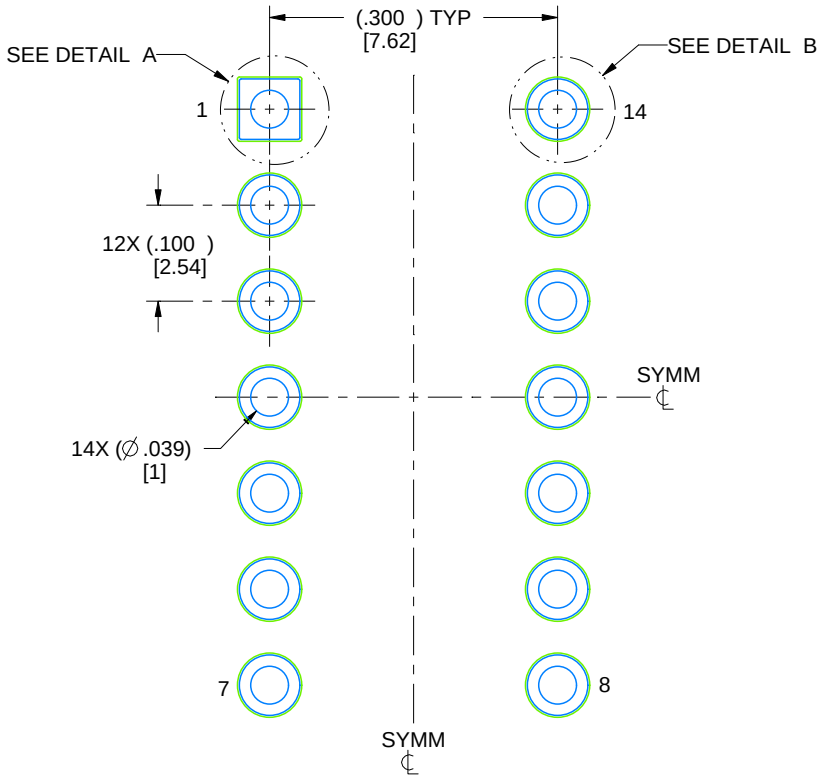
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

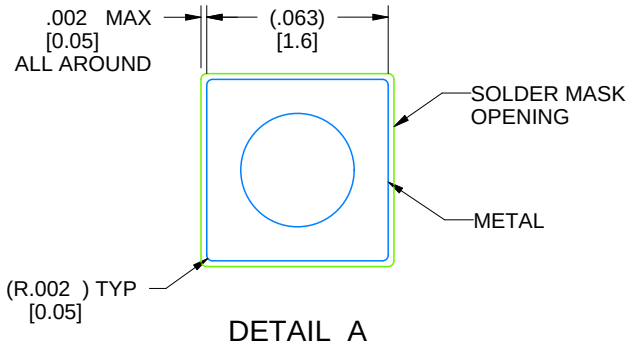
J0014A

CDIP - 5.08 mm max height

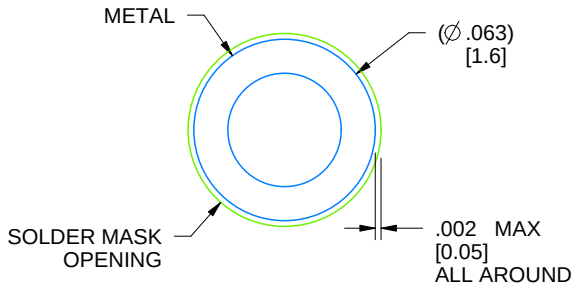
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



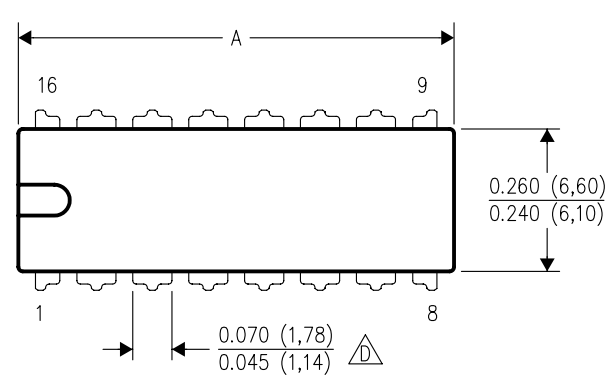
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

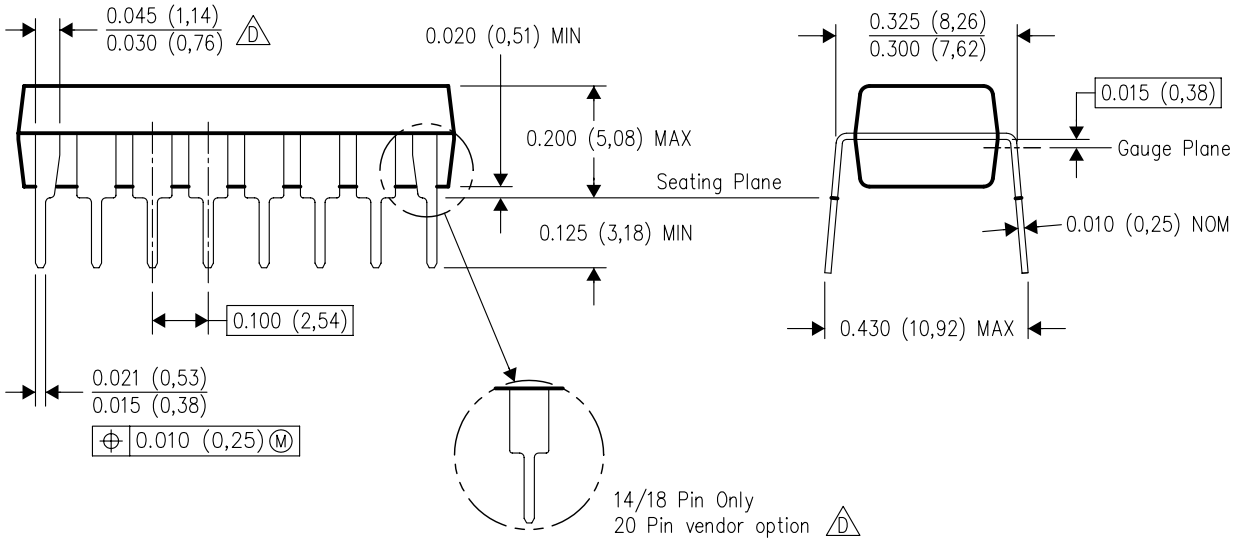
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

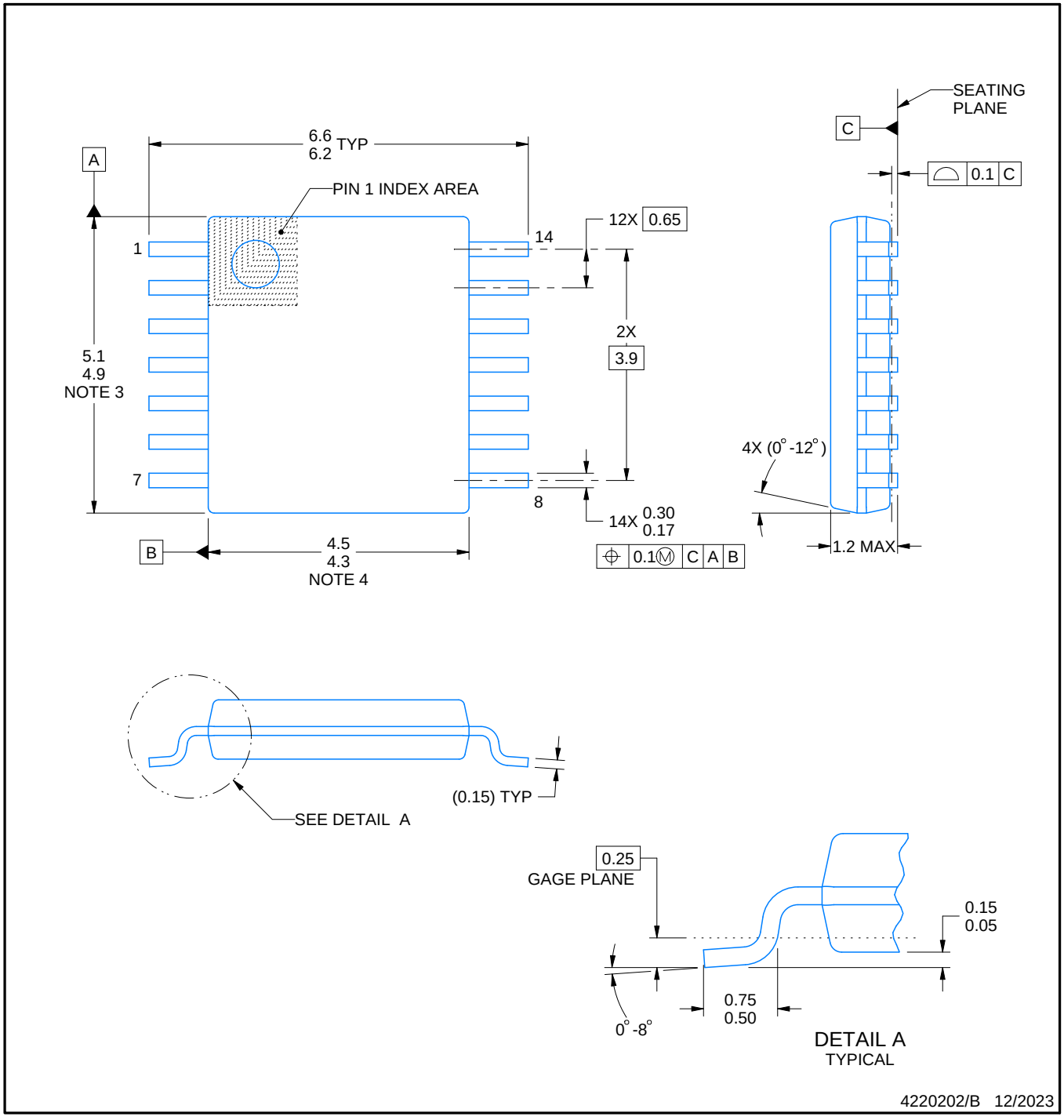
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

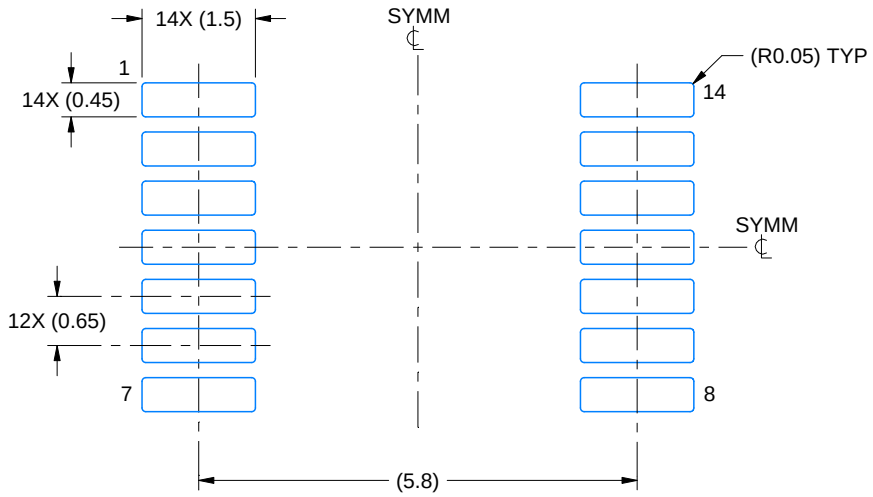
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

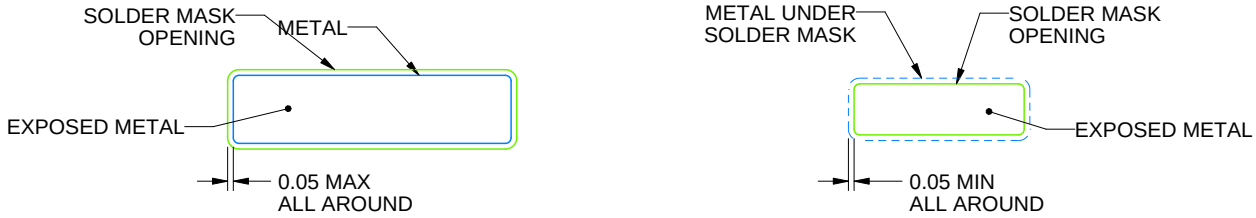


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

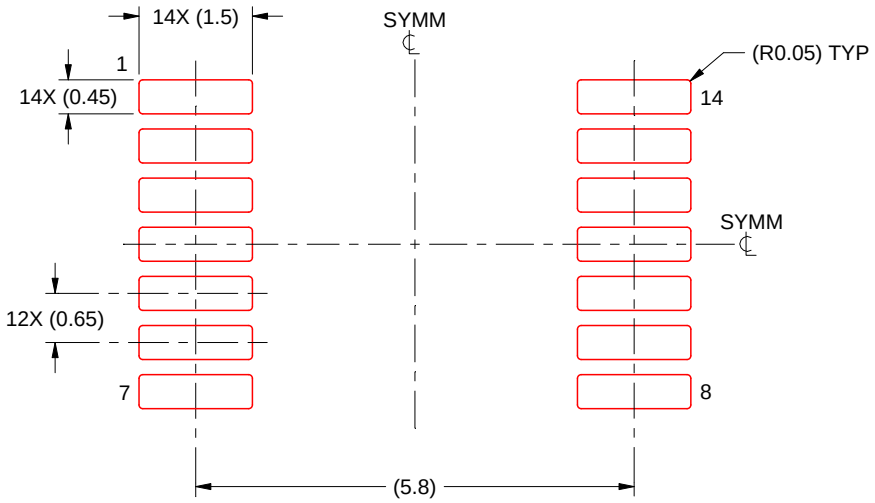


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

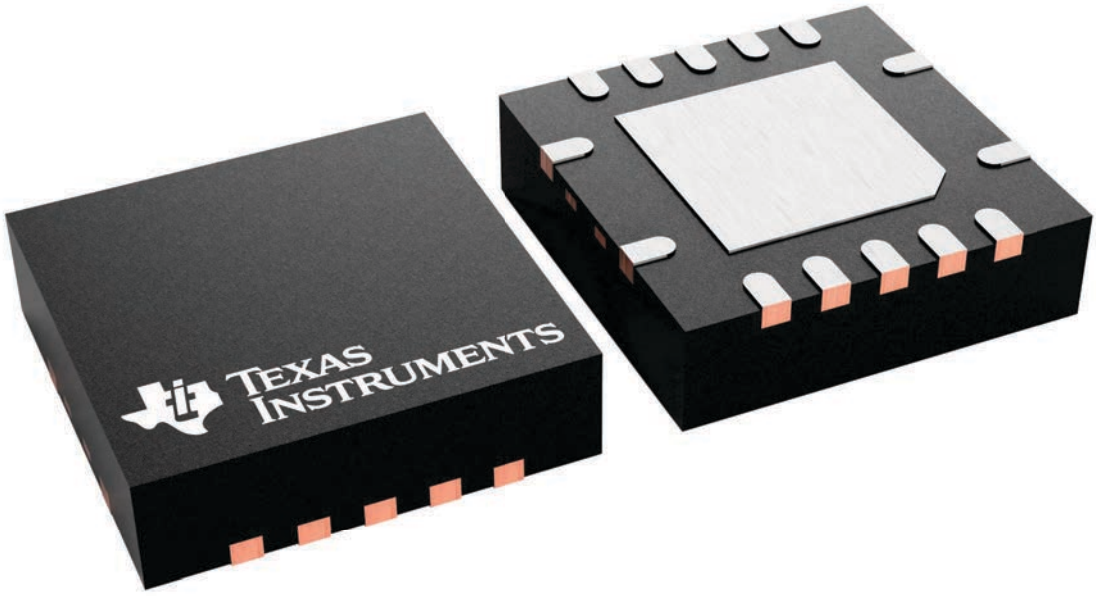
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

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