

SN74LVC1G86-Q1 Single 2-Input Exclusive-OR Gate

1 Features

- Qualified for Automotive Applications
- Supports 5V V_{CC} operation
- Inputs are over voltage tolerant up to 5.5V
- Supports down translation to V_{CC}
- Low power consumption, 15 μ A maximum I_{CC}
- Maximum t_{pd} of 6ns at 3.3V and 50pF load
- ± 24 mA output drive at 3.3V
- I_{off} supports partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Automotive HEV/EV and PowerTrain™
- Automotive infotainment and cluster
- Automotive advanced driver assistance systems
- Automotive body electronics

3 Description

The SN74LVC1G86-Q1 is an automotive qualified device that performs the Boolean function $Y = \bar{A}B + A\bar{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output. This device has low power consumption with maximum t_{pd} of 6ns at 3.3V and 50pF capacitive load. The maximum output drive is ± 32 mA at 4.5V and ± 24 mA at 3.3V.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current back flow through the device when it is powered down.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LVC1G86QDCKRQ1	SC70 (5)	2.00mm × 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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Functional Block Diagram



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4 Pin Configuration and Functions

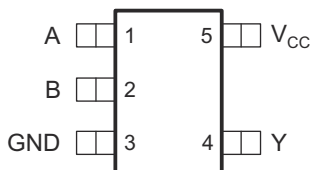


Figure 4-1. DCK Package 5-Pin SC70 Top View

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	—	Ground
V _{CC}	5	—	Positive Supply
Y	4	O	Output Y

Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	DBV, DRL, DCK	DSBGA		
A	1	A1	I	Input A
B	2	B1	I	Input B
GND	3	C1	—	Ground
V _{CC}	5	A2	—	Positive Supply
Y	4	C2	O	Output Y

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through V _{CC} or GND		±100		mA
T _J	Junction temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}	V
		V _{CC} = 2.3V to 2.7V	1.7	
		V _{CC} = 3V to 3.6V	2	
		V _{CC} = 4.5V to 5.5V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V	0.35 × V _{CC}	V
		V _{CC} = 2.3V to 2.7V	0.7	
		V _{CC} = 3V to 3.6V	0.8	
		V _{CC} = 4.5V to 5.5V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V	−4	mA
		V _{CC} = 2.3V	−8	
		V _{CC} = 3V	−16	
			−24	
		V _{CC} = 4.5V	−32	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
I_{OL} Low-level output current	$V_{CC} = 1.65V$		4	mA
	$V_{CC} = 2.3V$		8	
	$V_{CC} = 3V$		16	
			24	
	$V_{CC} = 4.5V$		32	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8V \pm 0.15V, 2.5V \pm 0.2V$		20	ns/V
	$V_{CC} = 3.3V \pm 0.3V$		10	
	$V_{CC} = 5V \pm 0.5V$		5	
T_A Operating free-air temperature	DCK package	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to maintain proper device operation. Refer to the TI application note, [Implications of Slow or Floating CMOS Inputs](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G86-Q1	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	371	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	297.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	258.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	195.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	256.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = −100 μA		1.65V to 5.5V	V _{CC} − 0.1		V	
	I _{OH} = −4mA		1.65V	1.2			
	I _{OH} = −8mA		2.3V	1.9			
	I _{OH} = −16mA		3V	2.4			
	I _{OH} = −24mA			2.3			
	I _{OH} = −32mA		4.5V	3.8			
V _{OL}	I _{OL} = 100 μA		1.65V to 5.5V	0.1		V	
	I _{OL} = 4mA		1.65V	0.45			
	I _{OL} = 8mA		2.3V	0.3			
	I _{OL} = 16mA		3V	0.4			
	I _{OL} = 24mA			0.55			
	I _{OL} = 32mA		4.5V	0.55			
I _I A or B input	V _I = 5.5V or GND		0 to 5.5V	±5		μA	
I _{off}	V _I or V _O = 5.5V		0	±10		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0		1.65V to 5.5V	15		μA	
ΔI _{CC}	One input at V _{CC} − 0.6V, Other inputs at V _{CC} or GND		3V to 5.5V	500		μA	

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
C _i	V _I = V _{CC} or GND	3.3V		6		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, C_L = 30pF or 50pF

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	–40°C to 125°C temperature range, see Figure 6-1	3.5	12	1.8	7	1.3	6	1	5	ns

5.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		UNIT
			TYP		TYP		TYP		TYP		
C _{pd}	Power dissipation capacitance	f = 10MHz	22		22		22		24		pF

5.8 Typical Characteristics

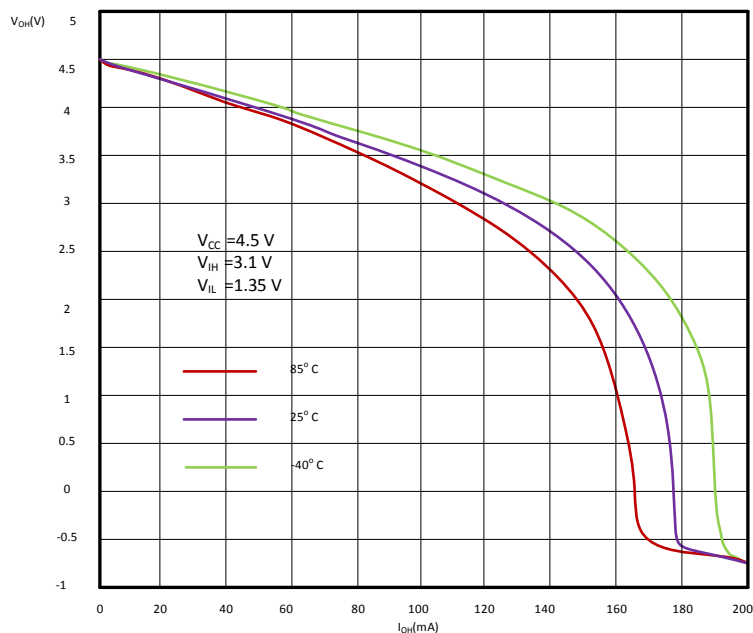
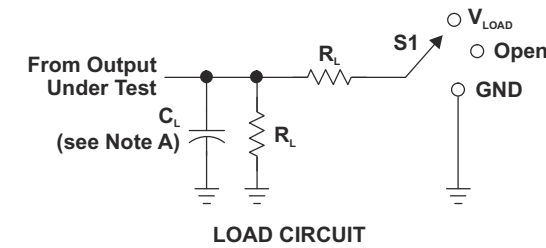


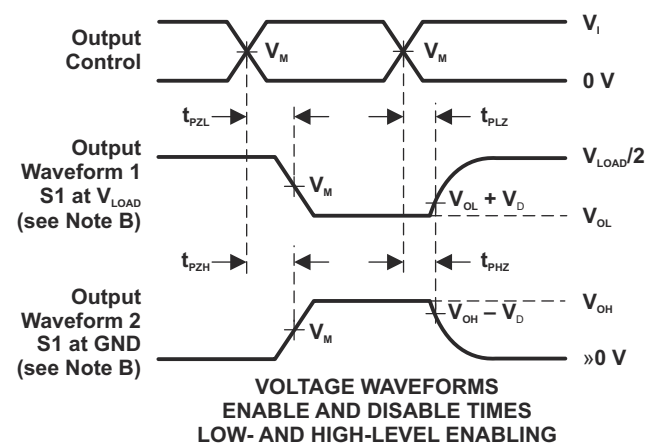
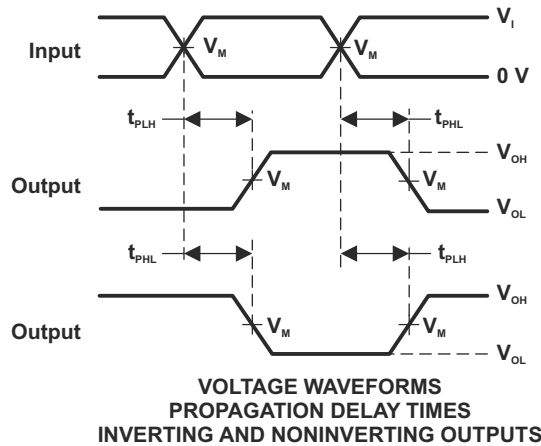
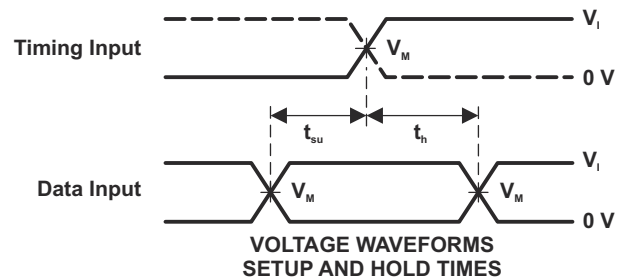
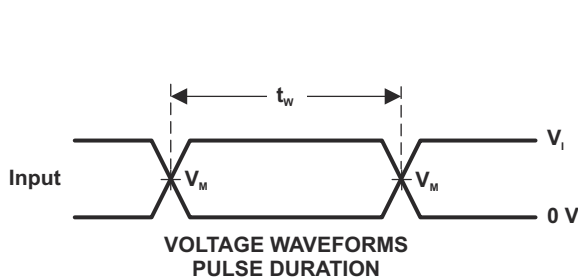
Figure 5-1. V_{OH} vs I_{OH} at 4.5V

6 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

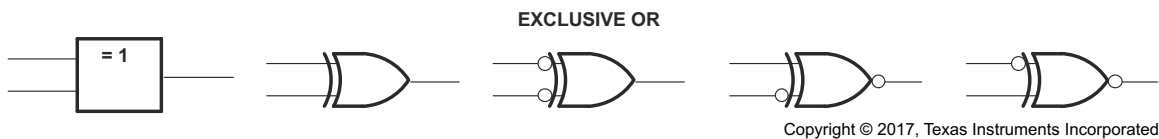
7.1 Overview

The SN74LVC1G86-Q1 is an automotive qualified device that performs the Boolean function $Y = \bar{A}B + A\bar{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

7.2 Functional Block Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86-Q1 gate in positive logic; negation can be shown at any two ports.

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the power output of the device to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Section 5.1](#) must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Section 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 5.3](#), and the maximum input leakage current, given in the [Section 5.5](#), using Ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Section 5.3](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input must be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Avoid any voltage below or above the input or output voltage specified in the [Section 5.1](#). In this event, the current must be limited to the maximum input or output clamp current value indicated in the [Section 5.1](#) to avoid damage to the device.

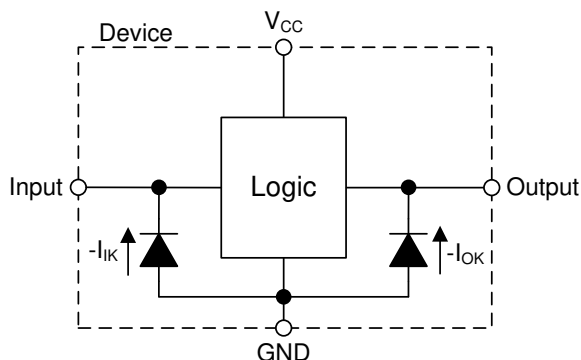


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Section 5.5](#).

7.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Section 5.3](#).

7.4 Function Table

[Table 7-1](#) lists the functional modes of the SN74LVC1G86-Q1 device.

Table 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G86-Q1 device can accept input voltages up to 5.5V at any valid V_{CC} which makes the device an excellent choice for down translation. Therefore, the SN74LVC1G86-Q1 is designed for various bus interface applications.

8.2 Typical Application

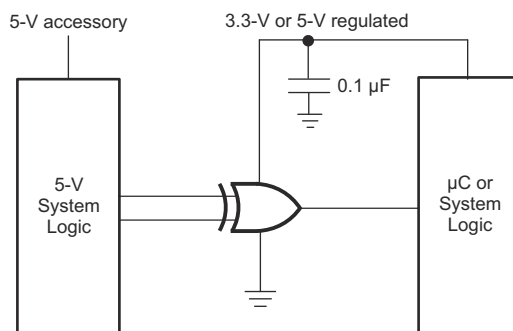


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents that exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Section 5.3](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Section 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents must not exceed 32mA per output and 50mA total for the part.
 - Outputs must not be pulled above V_{CC} .

8.2.3 Application Curve

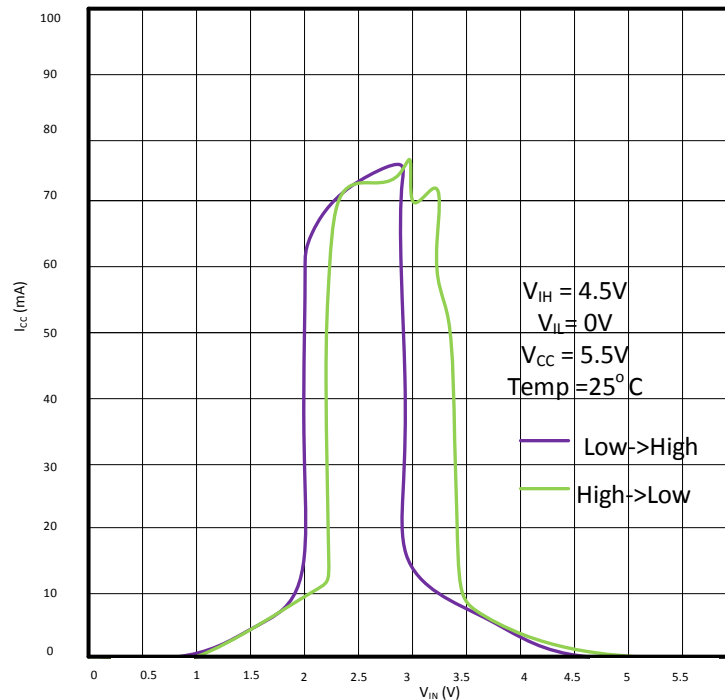


Figure 8-2. I_{CC} vs. V_{IN}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.3](#) table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. Parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8-3](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

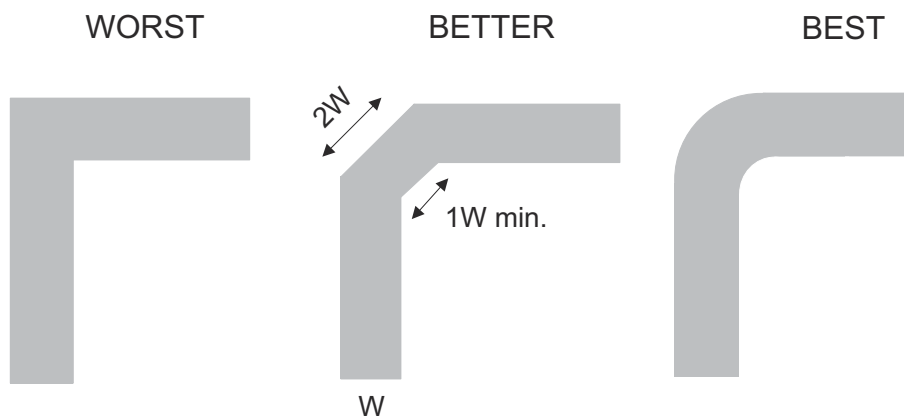


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

PowerTrain™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 1, 2016 to August 14, 2026 (from Revision * (October 2016) to Revision A (August 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed Junction-to-ambient thermal resistance value for DCK package from: 277.6°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 179.5°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 75.9°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 49.7°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 75.1°C/W to: 256.2°C/W.....	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G86QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16T
SN74LVC1G86QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16T
SN74LVC1G86QDCKRQ1.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16T
SN74LVC1G86QDCKTQ1	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16T
SN74LVC1G86QDCKTQ1.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16T

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G86-Q1 :

- Catalog : [SN74LVC1G86](#)
- Enhanced Product : [SN74LVC1G86-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

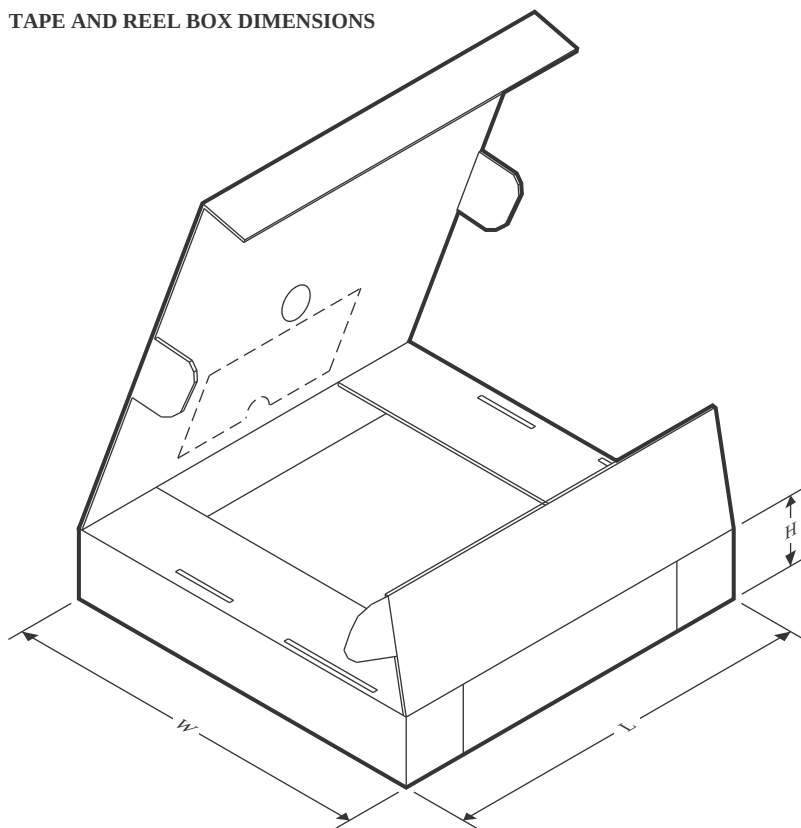
TAPE AND REEL INFORMATION



*All dimensions are nominal

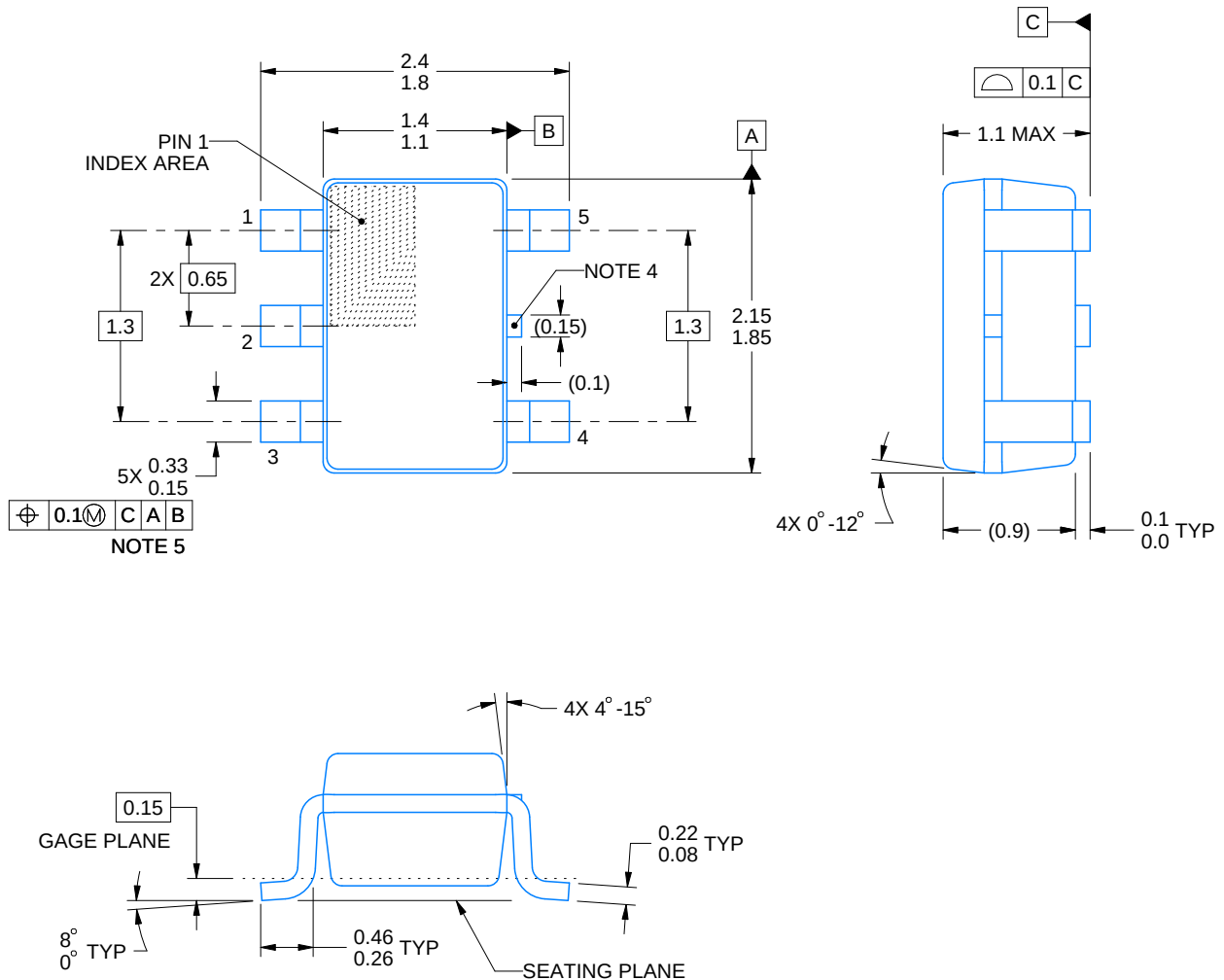
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G86QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G86QDCKTQ1	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G86QDCKTQ1	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

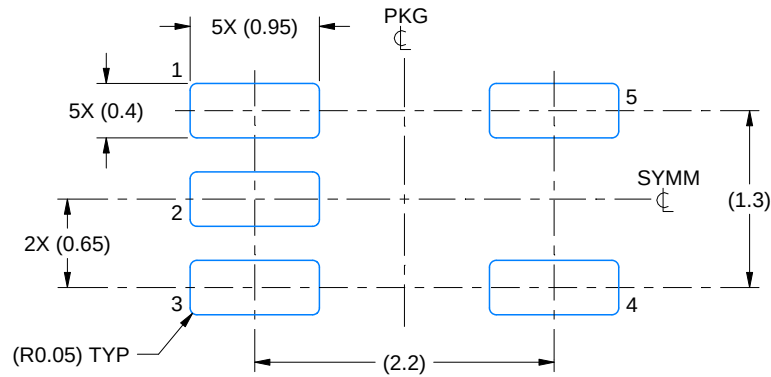
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G86QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G86QDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G86QDCKTQ1	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G86QDCKTQ1	SC70	DCK	5	250	210.0	185.0	35.0



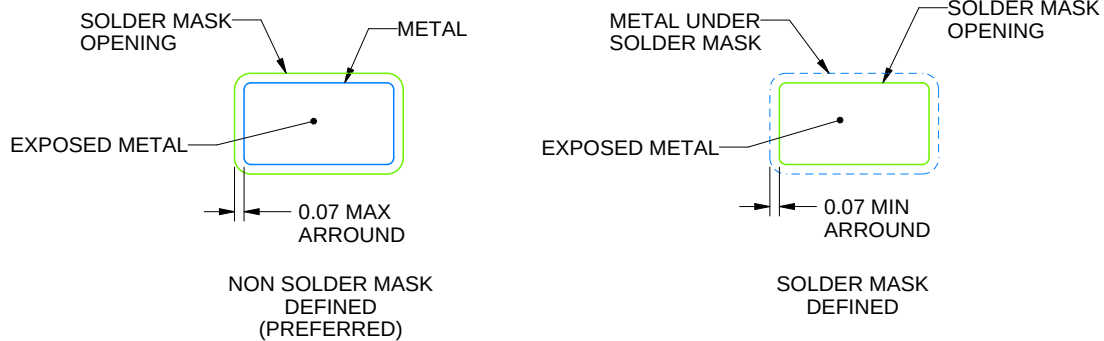
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

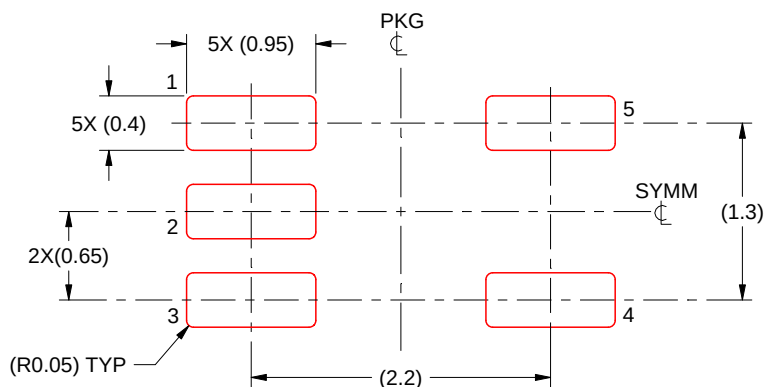


SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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