3.2W Mono Class-D Audio Power Amplifier With 6-dB Gain and Auto Short-Circuit Recovery

Check for Samples: TPA2037D1

FEATURES

- **Powerful Mono Class-D Speaker Amplifier**
  - **3.24 W (4 Ω, 5 V, 10% THDN)**
  - **2.57 W (4 Ω, 5 V, 1% THDN)**
  - **1.80 W (8 Ω, 5 V, 10% THDN)**
  - **1.46 W (8 Ω, 5 V, 1% THDN)**
- **+6 dB Fixed Gain**
- **Integrated Image Reject Filter for DAC Noise Reduction**
- **Low Output Noise of 20 μV**
- **Low Quiescent Current of 1.5 mA**
- **Differential Input Impedance of 300 kΩ**
- **Auto-Recovering Short-Circuit Protection**
- **Thermal-Overload Protection**
- **Filter-Free Mono Class-D Amp**
- **9-Ball 1,21 mm × 1,16 mm 0,4mm Pitch WCSP**

APPLICATIONS

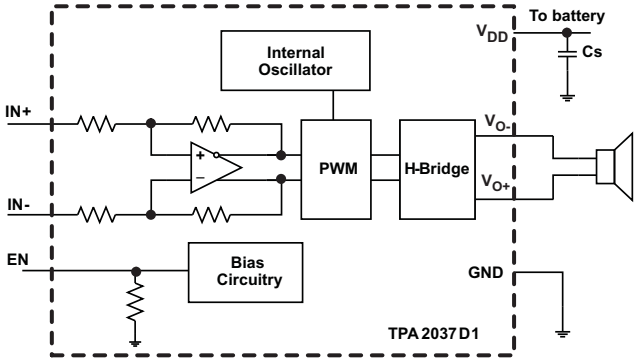
- **Wireless or Cellular Handsets and PDAs**
- **Portable Navigation Devices**
- **General Portable Audio Devices**

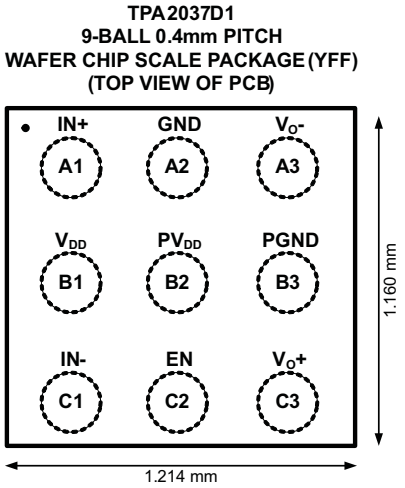
DESCRIPTION

The TPA2037D1 is a 3.2 W high efficiency filter-free class-D audio power amplifier (class-D amp) with 6 dB of fixed gain in a 1.21 mm x 1.16 mm wafer chip scale package (WCSP). The device requires only one external component.

Features like 95% efficiency, 1.5 mA quiescent current, 0.1 μA shutdown current, 81-dB PSRR, 20 μV output noise, and improved RF immunity make the TPA2037D1 class-D amplifier ideal for cellular handsets. A start-up time of 4 ms with no audible pop makes the TPA2037D1 ideal for PDA and smart-phone applications.

APPLICATION CIRCUIT





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES(1)	PART NUMBER(2)	SYMBOL
—40°C to 85°C	9-ball WSCP	TPA2037D1YFFR	OCA
		TPA2037D1YFFT	OCA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com
(2) The YFF package is only available taped and reeled. The suffix "R" indicates a reel of 3000, the suffix "T" indicates a reel of 250.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)(1)

			VALUE	UNIT
V_{DD}, PV_{DD}	Supply voltage	In active mode	–0.3 to 6.0	V
		In shutdown mode	–0.3 to 6.0	V
V_I	Input voltage	EN, IN+, IN–	–0.3 to V_{DD} + 0.3	V
R_L	Minimum load resistance		3.2	Ω
	Output continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR(1)	T_A < 25°C	T_A = 70°C	T_A = 85°C
YFF (WCSP)	4.2 mW/°C	525 mW	336 mW	273 mW

(1) Derating factor measure with high K board.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}, PV_{DD}	Class-D supply voltage		2.5	5.5	V
V_{IH}	High-level input voltage	EN	1.3		V
V_{IL}	Low-level input voltage	EN		0.35	V
V_{IC}	Common mode input voltage range	V_{DD} = 2.5V, 5.5V, CMRR ≥ 49 dB	0.75	V_{DD}-1.1	V
T_A	Operating free-air temperature		–40	85	°C

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ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V, V_{DD} = 2.5 V to 5.5 V		1	5	mV
$\|I_{IH}\|$	High-level EN input current	V_{DD} = 5.5 V, V_{EN} = 5.5 V			50	µA
$\|I_{IL}\|$	Low-level EN input current	V_{DD} = 5.5 V, V_{EN} = 0 V			1	µA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load		1.8	2.5	mA
		V_{DD} = 3.6 V, no load		1.5	2.3	
		V_{DD} = 2.5 V, no load		1.3	2.1	
$I_{(SD)}$	Shutdown current	V_{EN} = 0.35 V, V_{DD} = 3.6 V		0.1	2	µA
$R_{O, SD}$	Output impedance in shutdown mode	V_{EN} = 0.35 V		2		kΩ
$f_{(SW)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	250	300	350	kHz
A_V	Gain	V_{DD} = 2.5 V to 5.5 V, R_L = no load	5.5	6.0	6.5	dB
R_{EN}	Resistance from EN to GND			300		kΩ
R_{IN}	Single ended input resistance	$V_{EN} \geq V_{IH}$		150		kΩ
		$V_{EN} \leq V_{IL}$		75		

OPERATING CHARACTERISTICS

V_{DD} = 3.6 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 10%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		3.24		W
			V_{DD} = 3.6 V		1.62		
			V_{DD} = 2.5 V		0.70		
		THD + N = 1%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.57		W
			V_{DD} = 3.6 V		1.32		
			V_{DD} = 2.5 V		0.57		
		THD + N = 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.80		W
			V_{DD} = 3.6 V		0.91		
			V_{DD} = 2.5 V		0.42		
		THD + N = 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.46		W
			V_{DD} = 3.6 V		0.74		
			V_{DD} = 2.5 V		0.33		
V_n	Noise output voltage	V_{DD} = 3.6 V, Inputs AC grounded with C_I = 2µF, f = 20 Hz to 20 kHz	A-weighting		20		$µV_{RMS}$
			No weighting		26		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5.0 V, P_O = 1.0 W, f = 1 kHz, R_L = 8 Ω			0.12%		
		V_{DD} = 3.6 V, P_O = 0.5 W, f = 1 kHz, R_L = 8 Ω			0.05%		
		V_{DD} = 2.5 V, P_O = 0.2 W, f = 1 kHz, R_L = 8 Ω			0.05%		
		V_{DD} = 5.0 V, P_O = 2.0 W, f = 1 kHz, R_L = 4 Ω			0.32%		
		V_{DD} = 3.6 V, P_O = 1.0 W, f = 1 kHz, R_L = 4 Ω			0.11%		
		V_{DD} = 2.5 V, P_O = 0.4 W, f = 1 kHz, R_L = 4 Ω			0.12%		
PSRR	AC power supply rejection ratio	V_{DD} = 3.6 V, Inputs AC grounded with C_I = 2 µF, 200 mV_{pp} ripple, f = 217 Hz			81		dB
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{PP}, f = 217 Hz			79		dB
T_{SU}	Startup time from shutdown	V_{DD} = 3.6 V			4		ms

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OPERATING CHARACTERISTICS (continued)

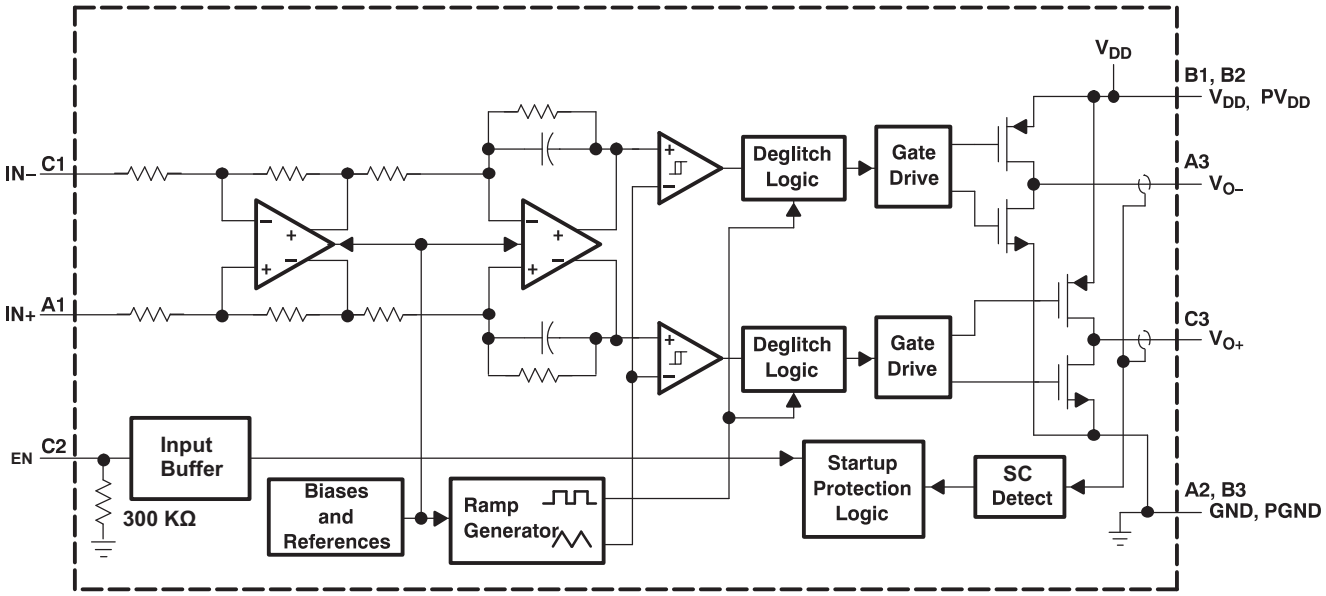
V_{DD} = 3.6 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	Short circuit protection threshold	V_{DD} = 3.6 V, V_{O+} shorted to VDD		2		A
		V_{DD} = 3.6 V, V_{O-} shorted to VDD		2		
		V_{DD} = 3.6 V, V_{O+} shorted to GND		2		
		V_{DD} = 3.6 V, V_{O-} shorted to GND		2		
		V_{DD} = 3.6 V, V_{O+} shorted to V_{O-}		2		
T_{AR}	Time for which output is disabled after a short circuit event, after which auto-recovery trials are continuously made	V_{DD} = 2.5 V to 5.5 V		100		ms

Terminal Functions

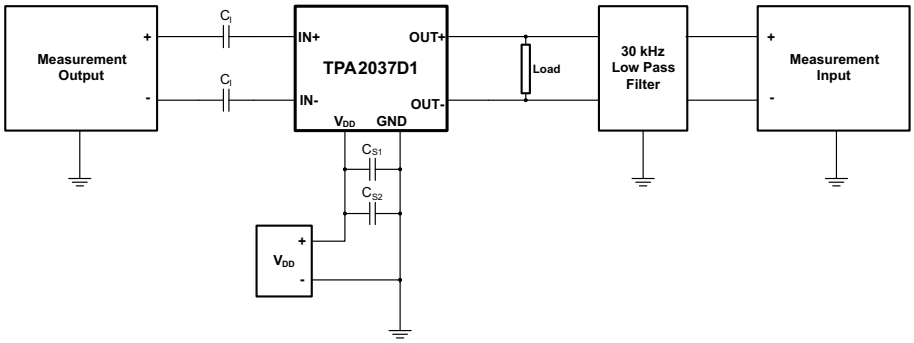
TERMINAL		I/O	DESCRIPTION
NAME	WCSP BALL		
IN–	C1	I	Negative differential audio input.
IN+	A1	I	Positive differential audio input.
V_{O-}	A3	O	Negative BTL audio output.
V_{O+}	C3	O	Positive BTL audio output.
GND	A2	I	Analog ground terminal. Must be connected to same potential as PGND using a direct connection to a single point ground.
PGND	B3	I	High-current Analog ground terminal. Must be connected to same potential as GND using a direct connection to a single point ground.
V_{DD}	B1	I	Power supply terminal. Must be connected to same power supply as PV_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
PV_{DD}	B2	I	High-current Power supply terminal. Must be connected to same power supply as V_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
EN	C2	I	Enable terminal. Connect to Logic High voltage to enable device, Logic Low voltage to disable (shutdown).

FUNCTIONAL BLOCK DIAGRAM



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TEST SETUP FOR GRAPHS



1. C_I was shorted for any common-mode input voltage measurement. All other measurements were taken with C_I = 0.1-μF (unless otherwise noted).
2. C_{S1} = 0.1μF is placed very close to the device. The optional C_{S2} = 10μF is used for datasheet graphs.
3. The 30-kHz low-pass filter is required even if the analyzer has an internal low-pass filter. An RC low-pass filter (1kΩ, 4700pF) is used on each output for the data sheet graphs.

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TYPICAL CHARACTERISTICS

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

EFFICIENCY vs OUTPUT POWER

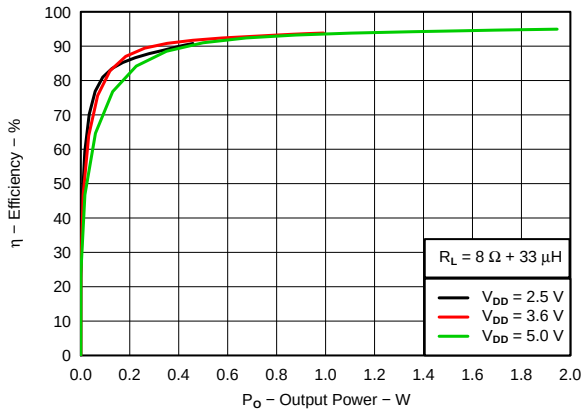


Figure 1.

EFFICIENCY vs OUTPUT POWER

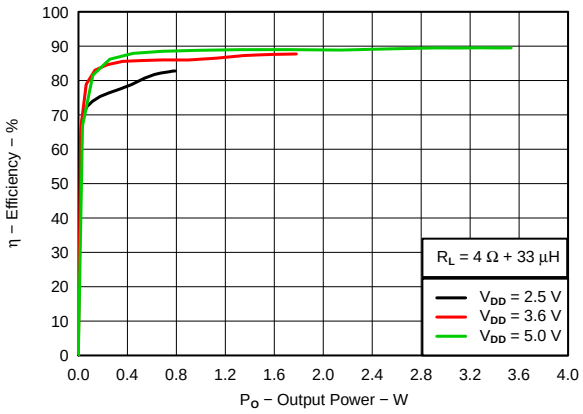


Figure 2.

POWER DISSIPATION vs OUTPUT POWER

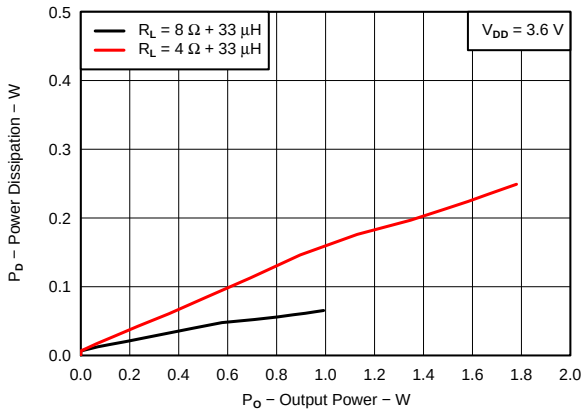


Figure 3.

POWER DISSIPATION vs OUTPUT POWER

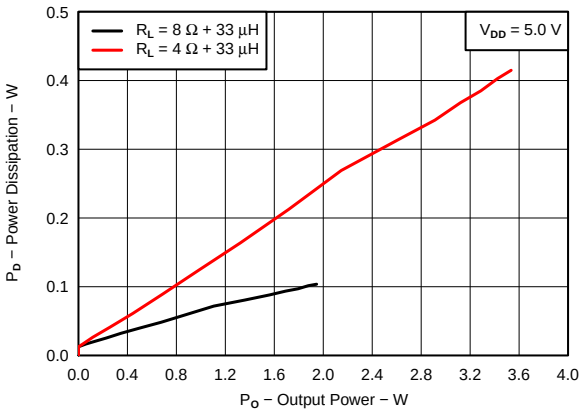


Figure 4.

SUPPLY CURRENT vs OUTPUT POWER

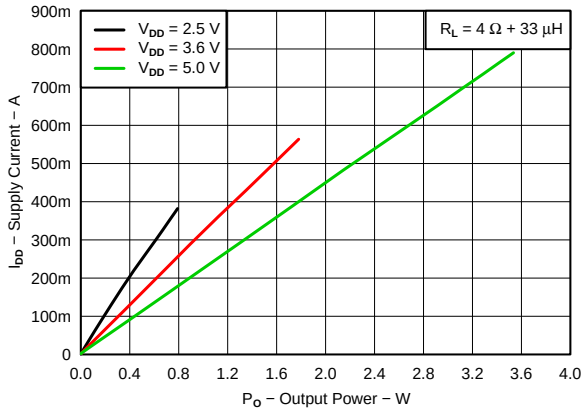


Figure 5.

SUPPLY CURRENT vs OUTPUT POWER

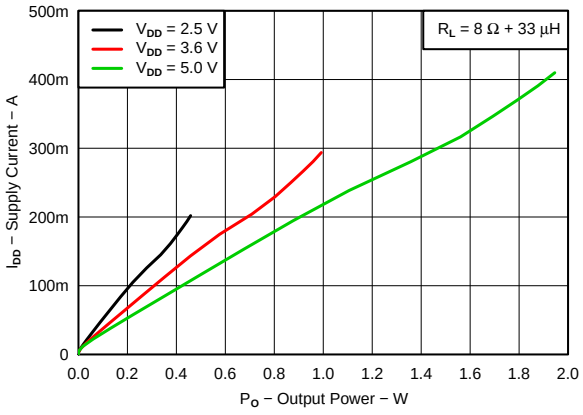


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

SUPPLY CURRENT vs SUPPLY VOLTAGE

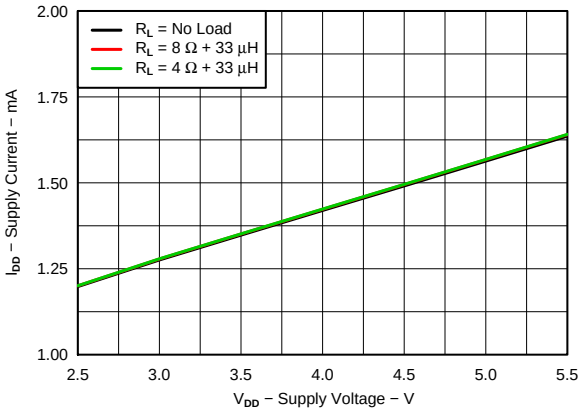


Figure 7.

SUPPLY CURRENT vs EN VOLTAGE

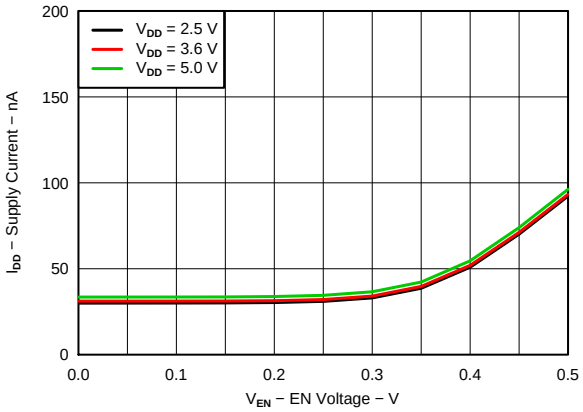


Figure 8.

OUTPUT POWER vs LOAD RESISTANCE

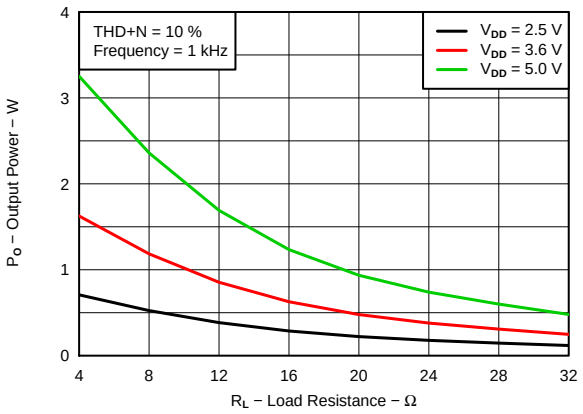


Figure 9.

OUTPUT POWER vs LOAD RESISTANCE

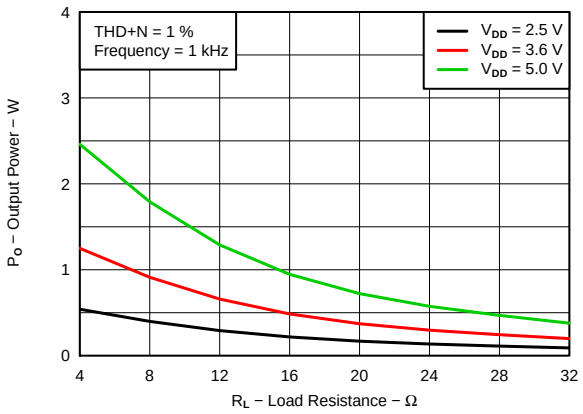


Figure 10.

OUTPUT POWER vs SUPPLY VOLTAGE

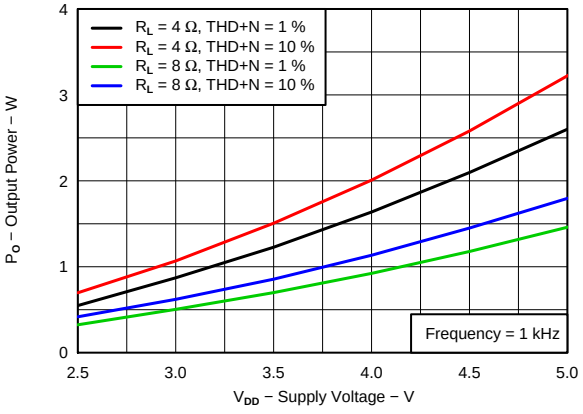


Figure 11.

THD + NOISE vs OUTPUT POWER

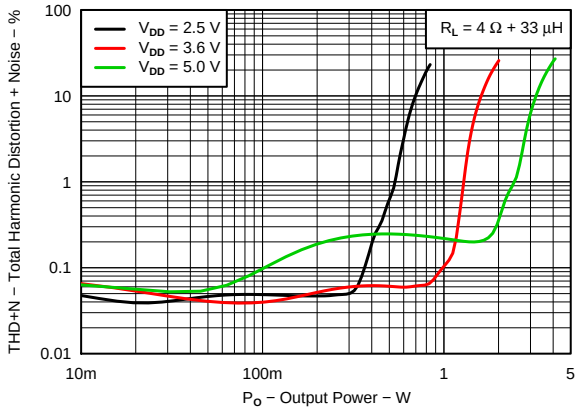


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

THD + NOISE vs OUTPUT POWER

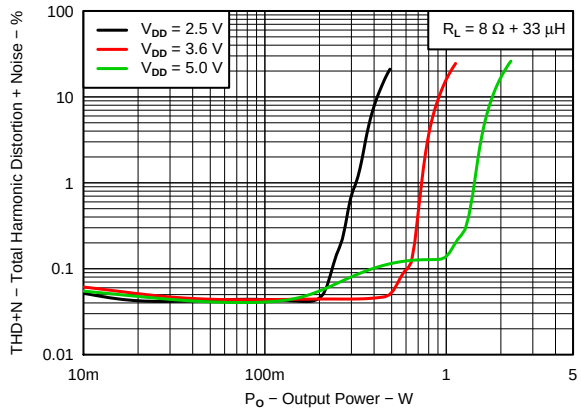


Figure 13.

THD + NOISE vs FREQUENCY

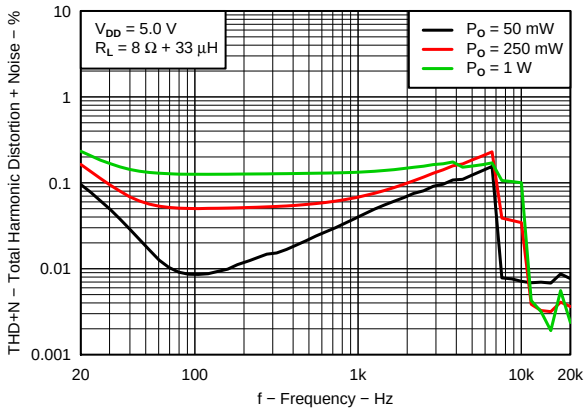


Figure 14.

THD + NOISE vs FREQUENCY

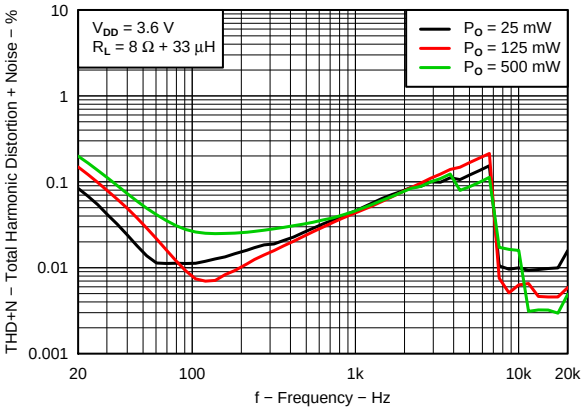


Figure 15.

THD + NOISE vs FREQUENCY

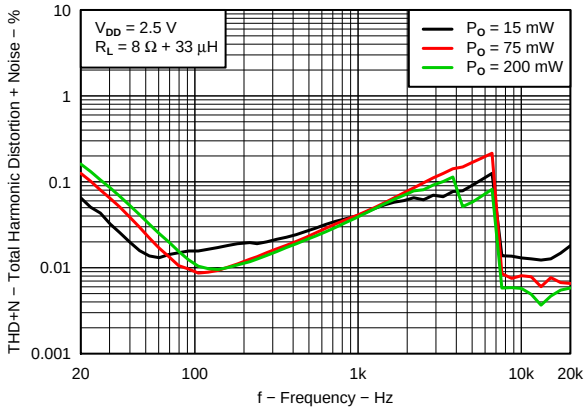


Figure 16.

THD + NOISE vs FREQUENCY

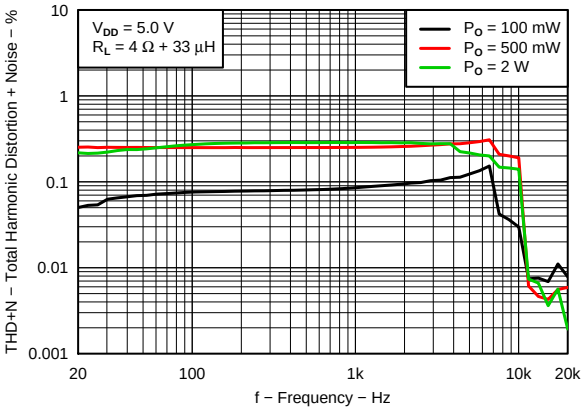


Figure 17.

THD + NOISE vs FREQUENCY

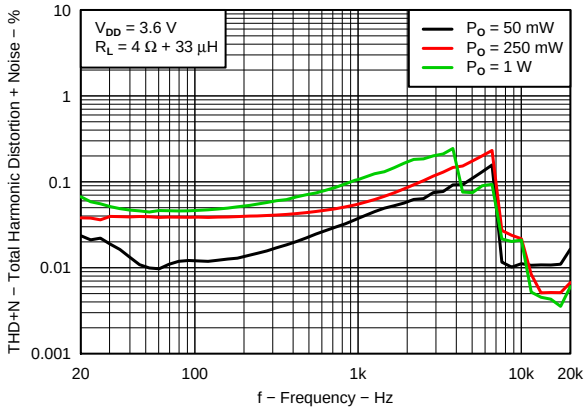


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

THD + NOISE vs FREQUENCY

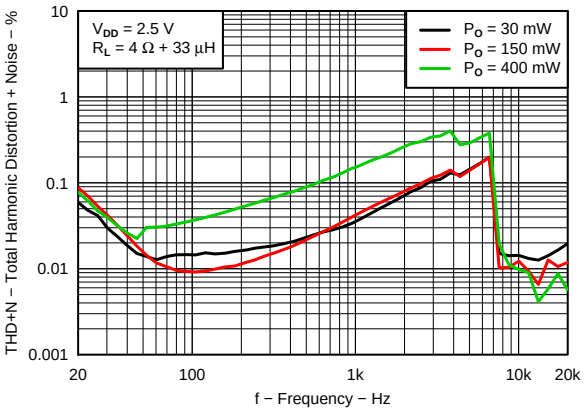


Figure 19.

THD + NOISE vs COMMON MODE INPUT VOLTAGE

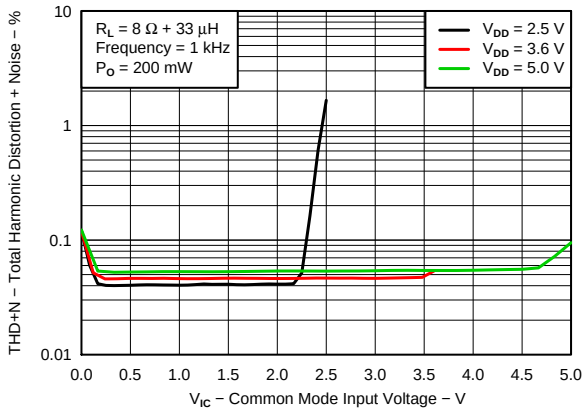


Figure 20.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

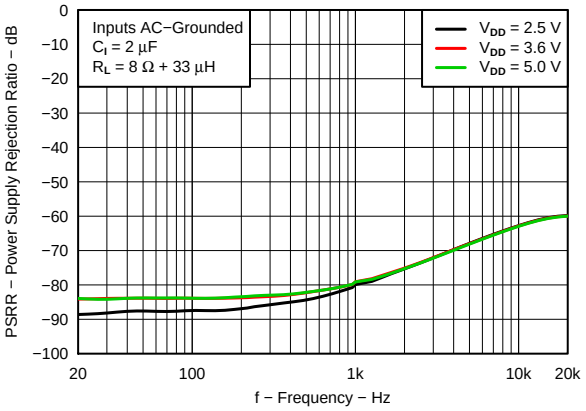


Figure 21.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

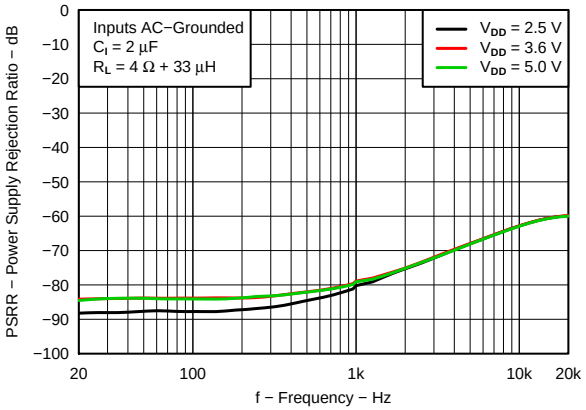


Figure 22.

POWER SUPPLY REJECTION RATIO vs COMMON MODE INPUT VOLTAGE

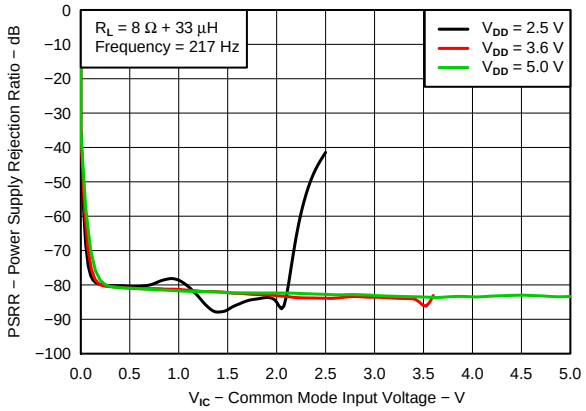


Figure 23.

COMMON MODE REJECTION RATIO vs FREQUENCY

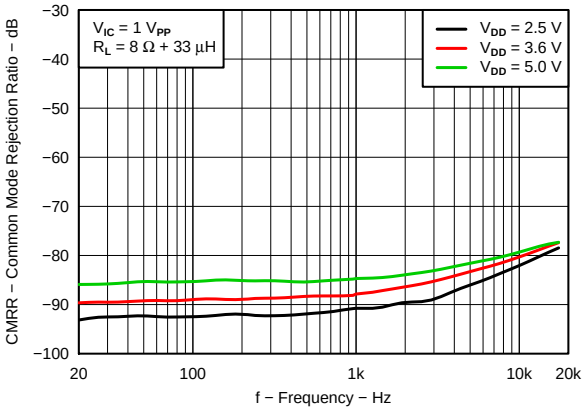


Figure 24.

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TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.6 V, C_I = 0.1 µF, C_{S1} = 0.1 µF, C_{S2} = 10 µF, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

COMMON MODE REJECTION RATIO vs COMMON MODE INPUT VOLTAGE

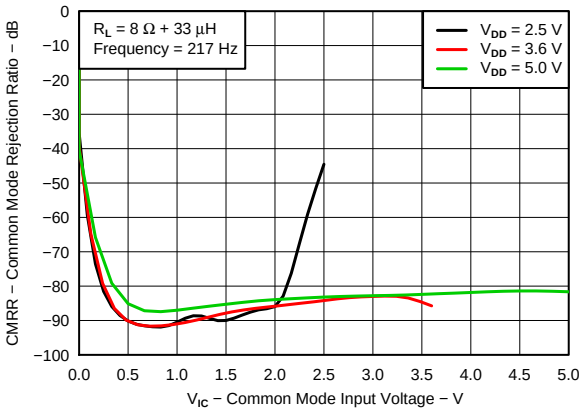


Figure 25.

GSM POWER SUPPLY REJECTION vs TIME

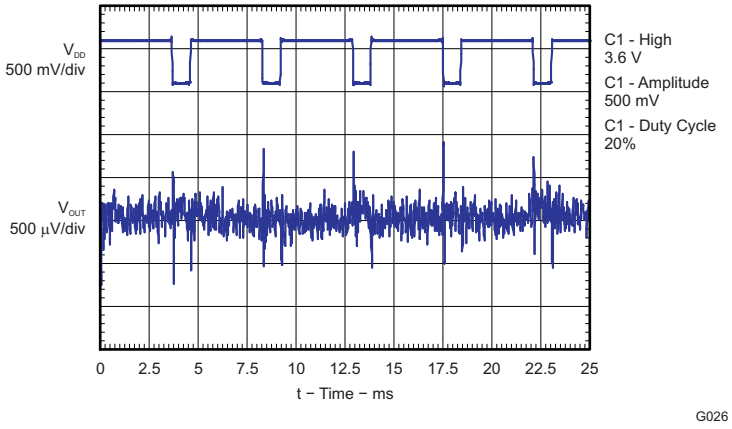


Figure 26.

GSM POWER SUPPLY REJECTION vs FREQUENCY

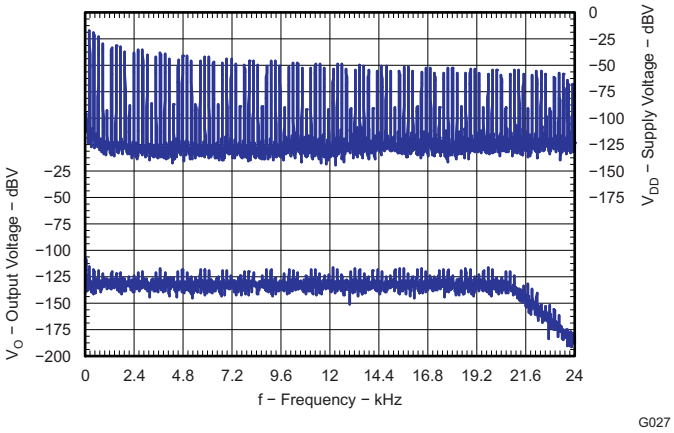


Figure 27.

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APPLICATION INFORMATION

SHORT CIRCUIT AUTO-RECOVERY

When a short-circuit event occurs, the TPA2037D1 goes to shutdown mode and activates the integrated auto-recovery process whose aim is to return the device to normal operation once the short-circuit is removed. This process repeatedly examines (once every 100ms) whether the short-circuit condition persists, and returns the device to normal operation immediately after the short-circuit condition is removed. This feature helps protect the device from large currents and maintain a good long-term reliability.

INTEGRATED IMAGE REJECT FILTER FOR DAC NOISE REJECTION

In applications which use a DAC to drive Class-D amplifiers, out-of-band noise energy present at the DAC's image frequencies fold back into the audio-band at the output of the Class-D amplifier. An external low-pass filter is often placed between the DAC and the Class-D amplifier in order to attenuate this noise.

The TPA2037D1 has an integrated Image Reject Filter with a low-pass cutoff frequency of 130 kHz, which significantly attenuates this noise. Depending on the system noise specification, the integrated Image Reject Filter may help eliminate external filtering, thereby saving board space and component cost.

COMPONENT SELECTION

Figure 28 shows the TPA2037D1 typical schematic with differential inputs, while Figure 29 shows the TPA2037D1 with differential inputs and input capacitors. Figure 30 shows the TPA2037D1 with a single-ended input.

Decoupling Capacitors (C_{S1}, C_{S2})

The TPA2037D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor C_{S1} = 0.1μF , placed as close as possible to the device V_{DD} lead works best. Placing C_{S1} close to the TPA2037D1 is important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 μF or greater capacitor (C_{S2}) placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device. Typically, the smaller the capacitor's case size, the lower the inductance and the closer it can be placed to the TPA2037D1. X5R and X7R dielectric capacitors are recommended for both C_{S1} and C_{S2}.

Input Capacitors (C_I)

The TPA2037D1 does not require input coupling capacitors if the design uses a differential source that is biased within the common-mode input voltage range. That voltage range is listed in the Recommended Operating Conditions table. If the input signal is not biased within the recommended common-mode input range, such as in needing to use the input as a high pass filter, shown in Figure 29, or if using a single-ended source, shown in Figure 30, input coupling capacitors are required. The same value capacitors should be used on both IN+ and IN– for best pop performance. The 3-dB high-pass cutoff frequency f_C of the filter formed by the input coupling capacitor C_I and the input resistance R_I (typically 150 kΩ) of the TPA2037D1 is given by Equation 1:

$$f_C = \frac{1}{(2\pi R_I C_I)} \quad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speaker response may also be taken into consideration when setting the corner frequency using input capacitors. Solving for the input coupling capacitance, we get:

$$C_I = \frac{1}{(2\pi R_I f_C)} \quad (2)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

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For a flat low-frequency response, use large input coupling capacitors (0.1 μF or larger). X5R and X7R dielectric capacitors are recommended.

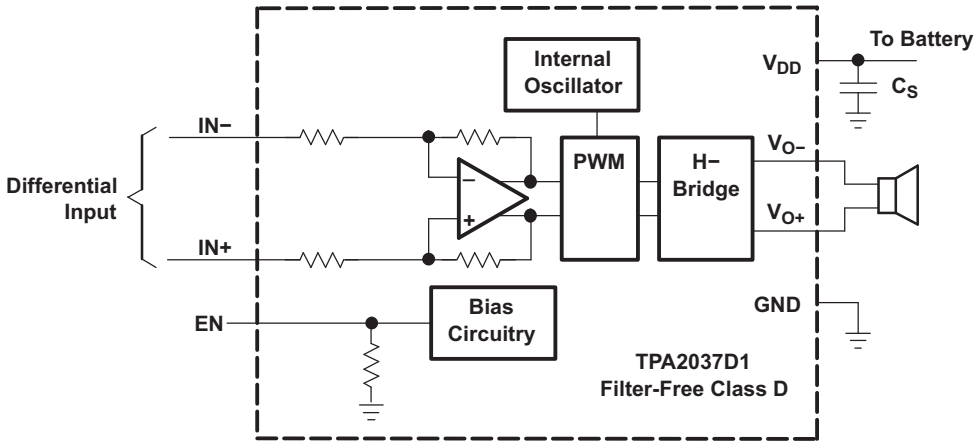


Figure 28. Typical TPA2037D1 Application Schematic With DC-coupled Differential Input

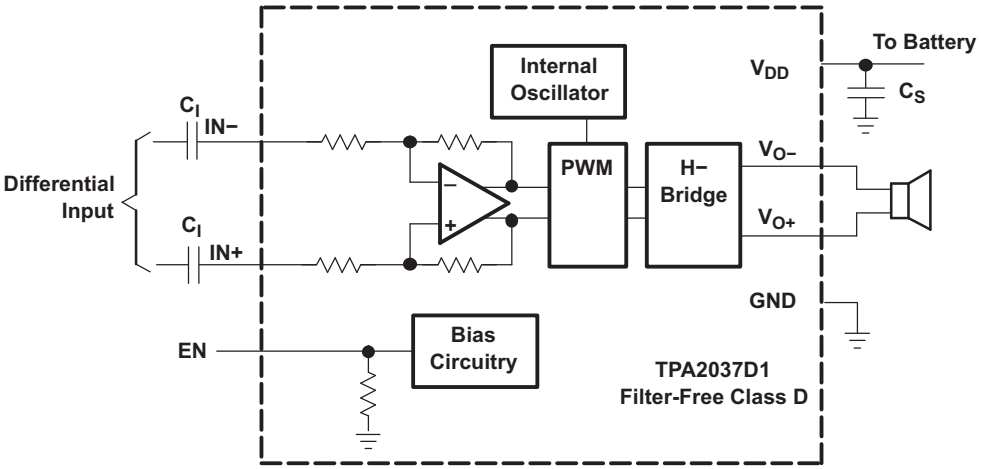


Figure 29. TPA2037D1 Application Schematic With Differential Input and Input Capacitors

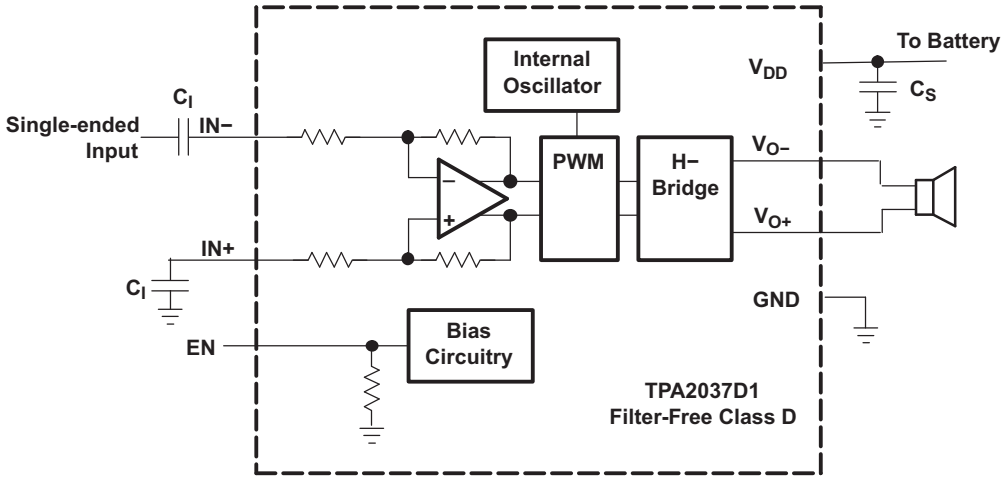


Figure 30. TPA2037D1 Application Schematic With Single-Ended Input

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EFFICIENCY AND THERMAL INFORMATION

The maximum ambient operating temperature of the TPA2037D1 depends on the load resistance, power supply voltage and heat-sinking ability of the PCB system. The derating factor for the YFF package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} \quad (3)$$

Given θ_{JA} (from the Package Dissipation ratings table), the maximum allowable junction temperature (from the Absolute Maximum ratings table), and the maximum internal dissipation (from Power Dissipation vs Output Power figures) the maximum ambient temperature can be calculated with the following equation. Note that the units on these figures are Watts RMS. Because of crest factor (ratio of peak power to RMS power) from 9–15 dB, thermal limitations are not usually encountered.

$$T_A Max = T_J Max - \theta_{JA} P_D max \quad (4)$$

The TPA2037D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Note that the use of speakers less resistive than 4-Ω (typ) is not advisable. Below 4-Ω (typ) the thermal performance of the device dramatically reduces because of increased output current and reduced amplifier efficiency. The Absolute Maximum rating of 3.2-Ω covers the manufacturing tolerance of a 4-Ω speaker and speaker impedance decrease due to frequency. θ_{JA} is a gross approximation of the complex thermal transfer mechanisms between the device and its ambient environment. If the θ_{JA} calculation reveals a potential problem, a more accurate estimate should be made.

WHEN TO USE AN OUTPUT FILTER

Design the TPA2037D1 without an Inductor / Capacitor (LC) output filter if the traces from the amplifier to the speaker are short. Wireless handsets and PDAs are great applications for this class-D amplifier to be used without an output filter.

The TPA2037D1 does not require an LC output filter for short speaker connections (approximately 100 mm long or less). A ferrite bead can often be used in the design if failing radiated emissions testing without an LC filter; and, the frequency-sensitive circuit is greater than 1 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. The selection must also take into account the currents flowing through the ferrite bead. Ferrites can begin to loose effectiveness at much lower than rated current values. See the EVM User's Guide (SLOU266) for components used successfully by TI.

Figure 31 shows a typical ferrite-bead output filter.

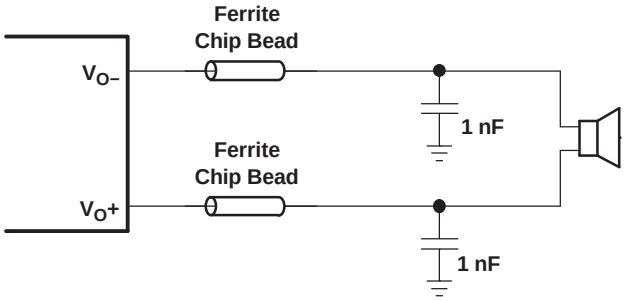


Figure 31. Typical Ferrite Chip Bead Filter

PRINTED CIRCUIT BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 32 shows the appropriate diameters for a WCSP layout.

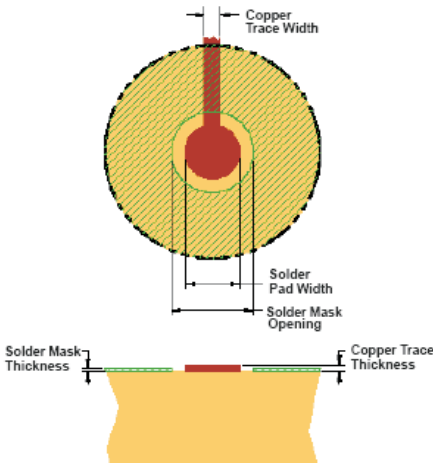


Figure 32. Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING(5)	COPPER THICKNESS	STENCIL OPENING(6)(7)	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	0.23 mm	0.310 mm	1 oz max (0.032 mm)	0.275 mm x 0.275 mm Sq. (rounded corners)	0.1 mm thick

1. Circuit traces from NSMD defined PWB lands should be 75 μm to 100 μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
3. Recommend solder paste is Type 3 or Type 4.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 μm on top of the copper circuit pattern
6. Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils give inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

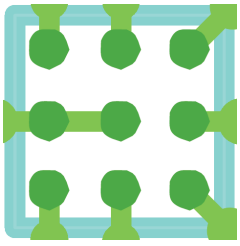


Figure 33. Layout Snapshot

An on-pad via is not required to route the middle ball B2 (PV_{DD}) of the TPA2037D1. Just short ball B2 (PV_{DD}) to ball B1 (V_{DD}) and connect both to the supply trace as shown in Figure 33. This simplifies board routing and saves manufacturing cost.

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PACKAGE DIMENSIONS

D	E
Max = 1190µm	Max = 1244µm
Min = 1130µm	Min = 1184µm

REVISION HISTORY

Changes from Original (October 2009) to Revision A **Page**

- Changed graph using supplied data 10
- Changed graph using supplied data 10
- Added package dimensions table 15

Changes from Revision A (December 2009) to Revision B **Page**

- Changed the Package Dimensions table. D was Max = 1244µm, Min = 1184µm. E was Max = 1190µm, Min = 1130µm 15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA2037D1YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OCA	Samples
TPA2037D1YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	OCA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

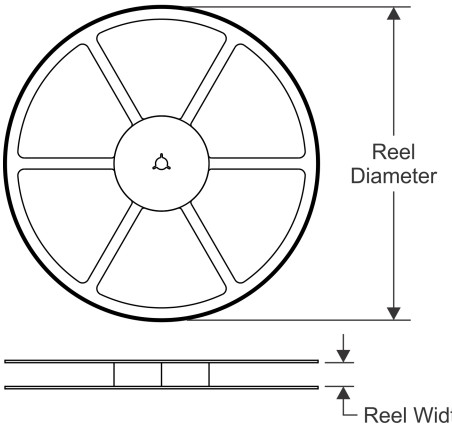
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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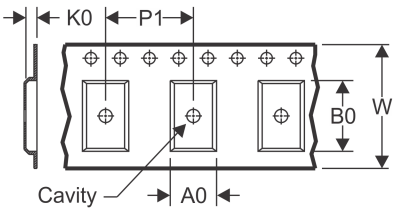
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

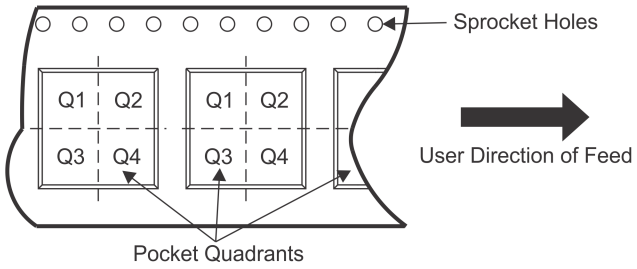


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

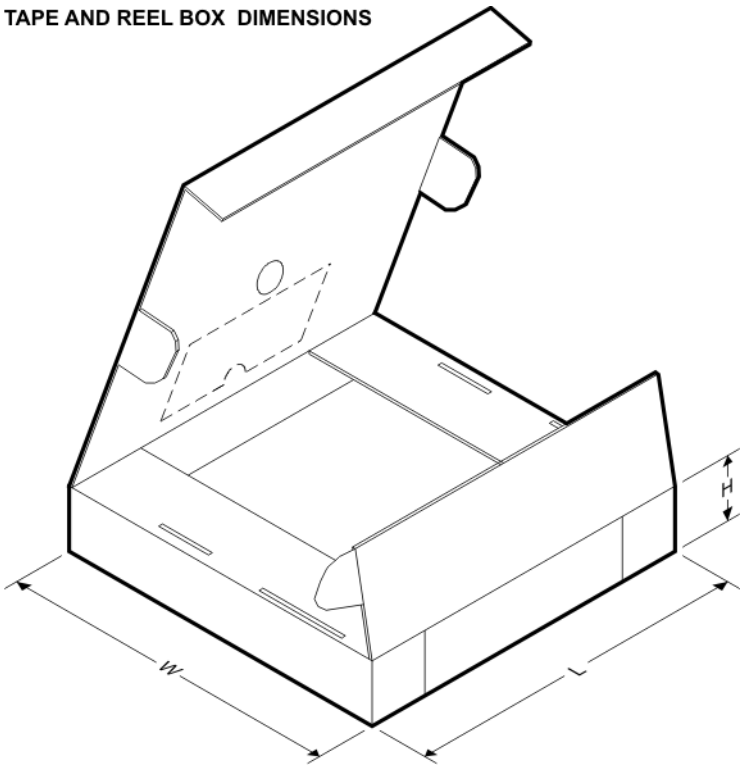
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2037D1YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPA2037D1YFFT	DSBGA	YFF	9	250	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

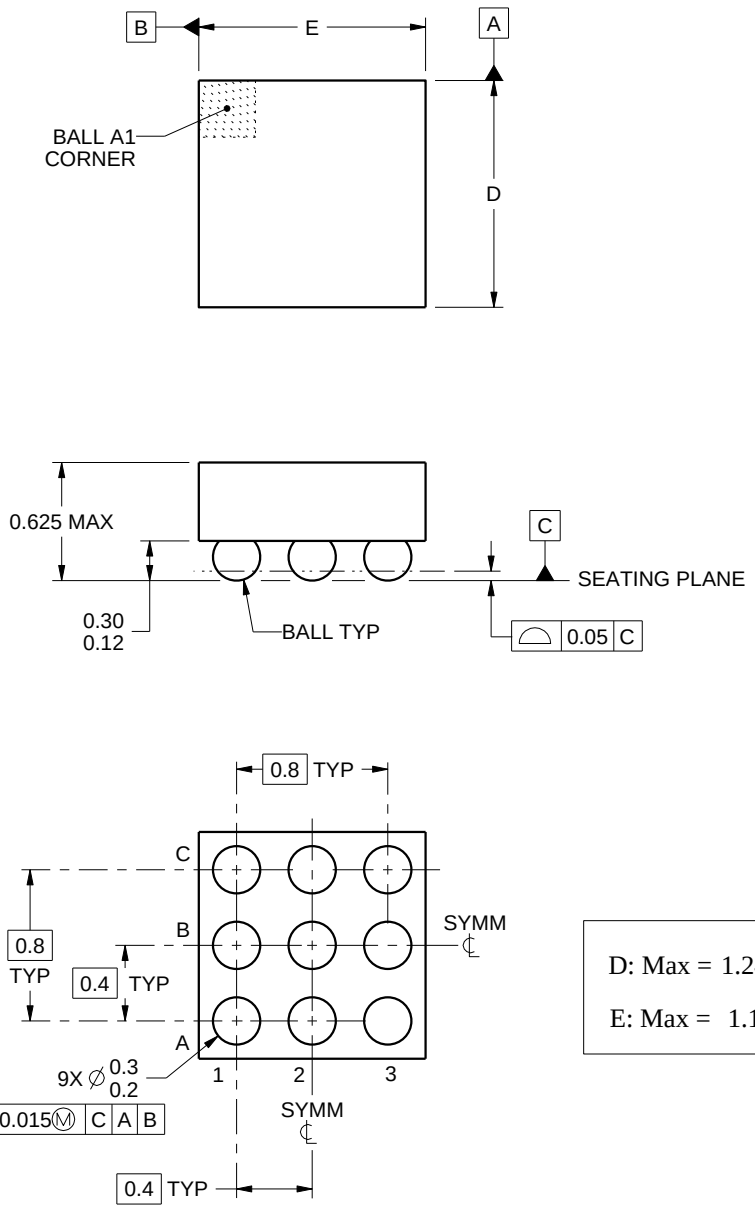
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2037D1YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPA2037D1YFFT	DSBGA	YFF	9	250	210.0	185.0	35.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



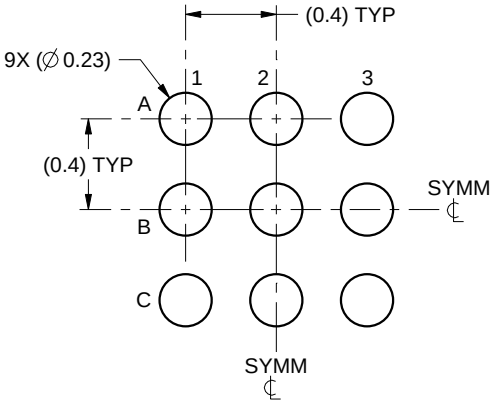
D: Max = 1.244 mm, Min =1.184 mm

E: Max = 1.19 mm, Min = 1.13 mm

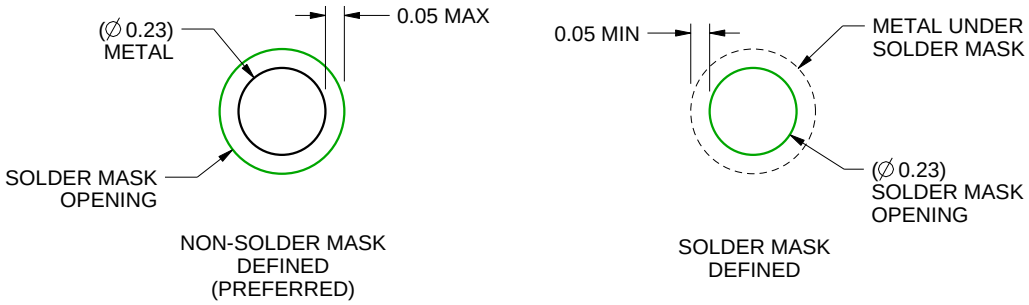
4219552/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

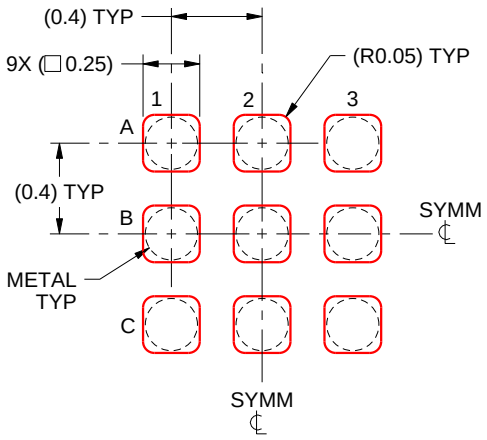


SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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