PCF2131

Nano-Power Highly Accurate RTC with Integrated Quartz Crystal

Rev. 2.5 — 26 June 2026 Product data sheet

1 General description

The PCF2131 is a CMOS RTC and calendar. It comes with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for high accuracy and ultra-low power consumption. The PCF2131 has a selectable I^2C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, four timestamps function, and many other features.

For a selection of NXP RTCs, see Section 19.1.

2 Features and benefits

- Operating temperature ranges from -40 °C to +85 °C
- TCXO with trimmed integrated capacitors
- Ultra low supply current: typical 64 nA at V_{DD} = 3.3 V
- Temperature compensated RTC, typical accuracy ±3 ppm from -40 °C to +85 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds, and 1/100 seconds
- Provides leap year correction
- Timestamp function
  - with interrupt capability
  - detection of four different events on four input pins (for example, for tamper detection)
- 2-line bidirectional 400 kHz Fast-mode I^2C-bus interface
- 4-line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Power-on Reset (POR)
- Software reset function
- Two interrupt outputs (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable watchdog timer with interrupt
- Programmable alarm function with interrupt capability
- Programmable square output
- Clock operating voltage: 1.2 V to 5.5 V

3 Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- Global Positioning System (GPS) equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4 Ordering information

This section describes the ordering information for PCF2131.

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCF2131TF	F31	HLSON16	Thermal enhanced low profile small outline; no leads, 16 terminals, 0.125 dimple wettable flank, 0.5 mm pitch, 4.5 mm x 3.5 mm x 1.45 mm body	SOT1992-1

4.1 Ordering options

This section describes the ordering options for PCF2131.

Table 2. Ordering options

Product type number	Orderable part number	Package	Packing method	Minimum Order Quantity	Temperature
PCF2131TF	PCF2131TFY	HLSON16	REEL 13" Q1 DP	4000	T_{amb} = -40 °C to +85 °C

5 Block diagram

Figure 1 shows the labeled block diagram of PCF2131.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

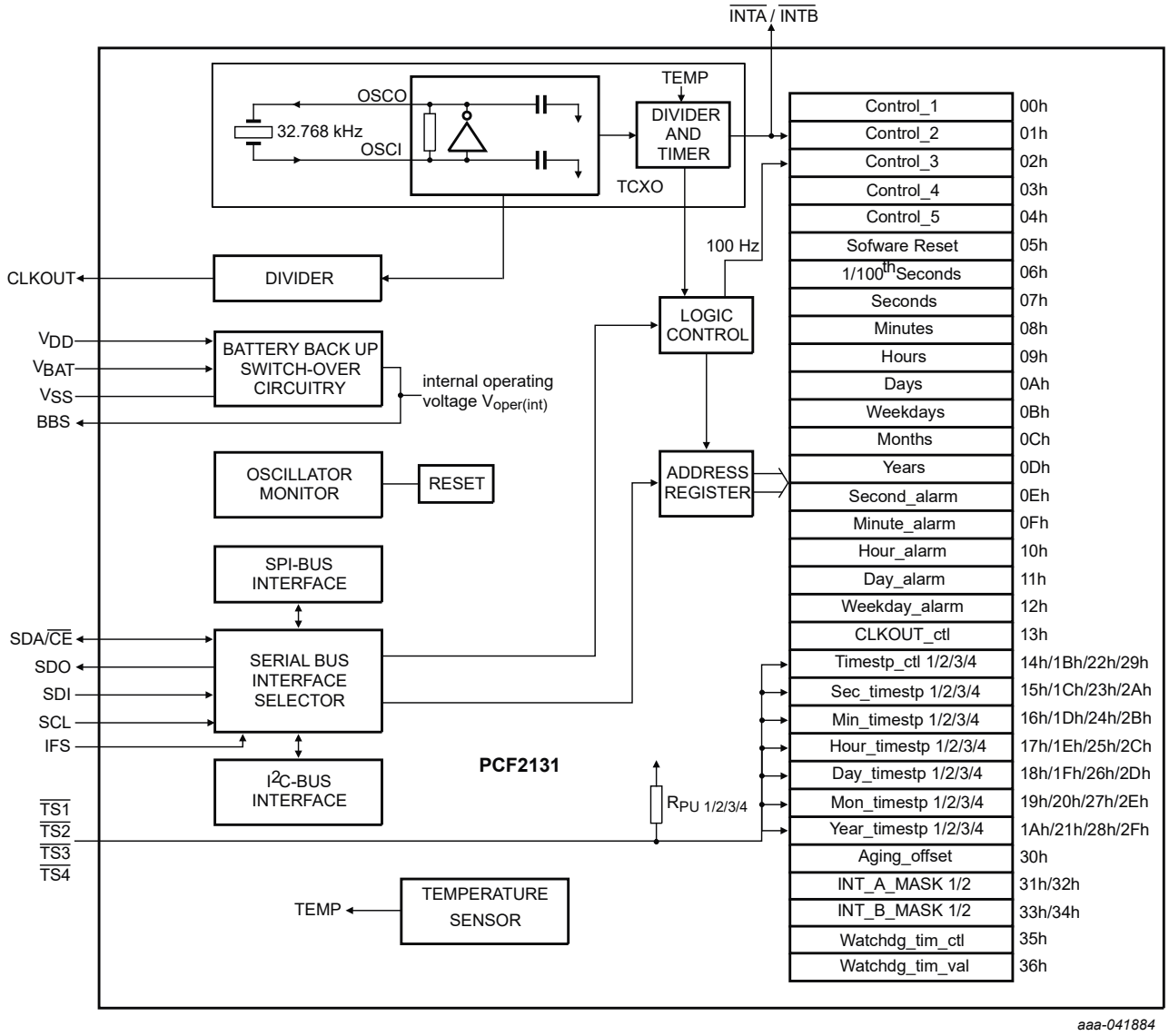


Figure 1. Block diagram of PCF2131

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6 Pinning information

This section outlines the pin configuration and provides a detailed description of the PCF2131.

6.1 Pinning

Figure 2 shows the pin configuration of PCF2131.

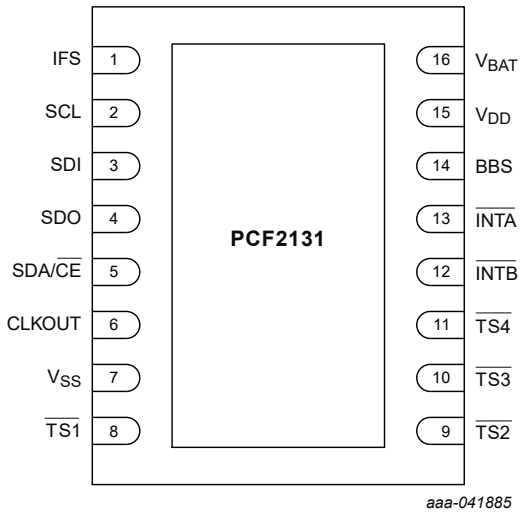


Figure 2. Pin configuration for PCF2131 (transparent top view)

6.2 Pin description

Table 3 provides detailed description of various pins on PCF2131.

Table 3. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
SCL	2	Combined serial clock input for both I^2C-bus and SPI-bus
SDI	3	Serial data input for SPI-bus Connect to pin V_{SS} if I^2C-bus is selected
SDO	4	Serial data output for SPI-bus, push-pull Leave open or connect to pin V_{SS} if I^2C-bus is selected
SDA/$\overline{CE}$	5	Combined serial data input and output for the I^2C-bus and chip enable input (active LOW) for the SPI-bus
IFS	1	Interface selector input Connect to pin V_{SS} to select the SPI-bus Connect to pin V_{DD} to select the I^2C-bus
$\overline{TS1}$, $\overline{TS2}$, $\overline{TS3}$, and $\overline{TS4}$	8,9,10,11	Timestamp input (active LOW) with 500 kΩ internal pullup resistor (R_{PU})
CLKOUT	6	Clock output (push-pull)
V_{SS}	7	Ground supply voltage
$\overline{INTB}$	12	Interrupt B output (open-drain; active LOW)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 3. Pin description...*continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
$\overline{INTA}$	13	Interrupt A output (open-drain; active LOW)
BBS	14	Output voltage (battery backed)
V_{BAT}	16	Battery supply voltage (backup) Connect to V_{SS} if battery switch-over is not used
V_{DD}	15	Supply voltage
Exposed Pad		Leave floating

7 Functional description

The PCF2131 is an RTC and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package.

Address and data are transferred by a selectable 400 kHz Fast-mode I^2C-bus or a 4-line SPI-bus with separate data input and output (see Section 7.15). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2131 has a backup battery input pin and backup battery switch-over circuit, which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see Section 7.5.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 7.5.2). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This condition ensures the integrity of the data during periods of battery backup.

7.1 Register overview

The PCF2131 contains an auto-incrementing address register: the built-in address register increments automatically after each read or write of a data byte up to the register 36h. After register 36h, the auto-incrementing wraps around to address 00h (see Figure 3).

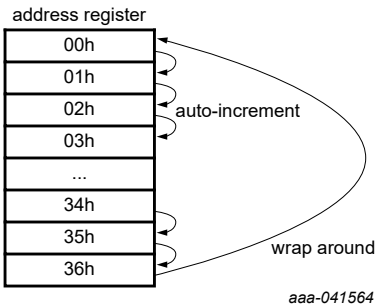


Figure 3. Handling address registers

- The first five registers (memory address 00h, 01h, 02h, 03h, and 04h) are used as control registers (see Section 7.2).
- The register at address 05h is for software reset.
- The memory addresses 06h through to 0Dh are used as counters for the clock function (1/100 seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 7.9).

- The registers at addresses 0Eh through 12h define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 7.10).
- The register at address 13h defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 32 minutes (default) down to every 4 minutes (see Table 17). CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 18).
- The registers at addresses 14h to 2Fh are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see Section 7.12).
- The register at address 30h is used for the correction of the crystal aging effect (see Section 7.4.1).
- The registers at addresses 31h to 34h are used for interrupt configuration.
- The registers at addresses 35h and 36h are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 20 ms to greater than 4 hours (see Table 59). An interrupt is generated when the watchdog times out.
- The registers 100th Seconds, Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bitwise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen, all registers hold their state during SPI or I^2C transactions. The timestamp registers are updated once the bus transaction completes. This functionality prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 7.9.9).

Table 4. Register overview

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
Control registers											
00h	Control_1	T	TC_DIS	STOP	100TH_S_DIS	T	12_24	MI	SI	0000 1000	Table 5
01h	Control_2	MSF	WDTF	T	AF	T	T	AIE	T	0000 0000	Table 7
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	1110 0000	Table 9
03h	Control_4	TSF1	TSF2	TSF3	TSF4	T	T	T	T	0000 0000	Table 11
04h	Control_5	TSIE1	TSIE2	TSIE3	TSIE4	T	T	T	T	0000 0000	Table 13
Software Reset											
05h	SR_Reset	CPR	0	1	0	SR	1	0	CTS	0010 0100	Table 24
Time and date registers											
06h	100th_Seconds	100TH_SECONDS(0 to 99)								0000 0000	Table 25
07h	Seconds	OSF	SECONDS (0 to 59)							1000 0000	Table 28
08h	Minutes	-	MINUTES (0 to 59)							0000 0000	Table 31
09h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode					0000 0000	Table 33
				HOURS (0 to 23) in 24-hour mode						0000 0000	
0Ah	Days	-	-	DAYS (1 to 31)						0000 0001	Table 35
0Bh	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			0000 0001	Table 37
0Ch	Months	-	-	-	MONTHS (1 to 12)					0000 0001	Table 40
0Dh	Years	YEARS (0 to 99)								0000 0001	Table 43
Alarm registers											
0Eh	Second_alarm	AE_S	SECOND_ALARM (0 to 59)							1000 0000	Table 45
0Fh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)							1000 0000	Table 47
10h	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode					1000 0000	Table 49
				HOUR_ALARM (0 to 23) in 24-hour mode						1000 0000	
11h	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)						1000 0000	Table 51
12h	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1000 0000	Table 53

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 4. Register overview...*continued*

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
CLKOUT control register											
13h	CLKOUT_ctl	TCR[1:0]		OTPR	-	-	COF[2:0]			00X0 0000	Table 15
Timestamp1 registers											
14h	Timestp_ctl1	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 64
15h	Sec_timestp1	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 66
16h	Min_timestp1	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 68
17h	Hour_timestp1	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 70
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
18h	Day_timestp1	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 72
19h	Mon_timestp1	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 74
1Ah	Year_timestp1	YEAR_TIMESTP (0 to 99)								0000 0000	Table 76
Timestamp2 registers											
1Bh	Timestp_ctl2	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 64
1Ch	Sec_timestp2	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 66
1Dh	Min_timestp2	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 68
1Eh	Hour_timestp2	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 70
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
1Fh	Day_timestp2	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 72
20h	Mon_timestp2	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 74
21h	Year_timestp2	YEAR_TIMESTP (0 to 99)								0000 0000	Table 76
Timestamp3 registers											
22h	Timestp_ctl3	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 64
23h	Sec_timestp3	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 66
24h	Min_timestp3	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 68
25h	Hour_timestp3	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 70
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
26h	Day_timestp3	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 72
27h	Mon_timestp3	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 74
28h	Year_timestp3	YEAR_TIMESTP (0 to 99)								0000 0000	Table 76
Timestamp4 registers											
29h	Timestp_ctl4	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]					0000 0000	Table 64
2Ah	Sec_timestp4	-	SECOND_TIMESTP (0 to 59)							0000 0000	Table 66
2Bh	Min_timestp4	-	MINUTE_TIMESTP (0 to 59)							0000 0000	Table 68
2Ch	Hour_timestp4	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					0000 0000	Table 70
				HOUR_TIMESTP (0 to 23) in 24-hour mode						0000 0000	
2Dh	Day_timestp4	-	-	DAY_TIMESTP (1 to 31)						0000 0000	Table 72
2Eh	Mon_timestp4	-	-	-	MONTH_TIMESTP (1 to 12)					0000 0000	Table 74
2Fh	Year_timestp4	YEAR_TIMESTP (0 to 99)								0000 0000	Table 76
Aging offset register											
30h	Aging_offset	-	-	-	-	AO[3:0]				0000 1000	Table 19
Interrupt mask registers											
31h	INT_A_MASK1	-	-	MIA	SIA	WD_CDA	AIEA	BIEA	BLIEA	0011 1111	Table 80
32h	INT_A_MASK2	-	-	-	-	TSIE1A	TSIE2A	TSIE3A	TSIE4A	0000 1111	Table 80
33h	INT_B_MASK1	-	-	MiB	SIB	WD_CDB	AIEB	BIEB	BLIEB	0011 1111	Table 82
34h	INT_B_MASK2	-	-	-	-	TSIE1B	TSIE2B	TSIE3B	TSIE4B	0000 1111	Table 82
Watchdog registers											
35h	Watchdg_tim_ctl	WD_CD	T	TI_TP	-	-	-	TF[1:0]		0000 0011	Table 55
36h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								0000 0000	Table 57

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.2 Control registers

The first five registers of the PCF2131, with the addresses 00h, 01h, 02h, 03h, and 04h, are used as control registers.

7.2.1 Register Control_1

Table 5 and Table 6 show the bit allocation and bit description of the Control_1 register, respectively.

Table 5. Control_1 - control and status register 1 (address 00h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	TC_DIS	STOP	100TH_S_DIS	T	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	T	0	Unused	-
6	TC_DIS	0	Temperature compensation enabled	Section 7.3.1
		1	Temperature compensation disabled	
5	STOP	0	RTC source clock runs	Section 7.14
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0 CLKOUT output frequencies are still available	
4	100TH_S_DIS	0	100th seconds counter enabled	-
		1	100th seconds counter disabled, register 06h reset to 00h.	-
3	T	1	Unused	-
2	12_24	0	24-hour mode selected	Table 34, Table 50, Table 71
		1	12-hour mode selected	
1	MI	0	Minute interrupt disabled	Section 7.13.1
		1	Minute interrupt enabled	
0	SI	0	Second interrupt disabled	
		1	Second interrupt enabled	

7.2.2 Register Control_2

Table 7 and Table 8 show the bit allocation and bit description of the Control_2 register, respectively.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 7. Control_2 - control and status register 2 (address 01h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	T	AF	T	T	AIE	T
Reset value	0	0	0	0	0	0	0	0

Table 8. Control_2 - control and status register 2 (address 01h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	MSF	0	No minute or second interrupt generated	Section 7.13
		1	Flag set when minute or second interrupt generated; The flag must be cleared to clear interrupt	
6	WDTF	0	No watchdog timer interrupt generated	Section 7.13.3
		1	Flag set when watchdog timer interrupt generated; The flag must be cleared to clear interrupt	
5	T	0	Unused	-
4	AF	0	No alarm interrupts were triggered	Section 7.10.6
		1	Flag set when alarm triggered; The flag must be cleared to clear interrupt	
3:2	T	0	Unused	-
1	AIE	0	No interrupt generated from the alarm flag	Section 7.13.4
		1	Interrupt generated when alarm flag set	
0	T	0	Unused	-

7.2.3 Register Control_3

Table 9 and Table 10 show the bit allocation and bit description of the Control_3 register, respectively.

Table 9. Control_3 - control and status register 3 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
Reset value	1	1	1	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 10. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	See Table 22	Control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 7.5
4	BTSE	0	No timestamp when battery switch-over occurs	Section 7.12.4
		1	Timestamped when battery switch-over occurs	
3	BF	0	No battery switch-over interrupt occurred	Section 7.5.1 and Section 7.12.4
		1	Flag set when battery switch-over occurs; The flag must be cleared to clear interrupt	
2	BLF	0	Battery status ok; No battery low interrupt generated	Section 7.5.2
		1	Battery status low flag cannot be cleared by command. The flag is automatically cleared when the battery is replaced.	
1	BIE	0	No interrupt generated from the battery flag (BF)	Section 7.13.6
		1	Interrupt generated when BF is set	
0	BLIE	0	No interrupt generated from battery low flag (BLF)	Section 7.13.7
		1	Interrupt generated when BLF is set	

7.2.4 Register Control_4

Table 11 and Table 12 show the bit allocation and bit description of the Control_4 register, respectively.

Table 11. Control_4 - control and status register 4 (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSF1	TSF2	TSF3	TSF4	T	T	T	T
Reset value	0	0	0	0	0	0	0	0

Table 12. Control_4 - control and status register 4 (address 03h) bit description

Bit	Symbol	Value	Description	Reference
7	TSF1	0	No timestamp interrupt generated for pin $\overline{TS1}$	Section 7.12.1
		1	Flag set when $\overline{TS1}$ input is driven to ground: The flag must be cleared to clear interrupt	
6	TSF2	0	No timestamp interrupt generated when pin $\overline{TS2}$	Section 7.12.1
		1	Flag set when $\overline{TS2}$ input is driven to ground; The flag must be cleared to clear interrupt	
5	TSF3	0	No timestamp interrupt generated for pin $\overline{TS3}$	Section 7.12.1
		1	Flag set when $\overline{TS3}$ input is driven to ground; The flag must be cleared to clear interrupt	
4	TSF4	0	No timestamp interrupt generated when pin $\overline{TS4}$	Section 7.12.1
		1	Flag set when $\overline{TS4}$ input is driven to ground;	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 12. Control_4 - control and status register 4 (address 03h) bit description...*continued*

Bit	Symbol	Value	Description	Reference
			The flag must be cleared to clear interrupt	
3	T	0	Unused	-
2	T	0	Unused	-
1	T	0	Unused	-
0	T	0	Unused	-

7.2.5 Register Control_5

Table 13 and Table 14 show the bit allocation and bit description of the Control_5 register, respectively.

Table 13. Control_5 - control and status register 5 (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSIE1	TSIE2	TSIE3	TSIE4	T	T	T	T
Reset value	0	0	0	0	0	0	0	0

Table 14. Control_5 - control and status register 5 (address 04h) bit description

Bit	Symbol	Value	Description	Reference
7	TSIE1	0	No interrupt generated from timestamp flag of $\overline{TS1}$	Section 7.13.5
		1	Interrupt generated when timestamp flag set of $\overline{TS1}$	
6	TSIE2	0	No interrupt generated from timestamp flag of $\overline{TS2}$	Section 7.13.5
		1	Interrupt generated when timestamp flag set of $\overline{TS2}$	
5	TSIE3	0	No interrupt generated from timestamp flag of $\overline{TS3}$	Section 7.13.5
		1	Interrupt generated when timestamp flag set of $\overline{TS3}$	
4	TSIE4	0	No interrupt generated from timestamp flag of $\overline{TS4}$	Section 7.13.5
		1	Interrupt generated when timestamp flag set of $\overline{TS4}$	
3 to 0	T	0	Unused	-

7.3 Register CLKOUT_ctl

Table 15 and Table 16 show the bit allocation and bit description of the CLKOUT_ctl register, respectively.

Table 15. CLKOUT_ctl - CLKOUT control register (address 13h) bit allocation

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[1:0]		OTPR	T	T	COF[2:0]		

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 15. CLKOUT_ctl - CLKOUT control register (address 13h) bit allocation...*continued*

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	X	0	0	0	0	0

Table 16. CLKOUT_ctl - CLKOUT control register (address 13h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7 to 6	TCR[1:0]	See Table 17	Temperature measurement period	
5	OTPR	0	No OTP refresh	Section 7.3.2
		1	OTP refresh performed	
4	T	0	Unused [1]	
3	T	0	Unused	
2 to 0	COF[2:0]	See Table 18	CLKOUT frequency selection	Section 7.3.3

[1] Programming this bit to 1 may lead to a decrease of timing accuracy.

7.3.1 Temperature compensated RTC

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCF2131, the frequency deviation caused by temperature variation is corrected by adjusting the RTC frequency divider with digital method.

The load capacitance is trimmed to the required value at 25 °C to compensate the frequency deviation over process variation.

The frequency accuracy at 25 °C can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32.768 kHz (default value) can lead to inaccurate measurements. Accurate frequency measurement occurs when f_{CLKOUT} = 16.384 kHz or lower is selected (see Table 18).

The temperature compensated frequency input for the RTC cannot be observed at the CLKOUT pin but can be evaluated by following these steps.

- Set the Second Interrupt and the bit SI in register Control_1.
- Set bit TI_TP in register Watchdg_tim_ctl for a pulsed interrupt signal.
- Clear bit SIA in register INTA_MASK_1 to direct the Second Interrupt to pin INTA for a 1 Hz pulse output.

The RTC temperature compensation works by adding or deleting pulses at the 32.768 kHz level. These correction pulses are spaced evenly over a sufficiently long period of time to reach the required resolution and accuracy. Every second corrections with a resolution of about 30.5 ppm (1/32768) can be generated by the temperature compensation engine. If for instance a 10 ppm correction is called for, the correction pulses are generated approximately once every 3 seconds, for a 50 ppm correction every 0.6 s and so on.

The 1 Hz interrupt output signal can be measured with a counter and by selecting an appropriate gating time the measurement resolution can be set to the desired level. A gating time of 100 s for instance determines the averaged 1 second period with a resolution of 0.3 ppm.

The feature of temperature compensation can be turned off for ultra low power consumption by first performing a Software Reset (SR) followed by setting TC_DIS to ‘1’ within 5 seconds.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.3.1.1 Temperature measurement

The PCF2131 has a temperature sensor circuit used to perform temperature compensation of the clock input to the RTC. The temperature is measured immediately after power on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl. During the first approximately 60 s after startup, the compensation is inactive, after this period the temperature compensation is active.

Table 17. Temperature measurement period

TCR[1:0]	Note	Temperature measurement period
00	[1]	32 min
01		16 min
10		8 min
11		4 min

[1] Default value.

7.3.2 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

When read OTPR bit, its state is:

"0" until the OTP read state machine completes copying of the eFuse data into the shadow registers. It could be due to a POR event or to writing a 0 > 1 to the OTPR register bit.

"1" when the OTP read state machine completes copying to the shadow registers from the eFuse instances. During normal operation OTPR must be kept at 1 to prevent higher power usage.

The OTP logic is not affected by the Software Reset. The OTPR functionality is only reset by the initial digital POR.

During OTP refresh, V_{DD} must be above 1.8 V. The rising speed from 0 V to 1.8 V must be faster than 2 V/100 ms. After OTP refresh has finished, PCF2131 can operate with V_{DD} as low as 1.2 V.

7.3.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator at 25 °C to determine aging offset. The CLKOUT output is not temperature compensated to prevent jitter due to the digital compensation method.

CLKOUT is a push-pull output and is enabled at power on. When disabled, the output is high-impedance.

Table 18. CLKOUT frequency selection

COF[2:0]	Note	CLKOUT frequency (Hz)	Typical duty cycle [1]
000	[2]	32 768	60 : 40 to 40 : 60
001		16 384	50 : 50
010		8 192	50 : 50
011		4 096	50 : 50

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 18. CLKOUT frequency selection*...continued*

COF[2:0]	Note	CLKOUT frequency (Hz)	Typical duty cycle [1]
100		2 048	50 : 50
101		1 024	50 : 50
110		1	50 : 50
111		CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time: % LOW-level time.
[2] Default value.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies are 50 : 50.

7.4 Register Aging_offset

Table 19 and Table 20 show the bit allocation and bit description of the Aging_offset register, respectively.

Table 19. Aging_offset - crystal aging offset register (address 30h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	T	AO[3:0]			
Reset value	0	0	0	0	1	0	0	0

Table 20. Aging_offset - crystal aging offset register (address 30h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	T	0000	Unused
3 to 0	AO[3:0]	See Table 21	Aging offset value

7.4.1 Crystal aging correction

The PCF2131 has an offset register Aging_offset to correct the crystal aging effects. For further information, refer to ref.[1] in references.

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit, which allows correcting the aging effect.

The aging offset bits allow a frequency correction of typically 2 ppm per AO[3:0] value, from -14 ppm to +16 ppm.

Table 21. Frequency correction at 25 °C, typical

AO[3:0]			ppm
Decimal	Binary	Note	
0	0000		+16
1	0001		+14
2	0010		+12

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 21. Frequency correction at 25 °C, typical*...continued*

AO[3:0]			ppm
Decimal	Binary	Note	
3	0011		+10
4	0100		+8
5	0101		+6
6	0110		+4
7	0111		+2
8	1000	[1]	0
9	1001		-2
10	1010		-4
11	1011		-6
12	1100		-8
13	1101		-10
14	1110		-12
15	1111		-14

[1] Default value.

7.5 Power management functions

The PCF2131 has two power supplies:

V_{DD} - the main power supply

V_{BAT} - the battery backup supply

Internally, PCF2131 operates with the internal operating voltage $V_{oper(int)}$, which is also available as V_{BBS} on the battery backed output voltage pin, BBS. Depending on the condition of the main power supply and the selected power management function, $V_{oper(int)}$ is either on the potential of V_{DD} or V_{BAT}.

Two power management functions are implemented:

Battery switch-over function - monitors the main power supply V_{DD} and switching to V_{BAT} in case a power fail condition is detected (see Section 7.5.1).

Battery low detection function - monitors the status of the battery, V_{BAT} (see Section 7.5.2).

The power management functions are controlled by the control bits PWRMNG[2:0] (see Table 22) in register Control_3 (see Table 10):

Table 22. Power management control bit description

PWRMNG[2:0]	Note	Function
000		Battery switch-over function is enabled in standard mode; Battery low detection function is enabled
001,010		Battery switch-over function is enabled in standard mode; Battery low detection function is disabled
011		Battery switch-over function is enabled in direct switching mode; Battery low detection function is enabled

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 22. Power management control bit description...*continued*

PWRMNG[2:0]	Note	Function
100,101		Battery switch-over function is enabled in direct switching mode; Battery low detection function is disabled
110,111	[1] [2]	Battery switch-over function is disabled, only one power supply (V_{DD}); Battery low detection function is disabled

[1] Default value.
[2] When the battery switch-over function is disabled, the device works only with the power supply V_{DD}. V_{BAT} must be put to ground and the battery low detection function is disabled.

7.5.1 Battery switch-over function

PCF2131 has a backup battery switch-over circuit, which monitors the main power supply V_{DD}. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

Standard mode - the power failure condition happens when:

$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. The typical value is 2.5 V. The battery switch-over in standard mode works only for $V_{DD} > 2.5$ V. Applying back-up battery voltage to V_{BAT} without applying V_{DD} supply does not power on the device; only when V_{DD} main power is supplied to the device starts operating.

Direct switching mode - the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$.

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set to logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 7.13.6).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp 4 registers store the time and date when the battery switch occurred (see Section 7.12.4).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

The interface and CLKOUT output are disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device.
- Interface outputs are high-impedance.

For further information about I^2C-bus communication and battery backup operation, see Section 7.15.3.

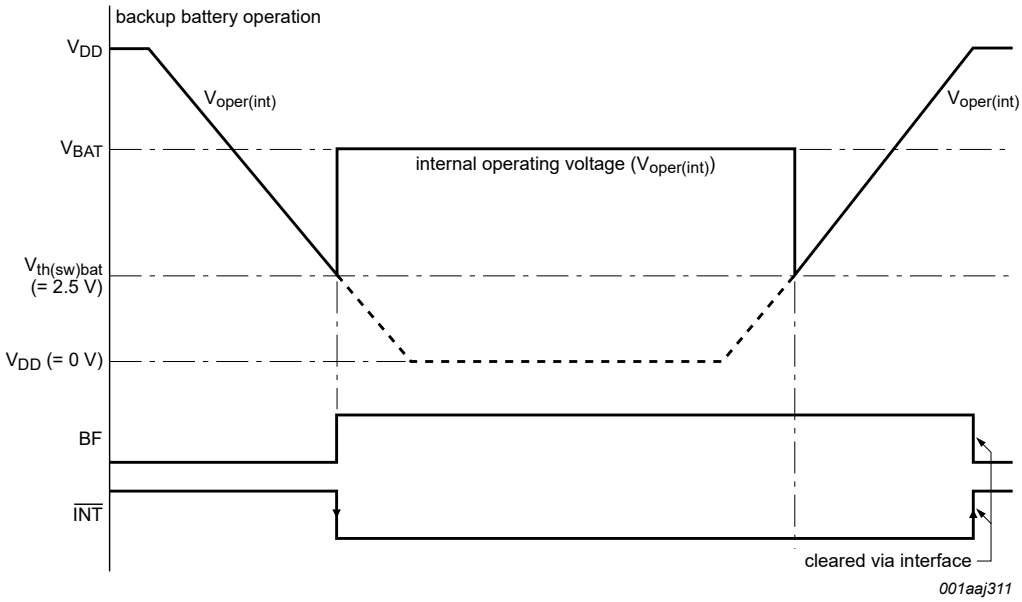
7.5.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{BAT} potential.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



$V_{th(sw)bat}$ is the battery switch threshold voltage. The typical value is 2.5 V. In standard mode, the battery switch-over works only for V_{DD} > 2.5 V.

V_{DD} can be lower than V_{BAT} (for example V_{DD} = 3 V, V_{BAT} = 4.1 V).

Figure 4. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

7.5.1.2 Direct switching mode

If V_{DD} > V_{BAT}: $V_{oper(int)}$ is at V_{DD} potential.

If V_{DD} < V_{BAT}: $V_{oper(int)}$ is at V_{BAT} potential.

The direct switching mode is useful in systems where V_{DD} is always higher than V_{BAT}. This mode is not recommended if the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3 V, V_{BAT} ≥ 3.0 V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

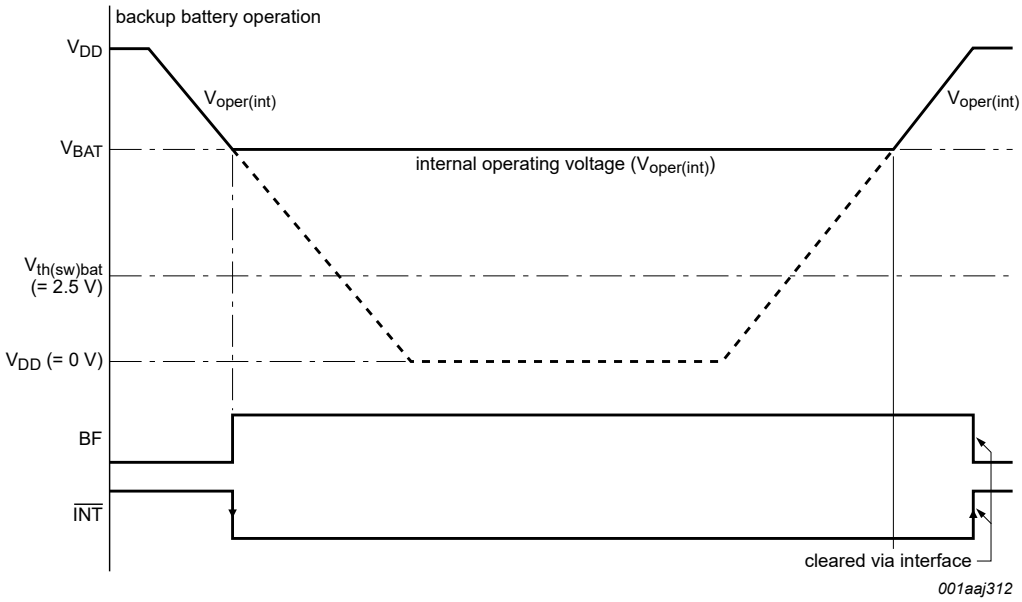


Figure 5. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

7.5.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- $V_{oper(int)}$ is at V_{DD} potential
- The Battery Flag (BF) is always logic 0

7.5.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 6.

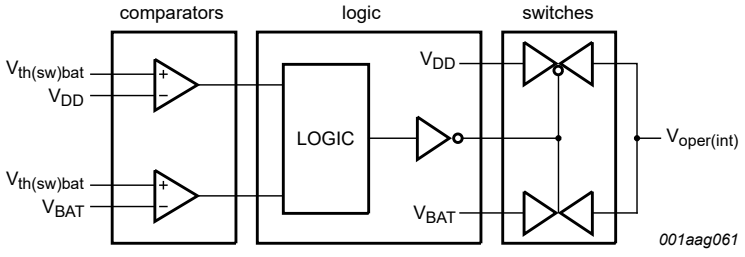


Figure 6. Battery switch-over circuit, simplified block diagram

$V_{oper(int)}$ is at V_{DD} or V_{BAT} potential.

Remark: It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

7.5.2 Battery low detection function

The PCF2131 has a battery low detection circuit, which monitors the status of the battery V_{BAT}.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typical 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent the supply voltage from dropping below V_{low} (typical 1.2 V) and with that the data integrity gets lost. (For further information about V_{low}, see Section 7.6.)

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 7):

1. The battery low flag BLF is set to logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 7.13.7).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is automatically cleared by the battery low detection circuit when the battery is replaced or when the voltage rises again above the threshold value. This condition could happen if a super capacitor is used as a backup source and the main power is applied again.

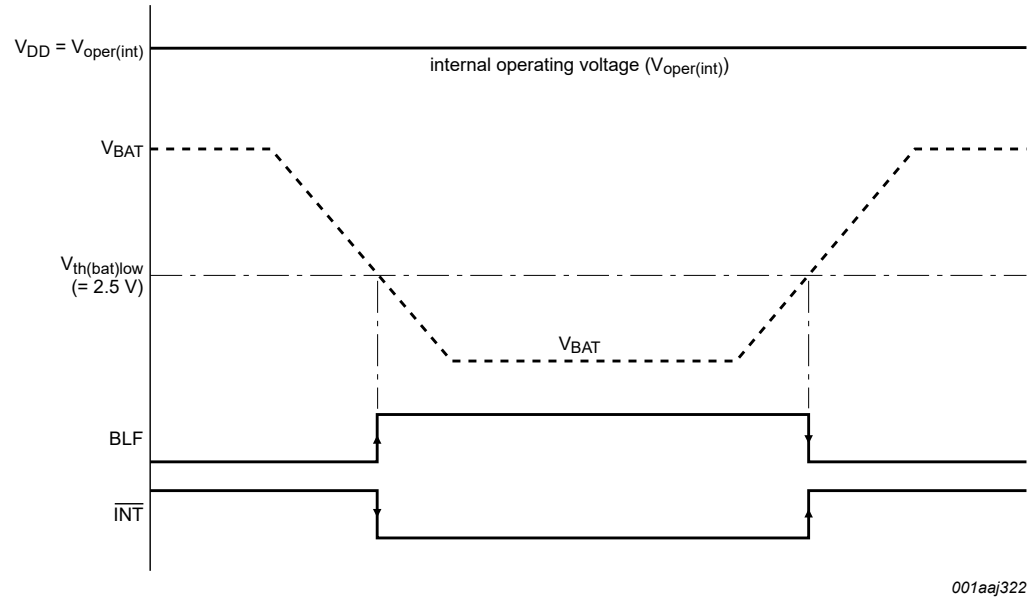


Figure 7. Battery low detection behavior with bit BLIE set logic 1 (enabled)

7.5.3 Battery backup supply

The V_{BBS} voltage on output pin BBS is at the same potential as the internal operating voltage $V_{oper(int)}$, depending on the selected battery switch-over function mode:

Table 23. Output pin BBS

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and V_{BBS}
Standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
Direct switching	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
Disabled	Only V_{DD} available, V_{BAT} must be put to the ground	V_{DD}

All information provided in this document is subject to legal disclaimers.

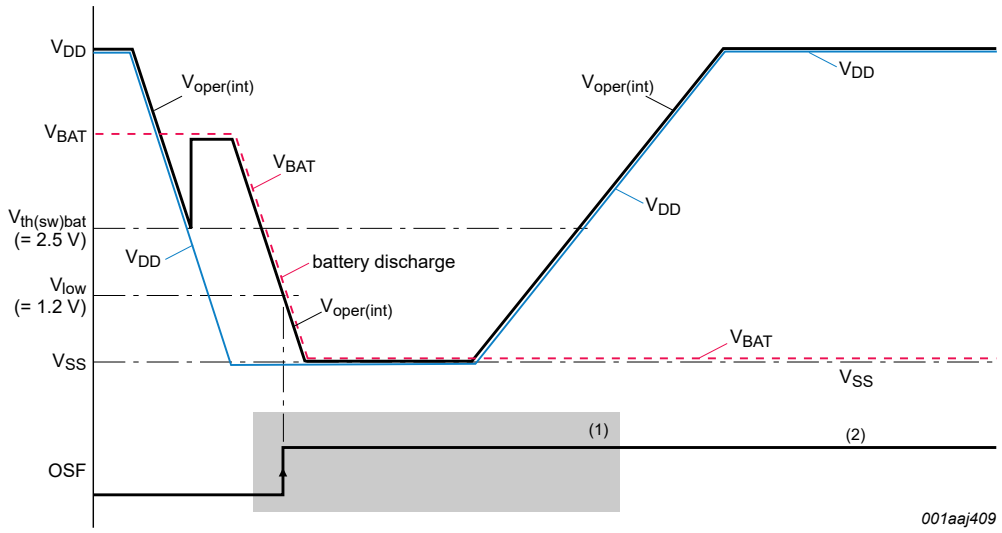
© 2026 NXP B.V. All rights reserved.

The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see ref.[1]).

7.6 Oscillator stop detection function

The PCF2131 has an on-chip oscillator detection circuit, which indicates the status of the oscillation by monitoring the supply of oscillator: whenever the supply is out of the expected range, a reset occurs and the Oscillator Stop Flag (OSF, in register Seconds) is set logic 1.

- **Power on:**
  1. The oscillator is not running and the chip is in reset (OSF is logic 1).
  2. When the oscillator starts running and the supply is OK after power on, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
- **Power supply failure:**
  1. When the power supply of the chip drops below a certain value (V_{low}), typically 1.2 V, the oscillator supply also fails and a reset occurs.
  2. When the power supply returns to normal operation, the oscillator supply is OK again, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
  4. When OSF flag is cleared, an OTP refresh must be performed (see Section 7.3.2).



1. Theoretical state of the signals since there is no power.
2. The Oscillator Stop Flag (OSF), set logic 1, indicates that the oscillation has stopped and a reset has occurred since the flag was last cleared (OSF set logic 0). In this case, the integrity of the clock information is not guaranteed. The OSF flag is cleared by command.

Figure 8. Power failure event due to battery discharge: reset occurs

7.7 Power-on Reset (POR) function

The PCF2131 has a POR function implemented.

7.7.1 Power-on Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator stops during the time between power on and stable crystal resonance (see Figure 9). This time can be in the range of 200 ms to 2 s depending on

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see Section 7.3.2) must ideally be executed as the first instruction after startup and also after a reset due to an oscillator stop.

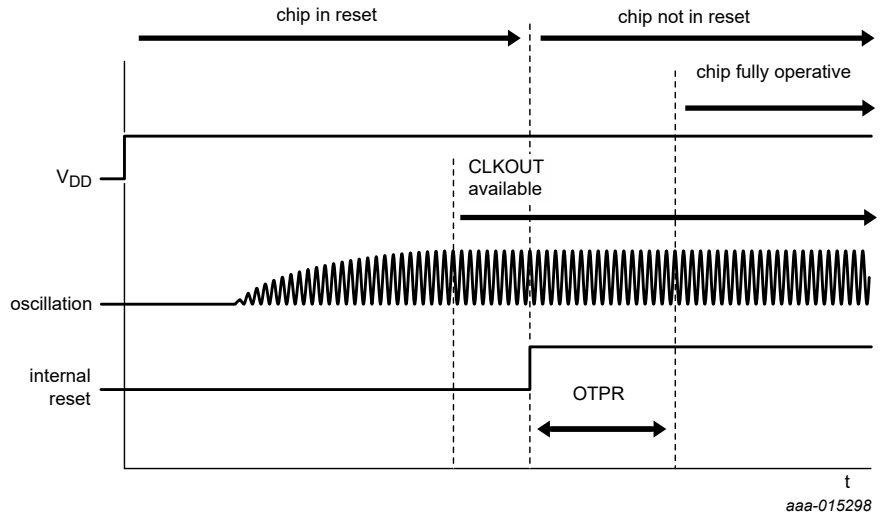


Figure 9. Dependency between POR and oscillator

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (V_{DD})
- Temperature compensation enabled
- 100th second enabled
- Time 00:00:00.00
- Date 2001.01.01
- Weekday Monday

The register values after power on are shown in Table 4.

7.8 Software reset register

Table 24 provides the software reset register bit description.

Table 24. Reset - software reset control (address 05h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CPR	0	1	0	SR	1	0	CTS
Section	Section 7.8.2				Section 7.8.1			Section 7.8.3

To

- Trigger a Software Reset (SR), 0010 1100 (2Ch) must be sent to register Reset (address 05h). A software reset also triggers CPR and CTS.
- Clear Prescaler (CPR), 1010 0100 (A4h) must be sent to register Reset (address 05h).
- Clear Timestamp (CTS), 0010 0101 (25h) must be sent to register Reset (address 05h).

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

It is possible to combine CPR and CTS by sending 1010 0101 (A5h).

Read of the SR_RESET register returns a fixed pattern of 00100100;

Remark: Any other value sent to this register is ignored.

7.8.1 Software Reset (SR)

A reset is automatically generated at power on as power-on reset as described in Section 7.7. A reset can also be initiated with the software reset command.

After software reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- OTP not reloaded, OTPR unchanged
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (V_{DD})
- Temperature compensation enabled
- 100th second enabled
- Time 00:00:00.00
- Date 2001.01.01
- Weekday Monday

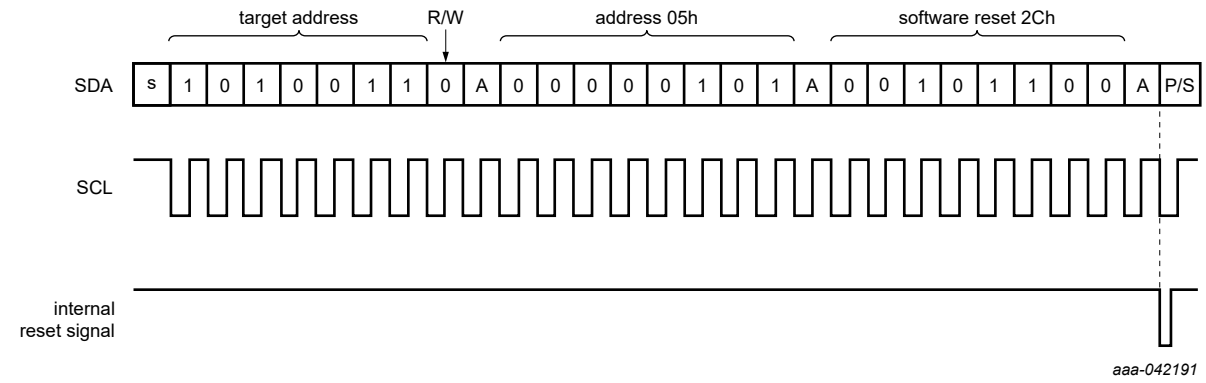


Figure 10. Software reset command

7.8.2 Clear Prescaler (CPR)

To set the time for RTC mode, the clear prescaler instruction is needed.

Before sending this instruction, it is mandatory to first set *stop* by the stop bit.

See the STOP definition for an explanation on using this instruction.

7.8.3 Clear timestamp (CTS)

The timestamp registers (address 14h to 2Fh) can be set to all 0 with this instruction.

7.9 Time and date function

Most of these registers are coded in the BCD format.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.9.1 Register 100th Seconds

This section details the 100th Seconds register, including its bit allocation, individual bit definitions, and the representation of 100th Seconds in BCD format.

Table 25. 100th Seconds - 100th seconds (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	100TH SECONDS (0 to 99)							
Reset value	0	0	0	0	0	0	0	0

Table 26. 100th Seconds - 100th seconds register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	100TH SECONDS	0 to 9	Ten's place	Actual seconds coded in BCD format
3 to 0		0 to 9	Unit place	

Table 27. 100th Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

7.9.2 Register Seconds

This section details the Seconds register, including its bit allocation, individual bit definitions, and the representation of Seconds in BCD format.

Table 28. Seconds - seconds and clock integrity register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 29. Seconds - seconds and clock integrity register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	Clock integrity is guaranteed
		1	-	Clock integrity is not guaranteed: The oscillator has stopped and chip reset has occurred since the flag was last cleared
6 to 4	SECONDS	0 to 5	Ten's place	Actual seconds coded in BCD format
3 to 0		0 to 9	Unit place	

Table 30. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

7.9.3 Register Minutes

This section details the Minutes register, including its bit allocation and individual bit definitions.

Table 31. Minutes - minutes register (address 08h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	MINUTES (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 32. Minutes - minutes register (address 08h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	Unused
6 to 4	MINUTES	0 to 5	Ten's place	Actual minutes coded in BCD format
3 to 0		0 to 9	Unit place	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.9.4 Register Hours

This section details the Hours register, including its bit allocation and individual bit definitions.

Table 33. Hours - hours register (address 09h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOURS (1 to 12) in 12-hour mode				
			HOURS (0 0to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

Table 34. Hours - hours register (address 09h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
12-hour mode[1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM
4	HOURS	0 to 1	Ten's place	Actual hours coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOURS	0 to 2	Ten's place	Actual hours coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Bit 12_24 in register Control_1 sets the hour mode(see Table 6).

7.9.5 Register Days

This section details the Days register, including its bit allocation and individual bit definitions.

Table 35. Days - days register (address 0Ah) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAYS (1 to 31)					
Reset value	0	0	0	0	0	0	0	0

Table 36. Days - days register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
5 to 4	DAYS[1]	0 to 3	Ten's place	Actual day coded in BCD format

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 36. Days - days register (address 0Ah) bit description...*continued*

Bit	Symbol	Value	Place value	Description
3 to 0		0 to 9	Unit place	

[1] If the year counter contains a value, which is exactly divisible by 4, excluding the year 00, the RTC compensates for leap years by adding a 29th day to February. Note that the next year rolls over to 00 in 2100, and it is not a leap year.

7.9.6 Register Weekdays

This section details the Weekdays register, including its bit allocation, individual bit definitions, and Weekday assignments.

Table 37. Weekdays - weekdays register (address 0Bh) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	T	T	WEEKDAYS (0 to 6)		
Reset value	0	0	0	0	0	0	0	1

Table 38. Weekdays - weekdays register (address 0Bh) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 3	T	000	Unused
2 to 0	WEEKDAYS	0 to 6	Actual weekday value, see Table 39

Although the association of the weekdays counter to the actual weekday is arbitrary, the PCF2131 assumes that Sunday is 000 and Monday is 001 for determining the increment for calendar weeks.

Table 39. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] The definition can be reassigned by the user.

7.9.7 Register Months

This section details the Months register, including its bit allocation, individual bit definitions, and the representation of Months assignments in BCD format.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 40. Months - months register (address 0Ch) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTHS (1 to 12)				
Reset value	0	0	0	0	0	0	0	1

Table 41. Months - months register (address 0Ch) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	Unused
4	MONTHS	0 to 1	Ten's place	Actual month coded in BCD format, see Table 42
3 to 0		0 to 9	Unit place	

Table 42. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

7.9.8 Register Years

This section details the Years register, including its bit allocation and individual bit definitions.

Table 43. Years - years register (address 0Dh) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	YEARS (0 to 99)							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 43. Years - years register (address 0Dh) bit allocation...*continued*

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	1

Table 44. Years - years register (address 0Dh) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	Ten's place	Actual year coded in BCD format
3 to 0		0 to 9	Unit place	

7.9.9 Setting and reading the time

Figure 11 shows the data flow and data dependencies starting from the 100 Hz/1 Hz clock tick.

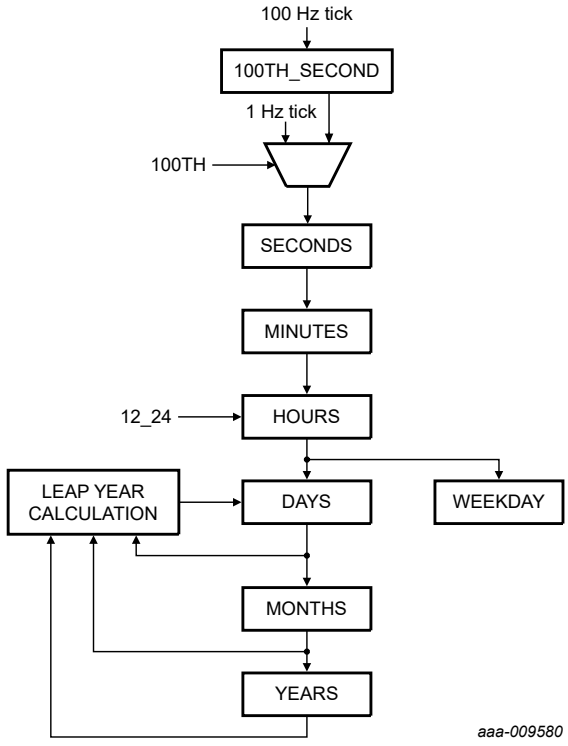


Figure 11. Data flow for the time function

Write access requires setting the stop bit. The flow for accurately setting the time in RTC mode is:

- Start an I2C access at register control_1
- Set the stop bit
- Set CPR (register SR_RESET, CPR is logic 1)
- Address counter rolls over to address 06h
- Set time (100th seconds, seconds to years)
- End I2C access

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Wait for an external time reference to indicate that time counting must start
- Start an I2C access at register control_1
- Clear stop bit (time starts counting from now)
- End I2C access

The first increment of the time circuits is between 0 s and 122 ms after STOP is released. See description for stop bit in Section 7.14.

During read operations, the time counting circuits (memory locations 06h through 0Dh) are blocked. This condition prevents the following:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read access is completed, the time circuit is released again. Any pending request to increment the time counters that occurred during the read access is serviced.

As a consequence of this method, it is important to make a read access in one go. That is, reading seconds through to years must be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

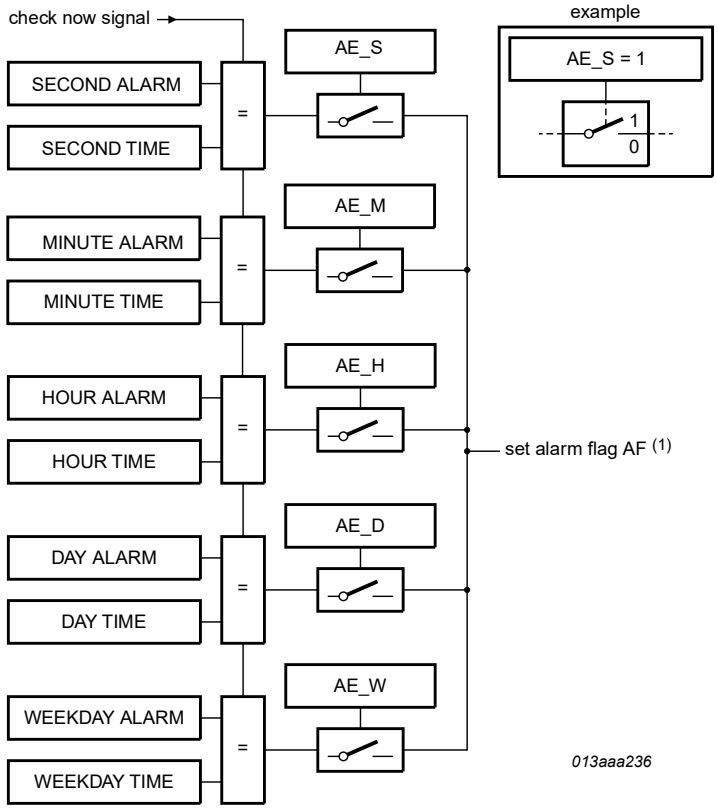
As an example, a roll-over can occur between reads, therefore giving the minutes from one moment and the hours from the next. Therefore, it is advised to read all time and date registers in one access.

7.10 Alarm function

When one or more of the alarm bit fields are loaded with a valid second, minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the actual second, minute, hour, day, and weekday (see Figure 12).

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



1. Only when all enabled alarm settings are matched.

Figure 12. Alarm function block diagram

The generation of interrupts from the alarm function is described in Section 7.13.4.

7.10.1 Register Second_alarm

This section details the Second_alarm register, including its bit allocation and individual bit definitions.

Table 45. Second_alarm - second alarm register (address 0Eh) bit allocation

Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_S	SECOND_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 46. Second_alarm - second alarm register (address 0Eh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_S	0	-	A second alarm is enabled
		1	-	The second alarm is disabled
6 to 4	SECOND_ALARM	0 to 5	Ten's place	Second alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.10.2 Register Minute_alarm

This section details the Minute_alarm register, including its bit allocation and individual bit definitions.

Table 47. Minute_alarm - minute alarm register (address 0Fh) bit allocation

Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_M	MINUTE_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 48. Minute_alarm - minute alarm register (address 0Fh) bit description

Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	Minute alarm is enabled
		1	-	Minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	Ten's place	Minute alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.3 Register Hour_alarm

This section details the Hour_alarm register, including its bit allocation and individual bit definitions.

Table 49. Hour_alarm - hour alarm register (address 10h) bit allocation

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_H	T	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			HOUR_ALARM (0 to 23) in 24-hour mode					
Reset value	1	0	0	0	0	0	0	0

Table 50. Hour_alarm - hour alarm register (address 10h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	Hour alarm is enabled
		1	-	Hour alarm is disabled
6	T	0	-	Unused
12-hour mode[1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 50. Hour_alarm - hour alarm register (address 10h) bit description...*continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
4	HOUR_ALARM	0 to 1	Ten's place	Hour alarm information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOUR_ALARM	0 to 2	Ten's place	Hour alarm information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Bit 12_24 in register Control_1 sets the hour mode.

7.10.4 Register Day_alarm

This section details the Day_alarm register, including its bit allocation and individual bit definitions.

Table 51. Day_alarm - day alarm register (address 11h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_D	T	DAY_ALARM (1 to 31)					
Reset value	1	0	0	0	0	0	0	0

Table 52. Day_alarm - day alarm register (address 11h) bit description

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	Day alarm is enabled
		1	-	Day alarm is disabled
6	T	0	-	Unused
5 to 4	DAY_ALARM	0 to 3	Ten's place	Day alarm information coded in BCD format
3 to 0		0 to 9	Unit place	

7.10.5 Register Weekday_alarm

This section details the Weekday_alarm register, including its bit allocation and individual bit definitions.

Table 53. Weekday_alarm - weekday alarm register (address 12h) bit allocation

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_W	T	T	T	T	WEEKDAY_ALARM (0 to 6)		
Reset value	1	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 54. Weekday_alarm - weekday alarm register (address 12h) bit description

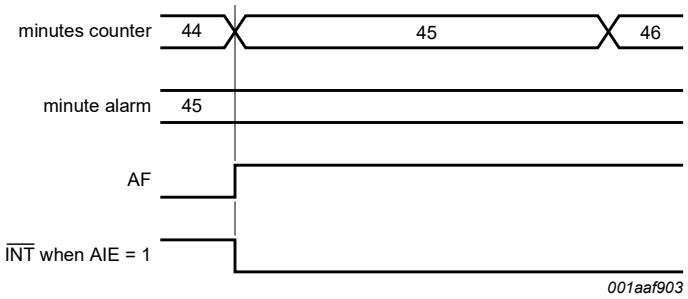
Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7	AE_W	0	Weekday alarm is enabled
		1	Weekday alarm is disabled
6 to 3	T	0	Unused
2 to 0	WEEKDAY_ALARM	0 to 6	Weekday alarm information

7.10.6 Alarm Flag (AF)

When all enabled comparisons match for the first time, the AF (register Control_2) is set. AF remains set until cleared by command. Once AF is cleared, it is set again only when the time increments to match the alarm condition once more. For clearing the flags, see Section 7.11.5.

Alarm registers, which have their alarm enable bit AE_x at logic 1 are ignored.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 13. Alarm flag timing diagram

7.11 Watchdog timer functions

The PCF2131 has a watchdog timer function. The timer can be switched on and off by using the control bit WD_CD in the register Watchdg_tim_ctl.

The watchdog timer has four selectable source clocks. It can, for example, be used to detect a microcontroller with interrupt and reset capability, which is out of control (see Section 7.11.3).

To control the timer function and timer output, the registers Control_2, Watchdg_tim_ctl, and Watchdg_tim_val are used.

7.11.1 Register Watchdg_tim_ctl

This section details the Watchdg_tim_ctl register, including its bit allocation and individual bit definitions.

Table 55. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	WD_CD	T	TI_TP	T	T	T	TF[1:0]	
Reset value	0	0	0	0	0	0	1	1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 56. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7	WD_CD	0	Watchdog timer interrupt disabled
		1	Watchdog timer interrupt enabled; The interrupt pin $\overline{\text{INTA/B}}$ is activated when timed out
6	T	0	Unused
5	TI_TP	0	The interrupt pin $\overline{\text{INTA/B}}$ is configured to generate a permanent active signal when MSF is set
		1	The interrupt pin $\overline{\text{INTA/B}}$ is configured to generate a pulsed signal when MSF flag is set (see Figure 15)
4 to 2	T	000	Unused
1 to 0	TF[1:0]		Timer source clock for watchdog timer
		00	64 Hz
		01	4 Hz
		10	$^1/_4$ Hz
		11	$^1/_{64}$ Hz

7.11.2 Register Watchdg_tim_val

This section details the Watchdg_tim_val register, including its bit allocation and individual bit definitions.

Table 57. Watchdg_tim_val - watchdog timer value register (address 36h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDG_TIM_VAL[7:0]							
Reset value	0	0	0	0	0	0	0	0

Table 58. Watchdg_tim_val - watchdog timer value register (address 36h) bit description

Bits labeled as X are undefined at power on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 0	WATCHDG_TIM_VAL[7:0]	00 to FF	Timer period in seconds: $TimerPeriod = \frac{(n-1)+/-0.5}{SourceClockFrequency}$ Where n is the timer value (n > 1) Write Only

Table 59. Programmable watchdog timer

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 2)	Units	Maximum timer period (n = 255)	Units
00	64	Hz	15.625	ms	3.984	s

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 59. Programmable watchdog timer...*continued*

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 2)	Units	Maximum timer period (n = 255)	Units
01	4	Hz	250	ms	63.744	s
10	$^1/_4$	Hz	4	s	1020	s
11	$^1/_{64}$	Hz	64	s	16320	s

7.11.3 Watchdog timer function

The watchdog timer interrupt function is enabled or disabled by the WD_CD bit of the register Watchdg_tim_ctl (see Table 56).

The 2-bit TF[1:0] in register Watchdg_tim_ctl determine one of the four source clock frequencies for the watchdog timer: 64 Hz, 4 Hz, $^1/_4$ Hz or $^1/_{64}$ Hz (see Table 59).

When the watchdog timer function is enabled, the 8-bit timer in register Watchdg_tim_val determines the watchdog timer period (see Table 59).

The watchdog timer counts down from the software programmed 8-bit binary value n in register Watchdg_tim_val. When the counter reaches 1, the watchdog timer flag WDTF (register Control_2) is set to logic 1, and an interrupt is generated. The period accuracy corresponds to n ± 0.5.

The register Watchdg_tim_val is write only and not readable after set.

The counter does not automatically reload.

When WD_CD is logic 1/0 (watchdog timer interrupt enabled/disabled) and the MCU loads a watchdog timer value n:

- The flag WDTF is reset
- $\overline{\text{INTA/B}}$ is cleared
- The watchdog timer starts again

Loading the counter with 0 or 1 will:

- Reset the flag WDTF
- Clear $\overline{\text{INTA/B}}$
- Stop the watchdog timer

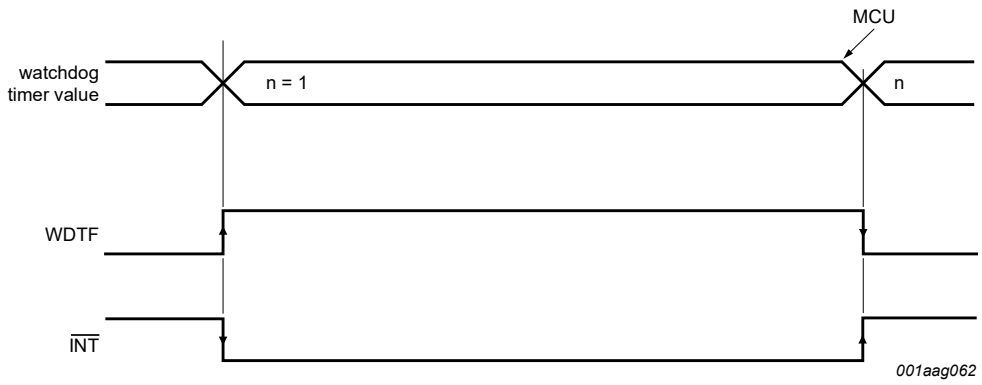
Remark: WDTF can be cleared by:

- Loading a value in register Watchdg_tim_val
- Writing a logic 0 to WDTF

Writing a logic 1 to WDTF has no effect.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



Counter reached 1, WDTF is logic 1, and an interrupt is generated.

Figure 14. WD_CD set logic 1: watchdog activates an interrupt when timed out

- When the watchdog timer counter reaches 1, the watchdog timer flag WDTF is set logic 1.
- When a minute or second interrupt occurs, the minute/second flag MSF is set logic 1 (see Section 7.13.1).

7.11.4 Predefined timers: second and minute interrupts

PCF2131 has two predefined timers, which are used to generate an interrupt either once per second or once per minute (see Section 7.13.1). The pulse generator for the minute or second interrupt operates from an internal 64 Hz clock. It is independent of the watchdog timer. Each of these timers can be enabled by the bits Second Interrupt (SI) and Minute Interrupt (MI) in register Control_1.

7.11.5 Clearing flags

The flags MSF and AF can be cleared by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Two examples are given for clearing the flags. Clearing a flag is made by a write command:

- Bits labeled with - must be written with their previous values
- Bits labeled with T have to be written with their default values
- WDTF is read-only and has to be written with logic 0

Repeatedly rewriting these bits has no influence on the functional behavior.

Table 60. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	MSF	WDTF	T	AF	T	-	-	T

Table 61. Example values in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	0	1	0	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 62. Example to clear only AF (bit 4)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	0	0	0	0[1]	0 [1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

Table 63. Example to clear only MSF (bit 7)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	0	1	0	0[1]	0 [1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

7.12 Timestamp function

The PCF2131 has four active LOW timestamp input pins $\overline{TS1}$, $\overline{TS2}$, $\overline{TS3}$, and $\overline{TS4}$, internally pulled with on-chip pullup resistors to $V_{oper(int)}$. It also has a timestamp detection circuit, which can detect the event when inputs on pin $\overline{TS1/2/3/4}$ are driven to ground.

The timestamp function is enabled by default after power on and it can be switched off by setting the control bit TSOFF (register Timestp_ctl1/2/3/4).

The time recorded in the timestamps, when in 100 Hz disable mode (1 Hz mode), is at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of the timestamp event is required then subtract 2 subseconds from the timestamp value and the result has -0 subseconds to +1 subseconds of uncertainty.

A most common application of the timestamp function is described in ref.[1].

See Section 7.13.5 for a description of interrupt generation from the timestamp function.

7.12.1 Timestamp flag

When the $\overline{TS1/2/3/4}$ input pin is driven to ground, the following sequence occurs:

1. The actual date and time are stored in the timestamp registers.
2. The timestamp flag TSF1/2/3/4 is set.
3. If the TSIE1/2/3/4 bit is active, and the corresponding interrupt mask is disabled, an interrupt on the $\overline{INTA/B}$ pin is generated.

The TSF1/2/3/4 and TSF1/2/3/4_2 flags can be cleared by command; clearing the flag clears the interrupt. Once TSF1/2/3/4 is cleared, it is set again only when $\overline{TS1/2/3/4}$ pin is driven to ground once again.

7.12.2 Timestamp mode

The timestamp function has two different modes selected by the control bit TSM (timestamp mode) in register Timestp_ctl:

- If TSM is logic 0 (default), in subsequent trigger events without clearing the timestamp flags, the last timestamp event is stored

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- If TSM is logic 1, in subsequent trigger events without clearing the timestamp flags, the first timestamp event is stored

The timestamp function also depends on the control bit BTSE in register Control_3, see Section 7.12.4.

7.12.3 Timestamp registers

This section covers the bit allocation and its description for various timestamp registers.

7.12.3.1 Register Timestp_ctl1/2/3/4

This section details the Timestp_ctl1/2/3/4 register, including its bit allocation and individual bit definitions.

Table 64. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	TSM	TSOFF	T	SUBSEC_TIMESTP[4:0]				
Reset value	0	0	0	0	0	0	0	0

Table 65. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7	TSM	0	In subsequent events without clearing the timestamp flags, the last event is stored
		1	In subsequent events without clearing the timestamp flags, the first event is stored
6	TSOFF	0	Timestamp function active
		1	Timestamp function disabled
5	-	-	Unused
4 to 0	SUBSEC_TIMESTP[4:0]		$^{1}/_{16}$ second timestamp information coded in BCD format when 100TH_S_DIS = '1'[1], $^{1}/_{20}$ second timestamp information coded in BCD format when 100TH_S_DIS = '0';

[1] The time recorded in the timestamps, when in 100 Hz disable mode (1 Hz mode), is at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of the timestamp event is required then subtract 2 subseconds from the timestamp value and the result has -0 subseconds to +1 subseconds of uncertainty.

7.12.3.2 Register Sec_timestp

This section details the Sec_timestp register, including its bit allocation and individual bit definitions.

Table 66. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	SECOND_TIMESTP (0 to 59)						

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 66. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit allocation*...continued*

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 67. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	Unused
6 to 4	SECOND_TIMESTP	0 to 5	Ten's place	Second timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.3 Register Min_timestp

This section details the Min_timestp register, including its bit allocation and individual bit definitions.

Table 68. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	MINUTE_TIMESTP (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 69. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	Unused
6 to 4	MINUTE_TIMESTP	0 to 5	Ten's place	Minute timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.4 Register Hour_timestp

This section details the Hour_timestp register, including its bit allocation and individual bit definitions.

Table 70. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
			HOUR_TIMESTP (0 to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 71. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	Unused
12-hour mode[1]				
5	AMPM	0	-	Indicates AM
		1	-	Indicates PM
4	HOUR_TIMESTP	0 to 1	Ten's place	Hour timestamp information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	Unit place	
24-hour mode [1]				
5 to 4	HOUR_TIMESTP	0 to 2	Ten's place	Hour timestamp information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	Unit place	

[1] Bit 12_24 in register Control_1 sets the hour mode.

7.12.3.5 Register Day_timestp

This section details the Day_timestp register, including its bit allocation and individual bit definitions.

Table 72. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAY_TIMESTP (1 to 31)					
Reset value	0	0	0	0	0	0	0	0

Table 73. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	Unused
5 to 4	DAY_TIMESTP	0 to 3	Ten's place	Day timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.6 Register Mon_timestp

This section details the Mon_timestp register, including its bit allocation and individual bit definitions.

Table 74. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTH_TIMESTP (1 to 12)				
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 75. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	Unused
4	MONTH_TIMESTP	0 to 1	Ten's place	Month timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.3.7 Register Year_timestp

This section details the Year_timestp register, including its bit allocation and individual bit definitions.

Table 76. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	YEAR_TIMESTP (0 to 99)							
Reset value	0	0	0	0	0	0	0	1

Table 77. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_TIMESTP	0 to 9	Ten's place	Year timestamp information coded in BCD format
3 to 0		0 to 9	Unit place	

7.12.4 Dependency between Battery switch-over and timestamp

The timestamp function depends on the control bit BTSE in register Control_3:

Table 78. Battery switch-over and timestamp

BTSE	BF	Note	Description
0	-	[1]	The battery switch-over does not affect the timestamp registers
1			If a battery switch-over event occurs:
	0	[1]	The timestamp 4 group registers store the time and date when the switch-over occurs; after this event occurred BF is set logic 1
	1		The timestamp 4 group registers are not modified; in this condition subsequent battery switch-over events or falling edges on pin $\overline{TS4}$ are not registered

[1] Default value.

7.13 Interrupt output, $\overline{INTA}$/$\overline{INTB}$

PCF2131 has two interrupt output pins $\overline{INTA}$ and $\overline{INTB}$, which are open-drain, active LOW (requiring a pullup resistor if used). Interrupts can be sourced from different places:

- Second or minute timer
- Watchdog timer

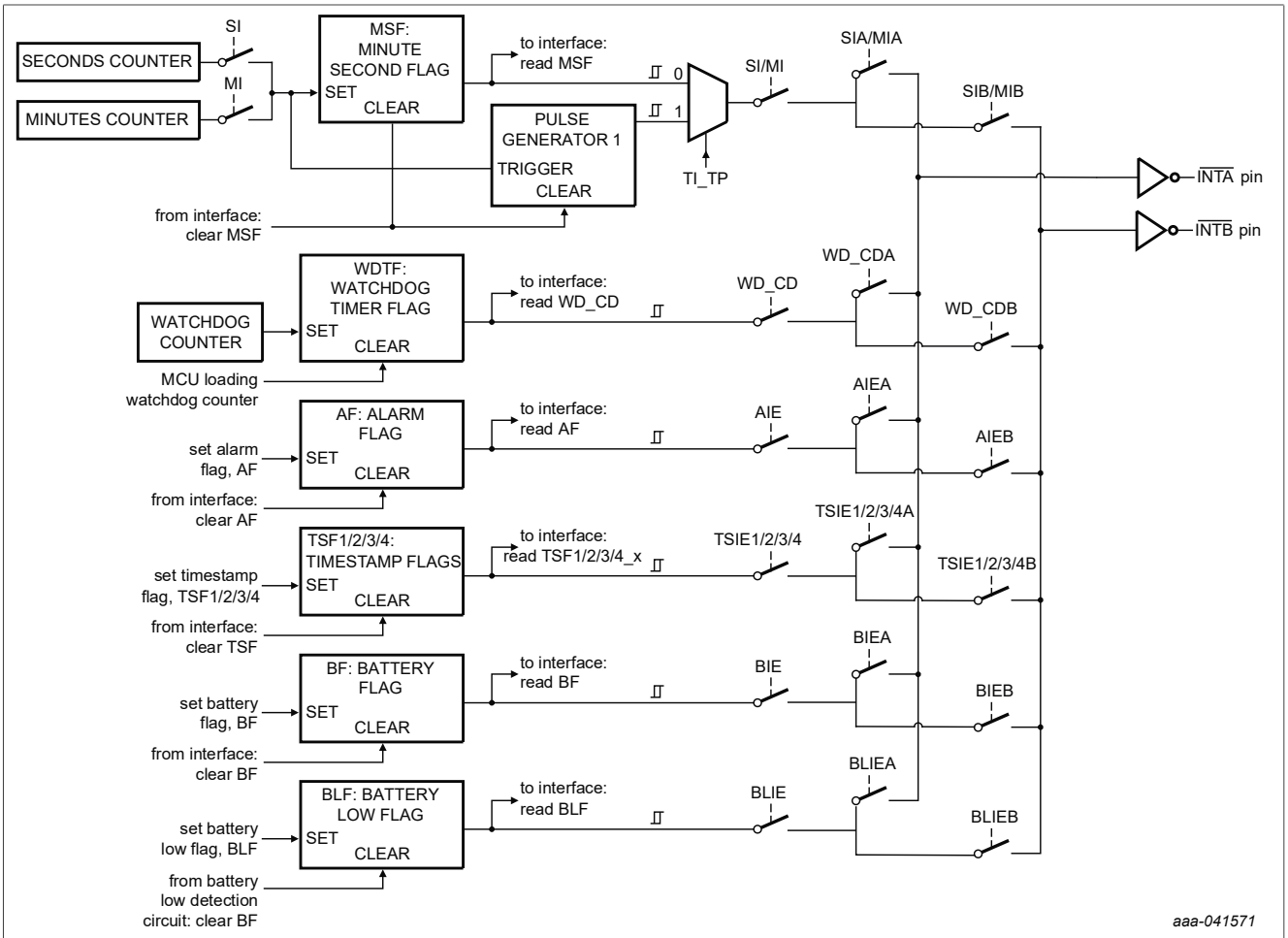
All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- Alarm
- Timestamp1/2/3/4
- Battery switch-over
- Battery low detection

The control bit TI_TP (register Watchdg_tim_ctl) is used to configure whether the interrupts generated from the second/minute timer (flag MSF in register Control_2) are pulsed signals or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags. When the interrupt sources are all disabled, $\overline{\text{INTA/B}}$ remains high-impedance.

- The flags MSF, AF, TSFx, and BF can be cleared by command.
- The flag WDTF is read-only. How it can be cleared is explained in Section 7.11.5.
- The flag BLF is read-only. It is cleared automatically from the battery low detection circuit when the battery is replaced.



When SI, MI, WD_CD, AIE, TSIE1/2/3/4, BIE, BLIE are all disabled, $\overline{\text{INTA/INTB}}$ remains high-impedance.

Figure 15. Interrupt block diagram

7.13.1 Minute and second interrupts

Minute and second interrupts are generated by predefined timers. The timers can be enabled independently from one another by the bits MI and SI in register Control_1. However, a minute interrupt enabled on top of a second interrupt cannot be distinguishable since it occurs at the same time.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

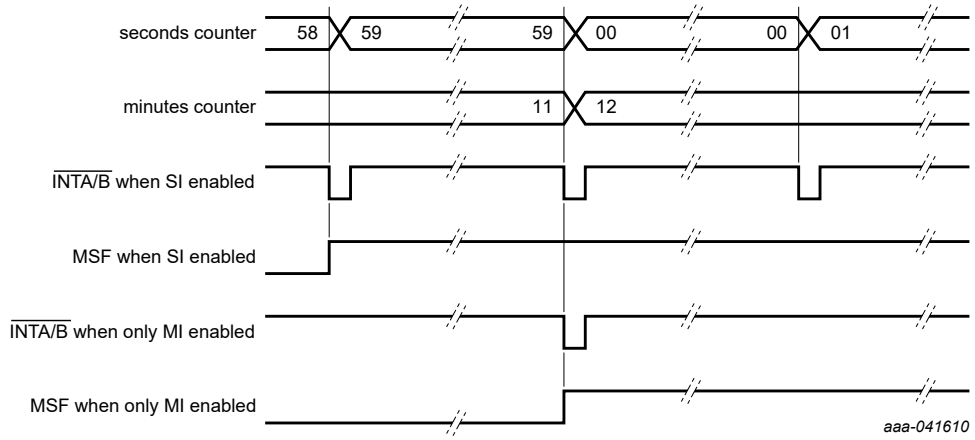
The minute/second flag MSF (register Control_2) is set logic 1 when either the seconds or the minutes counter increments according to the enabled interrupt (see Table 79). The MSF flag can be cleared by command.

Table 79. Effect of bits MI and SI on pin $\overline{\text{INTA/B}}$ and bit MSF

MI	SI	Result in $\overline{\text{INTA/B}}$	Result on MSF
0	0	No interrupt generated	MSF never sets
1	0	An interrupt once per minute	MSF is set when **minutes** counter increments
0	1	An interrupt once per second	MSF is set when **seconds** counter increments
1	1	An interrupt once per second	MSF is set when **seconds** counter increments

When MSF is set logic 1:

- If TI_TP is logic 1, the interrupt is generated as a pulsed signal if not masked.
- If TI_TP is logic 0, the interrupt is permanently active until MSF is cleared.

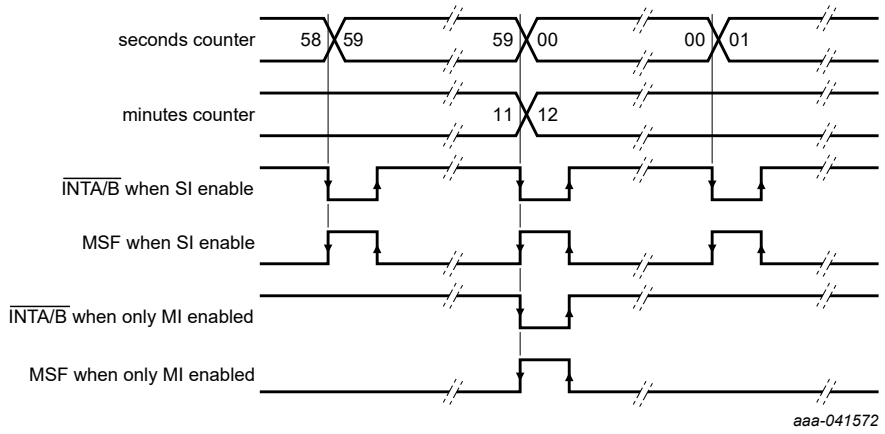


In this example, bit TI_TP is logic 1 and the MSF flag is not cleared after an interrupt.

Figure 16. $\overline{\text{INTA/B}}$ example for SI and MI when TI_TP is logic 1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



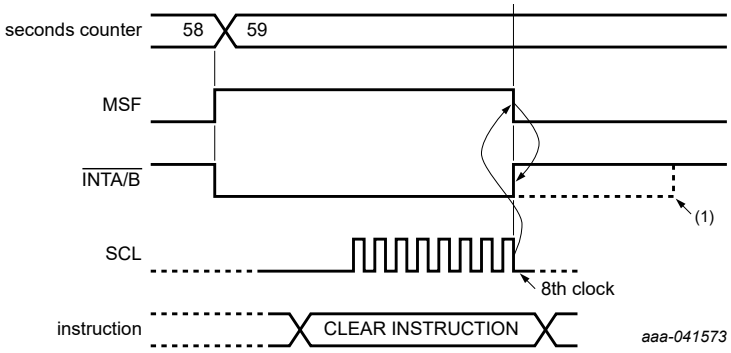
In this example, bit TI_TP is logic 0 and the MSF flag is cleared after an interrupt.

Figure 17. INTA/B example for SI and MI when TI_TP is logic 0

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and generates a pulse of $^{1}/_{64}$ seconds in duration.

7.13.2 INTA/B pulse shortening

If the MSF flag (register Control_2) is cleared before the end of the INTA/B pulse, then the INTA/B pulse is shortened. It allows the source of a system interrupt to be cleared immediately when it is serviced, that is, the system does not have to wait for the completion of the pulse before continuing; see Figure 18. Instructions for clearing the bit MSF can be found in Section 7.11.5.



1. Indicates normal duration of INTA/B pulse.

The timing shown for clearing bit MSF is also valid for the non-pulsed interrupt mode, that is, when TI_TP is logic 0, where the INTA/B pulse can be shortened by setting both bits MI and SI logic 0.

Figure 18. Example of shortening the INTA/B pulse by clearing the MSF flag

7.13.3 Watchdog timer interrupts

The generation of interrupts from the watchdog timer is controlled using the WD_CD bit (register Watchdg_tim_ctl). The interrupt is generated as an active signal, which follows the status of the watchdog timer flag WDTF (register Control_2) if not masked. No pulse generation is possible for watchdog timer interrupts.

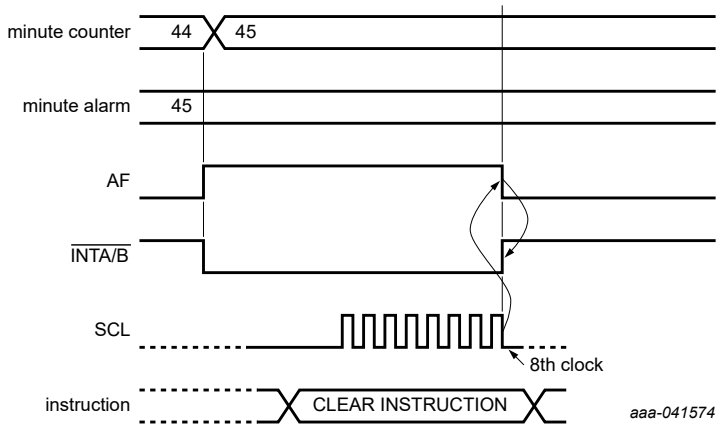
The interrupt is cleared when the flag WDTF is reset. Instructions for clearing it can be found in Section 7.11.5.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.13.4 Alarm interrupts

Generation of interrupts from the alarm function is controlled by the bit AIE (register Control_2). If AIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit AF (register Control_2) if not masked. Clearing AF immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for alarm interrupts.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 19. AF timing diagram

7.13.5 Timestamp interrupts

Interrupt generation from the timestamp function is controlled using the TSIE1-4 bit (register Control_5). If TSIE1-4 is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of the flags TSF1/2/3/4, if not masked. Clearing the flags TSFx immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for timestamp interrupts.

7.13.6 Battery switch-over interrupts

Generation of interrupts from the battery switch-over is controlled by the BIE bit (register Control_3). If BIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit BF in register Control_3 if not masked(see Table 78). Clearing BF immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for battery switch-over interrupts.

7.13.7 Battery low detection interrupts

Generation of interrupts from the battery low detection is controlled by the BLIE bit (register Control_3). If BLIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit BLF (register Control_3) if not masked. The interrupt is cleared when the battery is replaced (BLF is logic 0) or when bit BLIE is disabled (BLIE is logic 0). BLF is read only and therefore cannot be cleared by command.

7.13.8 Interrupt masks

This section details the Interrupt masks register, including its bit allocation and individual bit definitions.

Table 80. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INT_A/B_MASK1							
Reset value	-	-	1	1	1	1	1	1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 81. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 6	T	00	Unused
5	MIA/B	1	Minute interrupt mask
4	SIA/B	1	Second interrupt mask
3	WD_CDA/B	1	Watchdog interrupt mask
2	AIEA/B	1	Alarm interrupt mask
1	BIEA/B	1	Battery flag interrupt mask
0	BLIEA/B	1	Battery low flag interrupt mask

Table 82. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INT_A/B_MASK2							
Reset value	T	T	T	T	1	1	1	1

Table 83. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	T	0000	Unused
3	TSIE1A/B	1	Timestamp 1 interrupt mask
2	TSIE2A/B	1	Timestamp 2 interrupt mask
1	TSIE3A/B	1	Timestamp 3 interrupt mask
0	TSIE4A/B	1	Timestamp 4 interrupt mask

The registers at addresses 31h to 32h are used to configure interrupt source for $\overline{\text{INTA}}$ pin, and the registers at addresses 33h to 34h are for $\overline{\text{INTB}}$ pin.

All of above interrupts could be masked from either $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$, with corresponding bit set to ‘1’, as shown in Figure 15.

7.14 Stop bit function

The stop bit stops the time from counting. STOP must be set to unlock the time and date registers to set the time.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

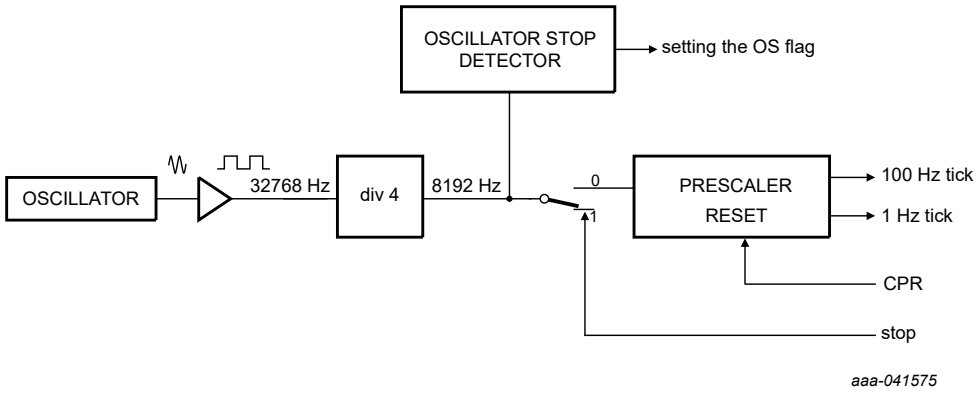


Figure 20. CPR and stop bit functional diagram

The *stop* signal blocks the 8.192 kHz clock from generating system clocks and freezes the time. In this state, the prescaler can be cleared with the CPR command in the Resets register.

Remark: The CLKOUT output of clock frequencies is not affected.

The time circuits can then be set and do not increment until the stop bit is released. There is a slight chance that STOP is set during a carry over of multiple time registers, which may have been executed incomplete. Therefore, a time must be set before clearing STOP to maintain time integrity.

The *stop* acts on the 8.192 kHz signal. Because the I^2C-bus or TS pin input is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero, and one 8.192 kHz cycle (see Figure 21).

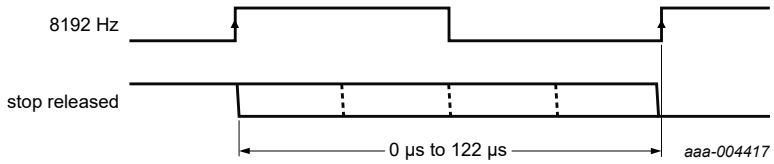


Figure 21. STOP release timing

The first increment of the time circuits is between 0 s and 122 µs after STOP is released.

7.15 Interfaces

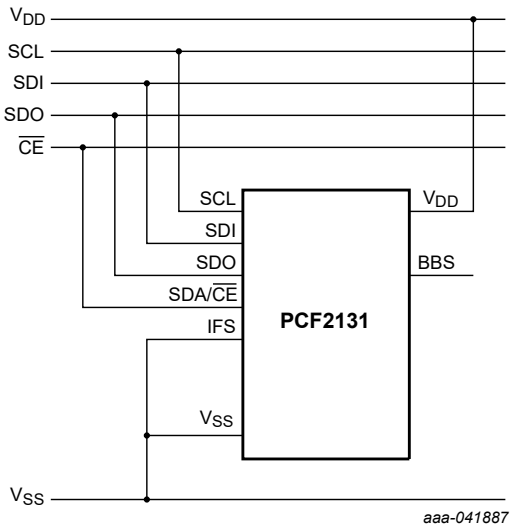
The PCF2131 has an I^2C-bus or SPI-bus interface using the same pins. The selection is done using the interface selection pin IFS (see Table 84).

Table 84. Interface selection input pin IFS

Pin	Connection	Bus interface	Reference
IFS	V_{SS}	SPI-bus	Section 7.15.1
	V_{DD}	I^2C-bus	Section 7.15.2

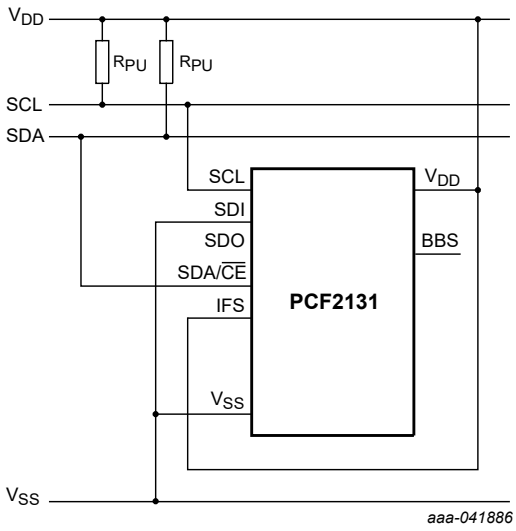
All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



To select the SPI-bus interface, pin IFS has to be connected to pin V_{SS}.

a. SPI-bus interface selection



To select the I^2C-bus interface, pin IFS has to be connected to pin V_{DD}.

b. I^2C-bus interface selection

Figure 22. Interface selection

7.15.1 SPI-bus interface

Data transfer to and from the device is made by a 4-line SPI-bus (see Table 85). The data lines for input and output are split. The SPI-bus is initialized whenever the chip enable line pin SDA/$\overline{CE}$ is inactive.

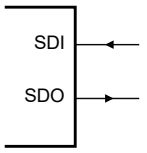


Figure 23. SDI, SDO configurations

Table 85. Serial interface

Symbol	Function	Note	Description
SDA/$\overline{CE}$	Chip enable input; active LOW	[1]	When HIGH, the interface is reset; Input can be higher than V_{DD}
SCL	Serial clock input		When SDA/$\overline{CE}$ is HIGH, the input can float; Input can be higher than V_{DD}
SDI	Serial data input		When SDA/$\overline{CE}$ is HIGH, the input can float; Input can be higher than V_{DD}; Input data is sampled on the rising edge of SCL
SDO	Serial data output		Push-pull output; Drives from V_{SS} to $V_{oper(int)}$ (V_{BBS}); Output data is changed on the falling edge of SCL

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

[1] The chip enable must not be wired permanently LOW.

7.15.1.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a whole byte, with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal SDA/$\overline{CE}$. The first byte transmitted is the command byte. Subsequent bytes are either data to be written or data to be read (see Figure 24).

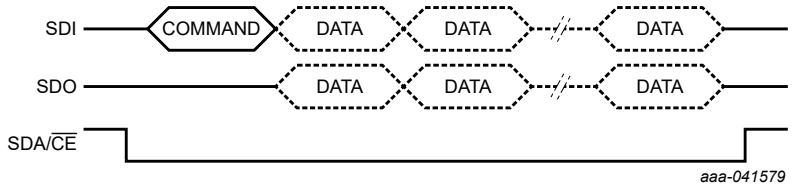
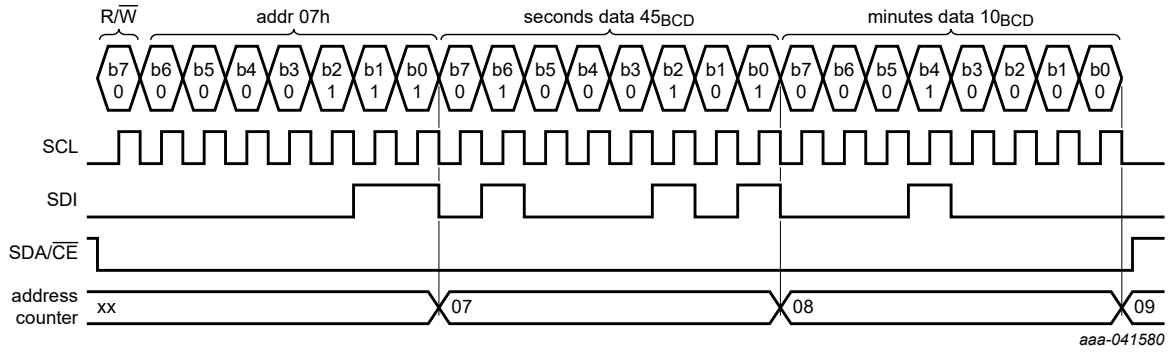


Figure 24. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter auto-increments after every access and reset to zero after the last valid register is accessed. The R/$\overline{W}$ bit defines if the following bytes are read or write information.

Table 86. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		Data read or write selection
		0	Write data
		1	Read data
6 to 0	RA	00h to 36h	Register address

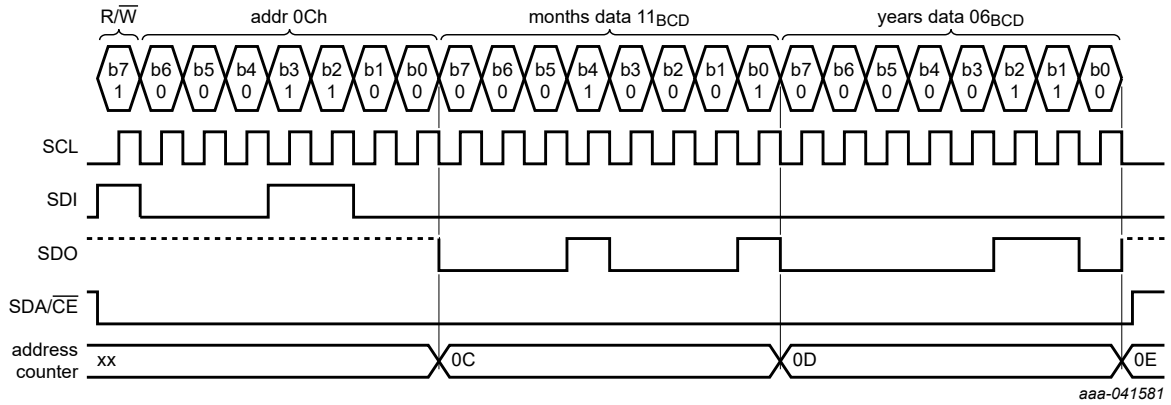


In this example, the Seconds register is set to 45 seconds and the Minutes register to 10 minutes.

Figure 25. SPI-bus write example

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



In this example, the registers Months and Years are read. The pins SDI and SDO are not connected. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents can result.

Figure 26. SPI-bus read example

7.15.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines are connected to a positive supply by a pullup resistor. Data transfer is initiated only when the bus is not busy.

7.15.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 27).

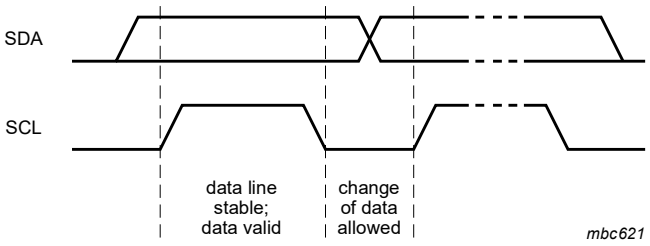


Figure 27. Bit transfer

7.15.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition S. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Figure 28).

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

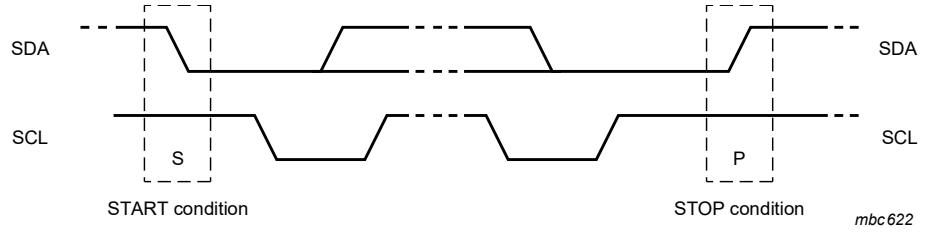


Figure 28. Definition of START and STOP conditions

7.15.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the controller; and the devices, which are controlled by the controller are the targets.

The PCF2131 can act as a target transmitter and a target receiver.

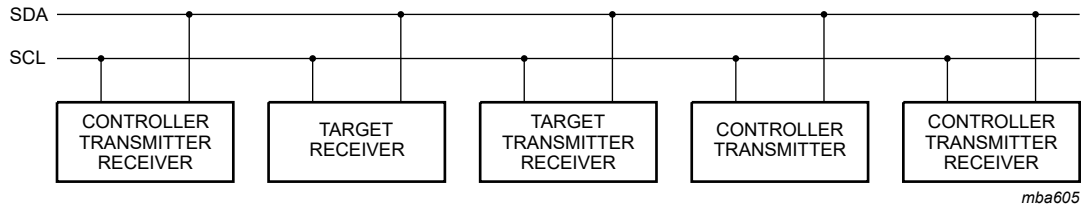


Figure 29. System configuration

7.15.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A target receiver, which is addressed must generate an acknowledge after the reception of each byte.
- Also, a controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

Acknowledgment on the I^2C-bus is illustrated in Figure 30.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

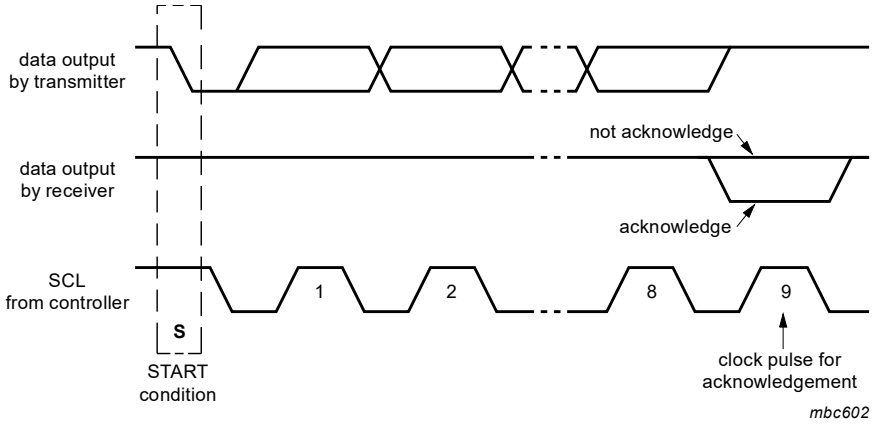


Figure 30. Acknowledgment on the I²C-bus

7.15.2.5 I²C-bus protocol

After a start condition, a valid hardware address has to be sent to a PCF2131 device. The appropriate I²C-bus target address is 1010 011. The entire I²C-bus target address byte is shown in Table 87.

Table 87. I²C target address byte

	Target address							
Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	1	0	1	0	0	1	1	R/$\overline{W}$

The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfers (read is logic 1, write is logic 0).

For the format and the timing of the START condition (S), the STOP condition (P), and the acknowledge (A) refer to the I²C-bus specification ref.[3] and the characteristics table (Table 92). In the write mode, a data transfer is terminated by sending a STOP condition.

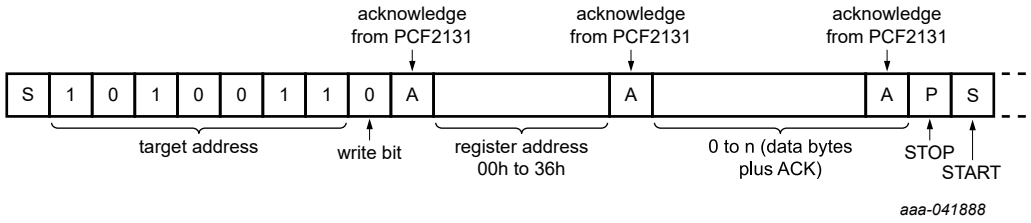


Figure 31. Bus protocol, writing to registers

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

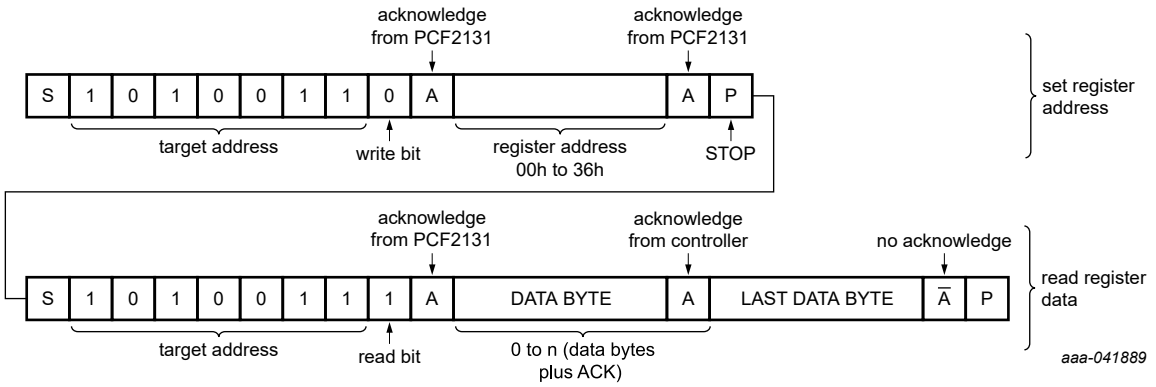


Figure 32. Bus protocol, reading from registers

7.15.3 Bus communication and battery backup operation

To save power during battery backup operation (see Section 7.5.1), the bus interfaces are inactive. Therefore, the communication via I^2C or SPI-bus must be terminated before the supply of the PCF2131 is switched from V_{DD} to V_{BAT}.

With I2C interface, PCF2131 terminates transaction before switching from V_{DD} to V_{BAT}, with SPI interface, PCF2131 corrupts SPI write and read data when battery switchover occurs.

Remark: If the I^2C-bus communication was terminated uncontrollably, the I^2C-bus has to be reinitialized by sending a STOP followed by a START after the device switched back from battery backup operation to V_{DD} supply operation.

7.16 Internal circuitry

Figure 33 shows the labeled device diode protection diagram of PCF2131.

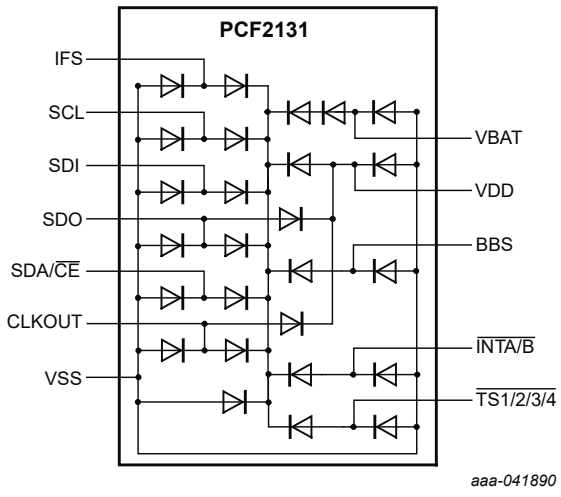


Figure 33. Device diode protection diagram of PCF2131

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.17 Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

8 Limiting values

Table 88 describes the limiting values of PCF2131.

Table 88. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Note	Min	Max	Unit
V_{DD}	Supply voltage			-0.5	+6.5	V
I_{DD}	Supply current			-50	+50	mA
V_i	Input voltage			-0.5	+6.5	V
I_I	Input current			-10	+10	mA
V_O	Output voltage			-0.5	+6.5	V
I_O	Output current			-10	+10	mA
		At pin SDA/$\overline{CE}$		-10	+20	mA
V_{BAT}	Battery supply voltage			-0.5	+6.5	V
P_{tot}	Total power dissipation			-	300	mW
V_{ESD}	Electrostatic discharge voltage	HBM	[1]	-	±2 000	V
		CDM	[2]	-	±500	V
I_{lu}	Latch-up current		[3]	-	1 00	mA
T_{stg}	Storage temperature		[4]	-55	+85	°C
T_{amb}	Ambient temperature	Operating device		-40	+85	°C

[1] Pass level; Human Body Model (HBM) according to AEC Q100-002.
[2] Pass level (750 V for corner pins); Charged-Device Model (CDM), according to AEC Q100-011.
[3] Pass level; latch-up testing according to AEC Q100-004 at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see ref.[4]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

Note: *The PCF2131 part is not guaranteed (nor characterized) above the operating range as denoted in the data sheet. NXP recommends not to bias the PCF2131 device during reflow (for example, if using a 'coin' type battery in the assembly). If the customer so chooses to use this assembly method, there must be the allowance for a full \Q0 V' level power supply \Qreset' to re-enable the device. Without a proper POR, the device can remain in an indeterminate state.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

9 Static characteristics

Table 89 describes the static characteristics of PCF2131.

Table 89. Static characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
Supplies							
V_{DD}	Supply voltage		[1]	1.2	-	5.5	V
V_{BAT}	Battery supply voltage			1.2	-	5.5	V
V_{low}	Low voltage			-	1.15	-	V
I_{DD} Supply current [2]		Interface active; supplied by V_{DD}					
		SPI-bus (f_{SCL} = 6.5 MHz)		-	-	800	µA
		I^2C-bus (f_{SCL} = 400 kHz)		-	-	200	µA
		Interface inactive (f_{SCL} = 0 Hz)[3]; TCR[1:0] = 00 (see Table 16)					
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V		-	88	400	nA
		V_{DD} = 3.3 V		-	64	350 [4]	nA
		V_{DD} = 5.5 V		-	71	450	nA
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V		-	101	500	nA
		V_{DD} = 3.3 V		-	70	450	nA
		V_{DD} = 5.5 V		-	76	550	nA
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 000 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5);					
		V_{DD} = 1.2 V	[5]	-	460	770	nA
		V_{DD} = 3.3 V	[5]	-	1035	1365	nA
		V_{DD} = 5.5 V	[5]	-	1670	2135	nA
		PWRMNG[2:0] = 000 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V		-	118	500	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V		-	104	500	nA
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V		-	107	550	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	104	565	nA
		V_{BAT} = 3.3 V, I_{BAT}:	[6]	-	83	450	nA

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 89. Static characteristics...*continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
		V_{BAT} = 5.5 V, I_{BAT}:	[6]	-	91	625	nA
I_{DD} Supply current [2]		PWRMNG[2:0] = 000 (see Table 22); COF[2:0] = 000 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V	[5]	-	640	945	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V	[5]	-	1060	1410	nA
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V	[5]	-	1705	2190	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	130	590	nA
		V_{BAT} = 3.3 V, I_{BAT}	[6]	-	145	560	nA
		V_{BAT} = 5.5 V, I_{BAT}	[6]	-	210	750	nA
$I_{L(bat)}$	Battery leakage current	V_{DD} is an active supply; V_{BAT} = 3.0 V		-	0.1	-	nA
Power management							
$V_{th(sw)bat}$	Battery switch threshold voltage			2.3	2.5		V
$V_{th(bat)low}$	Low battery threshold voltage			2.3	2.5		V
Inputs [7]							
V_I	Input voltage			-0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage			-	-	$0.25V_{DD}$	V
		T_{amb} = -40 °C to +85 °C; V_{DD} > 2.0 V		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
I_{LI}	Input leakage current	V_I = V_{DD} or V_{SS}		-	0	-	µA
		Post ESD event		-1	-	+1	µA
C_i	Input capacitance		[8]	-	-	7	pF
Outputs							
V_O	Output voltage	On pins $\overline{INTA/B}$, referring to the external pullup		-0.5	-	5.5	V
		On pin BBS	[9]	1.2	-	5.5	V
V_{OH}	HIGH output voltage	On pin SDO, CLKOUT at 1 mA source current		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW output voltage	On pins CLKOUT, $\overline{INTA/B}$ and SDO at 1 mA sink current		V_{SS}	-	$0.2V_{DD}$	V
		On pin SDA, V_{DD} > 2.0 V, 3 mA sink current		-	-	0.4	V
		On pin SDA, V_{DD} < 2.0 V, 2 mA sink current		-	-	$0.2V_{DD}$	V

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 89. Static characteristics...*continued*

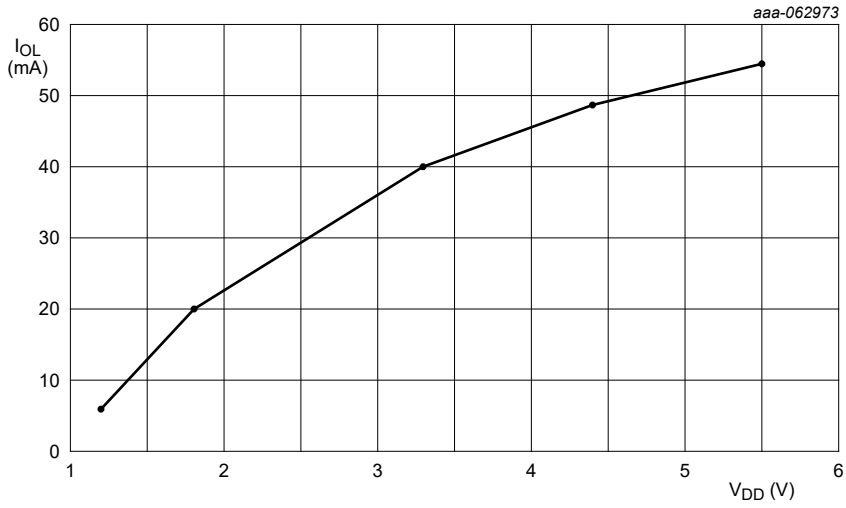
V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	Output sink current; V_{OL} = 0.4 V					
		On pin SDA/$\overline{CE}$	[10]	3	-	-	mA
		On all other outputs		1.0	-	-	mA
I_{OH}	HIGH-level output current	Output source current; on pin SDO, CLKOUT; V_{OH} = 0.8 * V_{DD}		1.0	-	-	mA
I_{LO}	Output leakage current	V_O = V_{DD} or V_{SS}		-	0	-	µA
		Post ESD event		-1	-	+1	µA

[1] For reliable oscillator startup and OTP refresh at power on: V_{DD} must be above 1.8 V.
[2] MAX I_{DD} and I_{BAT} determined by characterization.
[3] Timer source clock = $^{1}/_{60}$ Hz, level of pins SDA/$\overline{CE}$, SDI, and SCL is V_{DD} or V_{SS}.
[4] Production tested I_{DD} parameter.
[5] Any load in the application driven by CLKOUT adds to this value, for example, 10 pF, Vdd = 3v3 adds 32768 Hz * 10 pF * 3.3 V = 1.1 µA.
[6] When the device is supplied by the V_{BAT} pin instead of the V_{DD} pin, V_{DD} = 0 V. The device can only start up from V_{DD}.
[7] The I^2C-bus and SPI-bus interfaces of PCF2131 are 5 V tolerant.
[8] Tested on a sample basis.
[9] Pin BBS is internally connected to either V_{DD} or V_{BAT}, see section Section 7.5.3.
[10] For further information, see Figure 34.

9.1 Current consumption characteristics, typical

This section shows the current consumption characteristics for PCF2131.

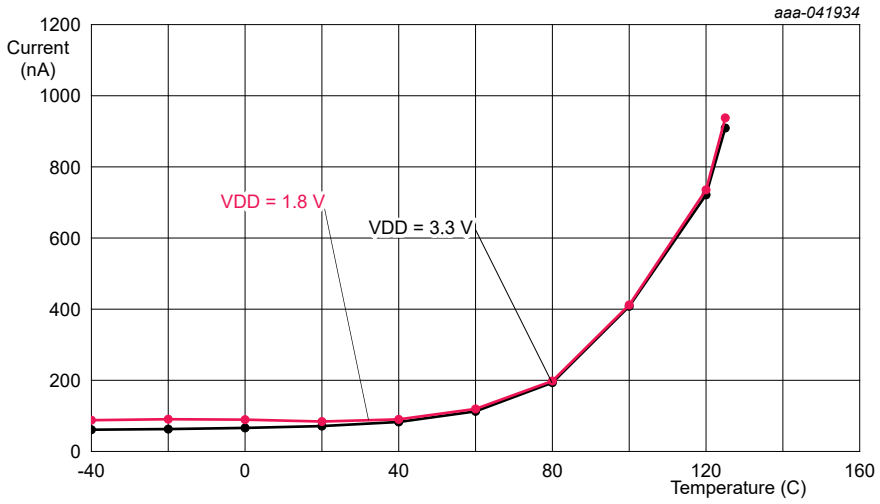


Typical value; V_{OL} = 0.4 V.

Figure 34. I_{OL} on pin SDA/$\overline{CE}$

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

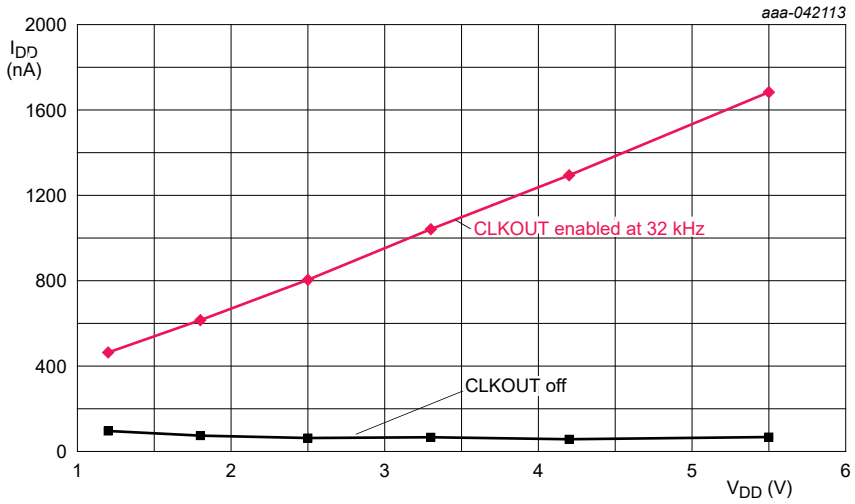


CLKOUT disabled; PWRMNG[2:0] = 111; TSOFF = 1; $\overline{TS}$ input floating.

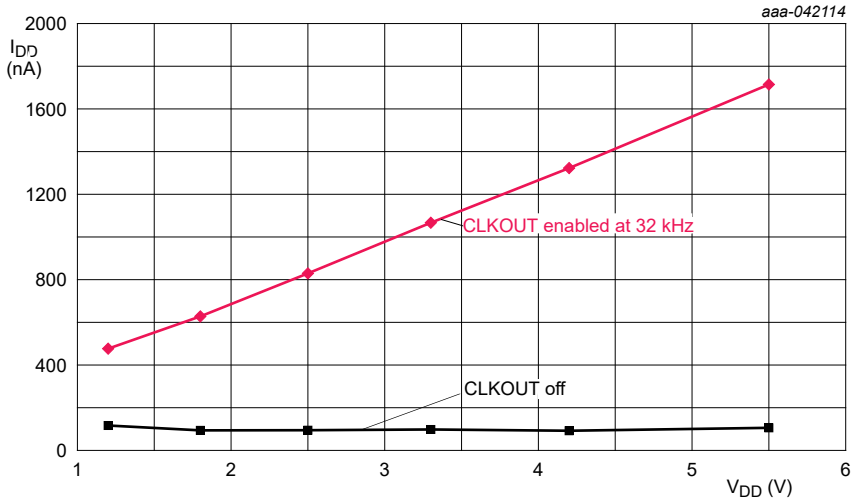
Figure 35. I_{DD} as a function of temperature

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



a. PWRMNG[2:0] = 111; TSOFF = 1; T_{amb} = 25 °C; $\overline{TS}$ input floating



b. PWRMNG[2:0] = 000; TSOFF = 0; T_{amb} = 25 °C; $\overline{TS}$ input floating

Figure 36. I_{DD} as a function of V_{DD}

9.2 Frequency characteristics

This section describes the frequency characteristics for PCF2131.

Table 90. Frequency characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_o	Output frequency	On pin CLKOUT; V_{DD} = 3.3 V; COF[2:0] = 000; AO[3:0] = 1000		-	32.768	-	kHz
Δf/f	Time accuracy	V_{DD} or V_{BAT} = 3.3 V, Tamb = -40 °C to +85 °C					
		TC_DIS = 0	[1] [2]	-8	±3	+8	ppm

All information provided in this document is subject to legal disclaimers.

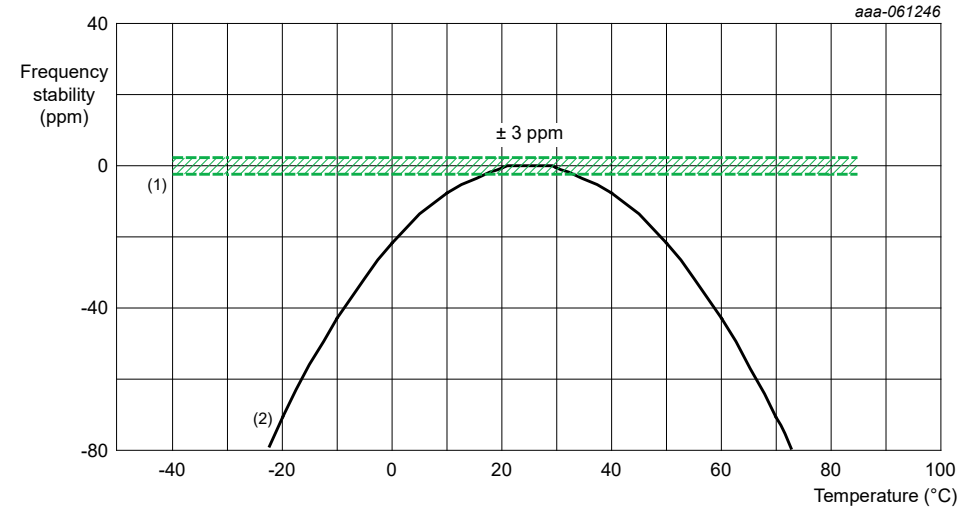
© 2026 NXP B.V. All rights reserved.

Table 90. Frequency characteristics...*continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		TC_DIS = 1	[1] [2]	-200		+4	ppm
		TC_DIS = 1, Tamb = 25 °C	[1] [2]	-3		+3	ppm
$\Delta f_{xtal}/f_{xtal}$	Relative crystal frequency variation	Crystal aging					
		PCF2131					
		First year; V_{DD} or V_{BAT} = 3.3 V	[3]	-3	-	+3	ppm
Δf/ΔV	Frequency variation with the voltage	On pin CLKOUT		-	±1	-	ppm/V
Jitter	Output clock peak-to-peak jitter	On pin CLKOUT		-	50	-	ns

[1] ±1 ppm corresponds to a time deviation of ±0.0864 seconds per day.
[2] Only valid if CLKOUT frequencies are not equal to 32.768 kHz or if CLKOUT is disabled.
[3] Not production tested. Effects of reflow soldering are included (see application note AN13203).



1. Performance is achieved with temperature compensation.
2. Typical uncalibrated oscillator performance.

Figure 37. Temperature compensation comparison

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

10 Dynamic characteristics

This section explains about the SPI-bus timing characteristics and I^{2}C-bus timing characteristics.

10.1 SPI-bus timing characteristics

Table 91 describes the SPI-bus characteristics for PCF2131.

Table 91. SPI-bus characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} (see Figure 38).

Symbol	Parameter	Conditions	Note	V_{DD} = 1.2 V to 3.3 V		V_{DD} = 3.3 V to 5.5 V		Unit
				Min	Max	Min	Max	
Pin SCL								
$f_{clk(SCL)}$	SCL clock frequency			-	0.5	-	6.5	MHz
$t_{clk(H)}$	Clock HIGH time			1000	-	70	-	ns
$t_{clk(L)}$	Clock LOW time			1000	-	70	-	ns
t_r	Rise time	For SCL signal		-	100	-	100	ns
t_f	Fall time	For SCL signal		-	100	-	100	ns
Pin SDA/$\overline{CE}$								
$t_{su(CE_N)}$	CE_N set-up time			300	-	30	-	ns
$t_{h(CE_N)}$	CE_N hold time			325	-	25	-	ns
$t_{rec(CE_N)}$	CE_N recovery time			1500	-	1500	-	ns
$t_{w(CE_N)}$	CE_N pulse width			-	0.99	-	0.99	s
Pin SDI								
t_{su}	Set-up time	Set-up time for SDI data		250	-	20	-	ns
t_h	Hold time	Hold time for SDI data		250	-	20	-	ns
Pin SDO								
$t_{d(R)SDO}$	SDO read delay time	C_L = 50 pF		-	550	-	55	ns
$t_{dis(SDO)}$	SDO disable time		[1]	-	150	-	25	ns

[1] No load value; bus is held up by bus capacitance; use RC time constant with application values.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

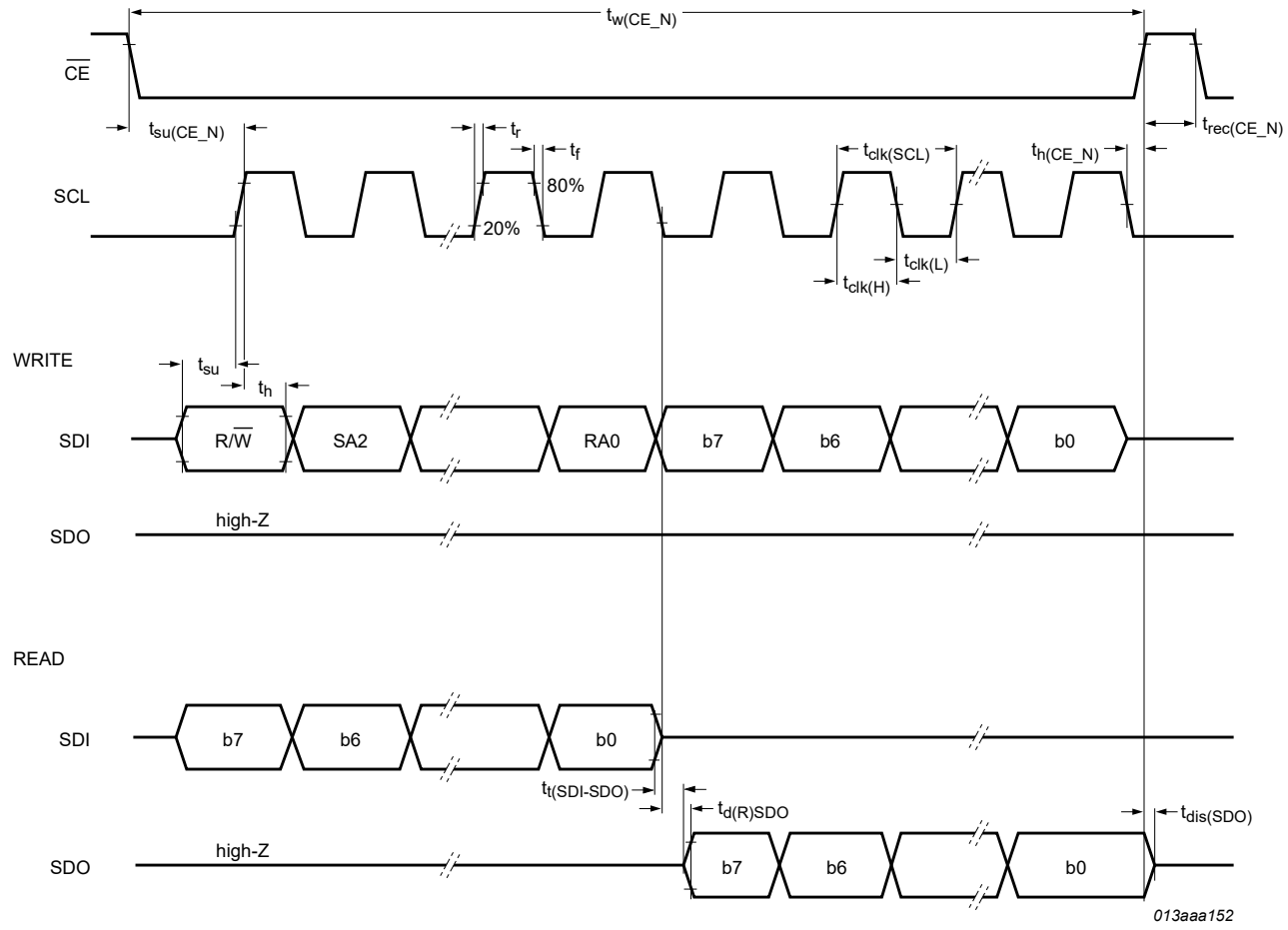


Figure 38. SPI-bus timing

10.2 I²C-bus timing characteristics

Table 92 describes the I²C-bus characteristics for PCF2131.

Table 92. I²C-bus characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 39).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Unit
			Min	Max	Min	Max	
Pin SCL							
f_{SCL}	SCL clock frequency	[1]	10	100	10	400	kHz
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
Pin SDA/$\overline{CE}$							
$t_{SU;DAT}$	Data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	[2]	0	-	0	-	ns
Pins SCL and SDA/$\overline{CE}$							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 92. I^2C-bus characteristics...*continued*

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 39).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Unit
			Min	Max	Min	Max	
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.5	-	µs
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	µs
t_r	Rise time of both SDA and SCL signals	[2] [3] [4]	-	1 000	$20 + 0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	[2] [3] [4]	-	300	$20 + 0.1C_b$	300	ns
$t_{VD;ACK}$	Data valid acknowledge time	[5]	-	3.45	-	0.9	µs
$t_{VD;DAT}$	Data valid time	[6]	-	3.45	-	0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.
[2] A controller device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[3] C_b is the total capacitance of one bus line in pF.
[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA/$\overline{CE}$ pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum t_f.
[5] $t_{VD;ACK}$ is the time of the acknowledgment signal from SCL LOW to SDA (out) LOW.
[6] $t_{VD;DAT}$ is the minimum time for valid SDA (out) data following SCL LOW.
[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

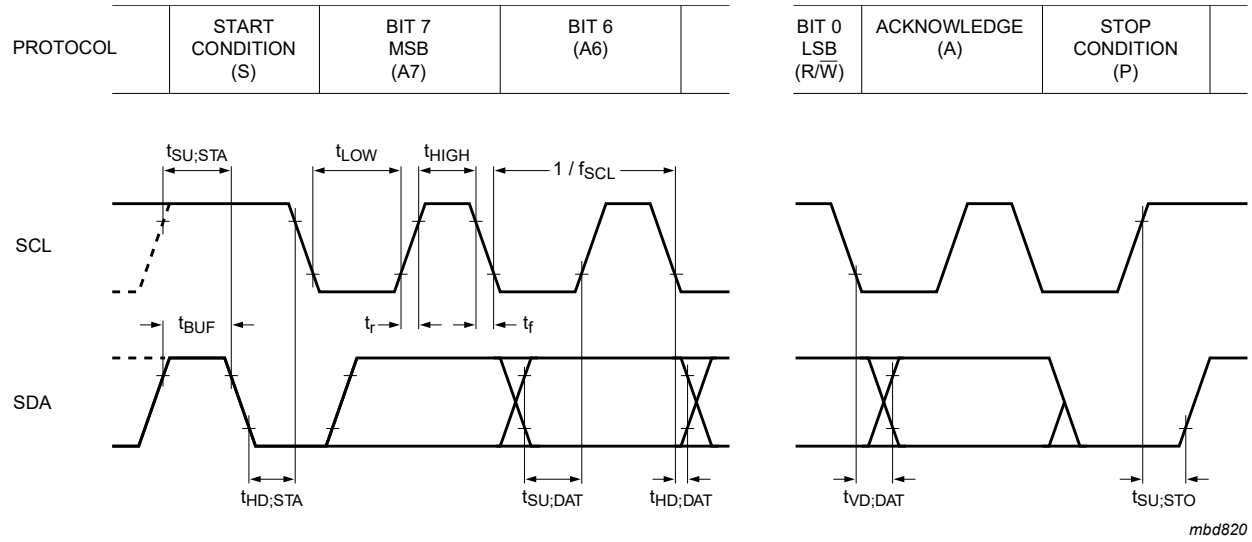


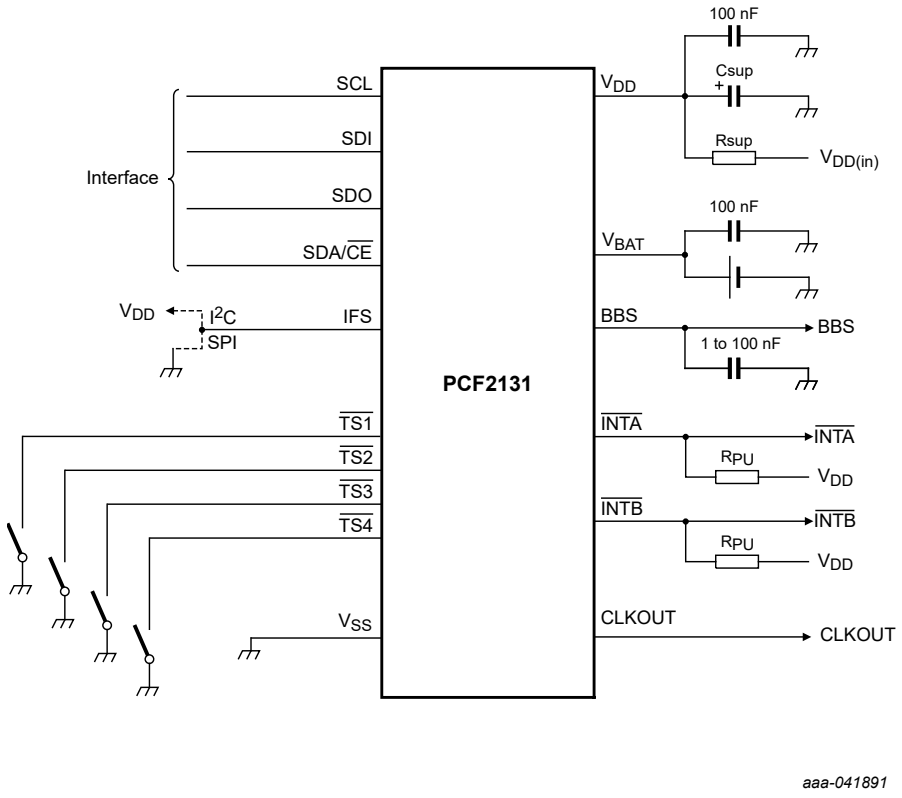
Figure 39. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11 Application information

Figure 40 shows the application diagram of PCF2131.



R_{PU}: 10 kΩ is recommended.

R_{SUP} and C_{SUP}: An appropriate RC filter must be added to guarantee the chip only sees <0.35 V/ms ramp down rate on supply, even if Vdd_in ramp rate is high.

Figure 40. General application diagram

12 Quality information

UL Component Recognition

This (component or material) is Recognized by UL. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13 Package outline

This section shows the package outline for the PCF2131.

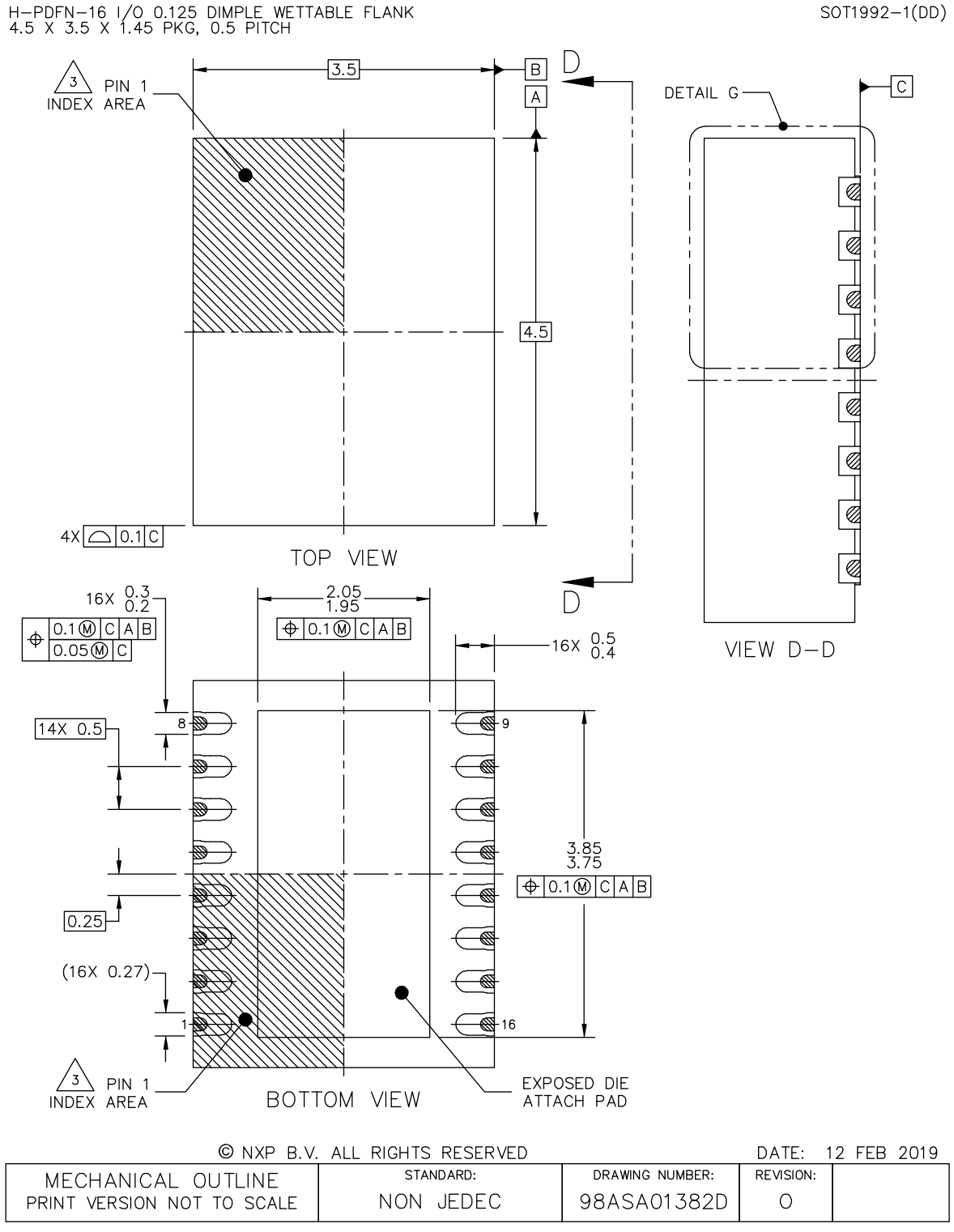
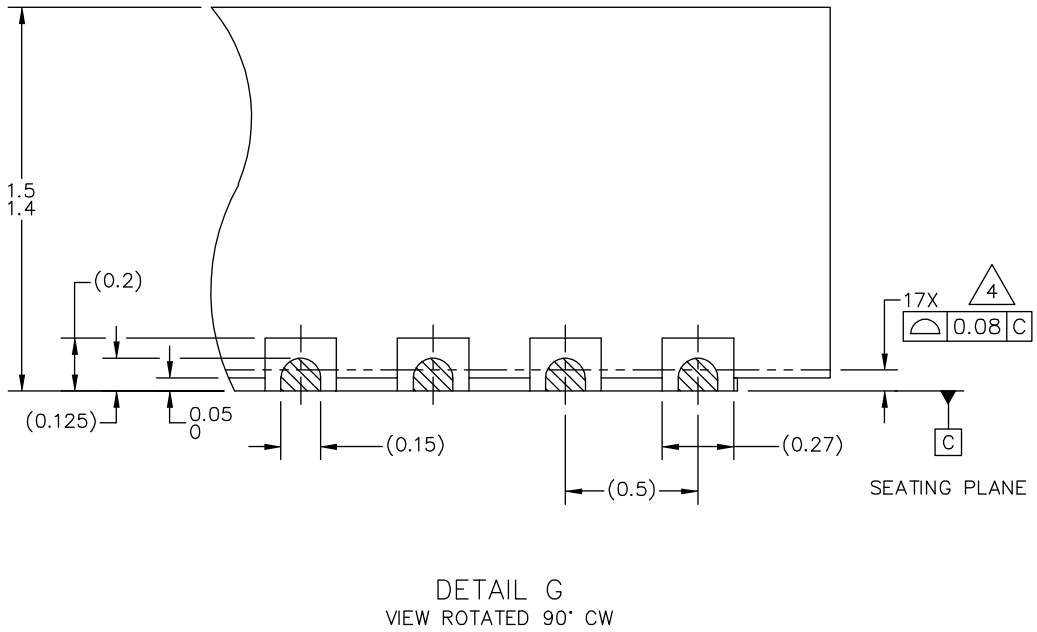


Figure 41. Package outline SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



© NXP B.V. ALL RIGHTS RESERVED

DATE: 12 FEB 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01382D	REVISION: O	

Figure 42. Package outline SOT1992-1 (HLSON16); detail G

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

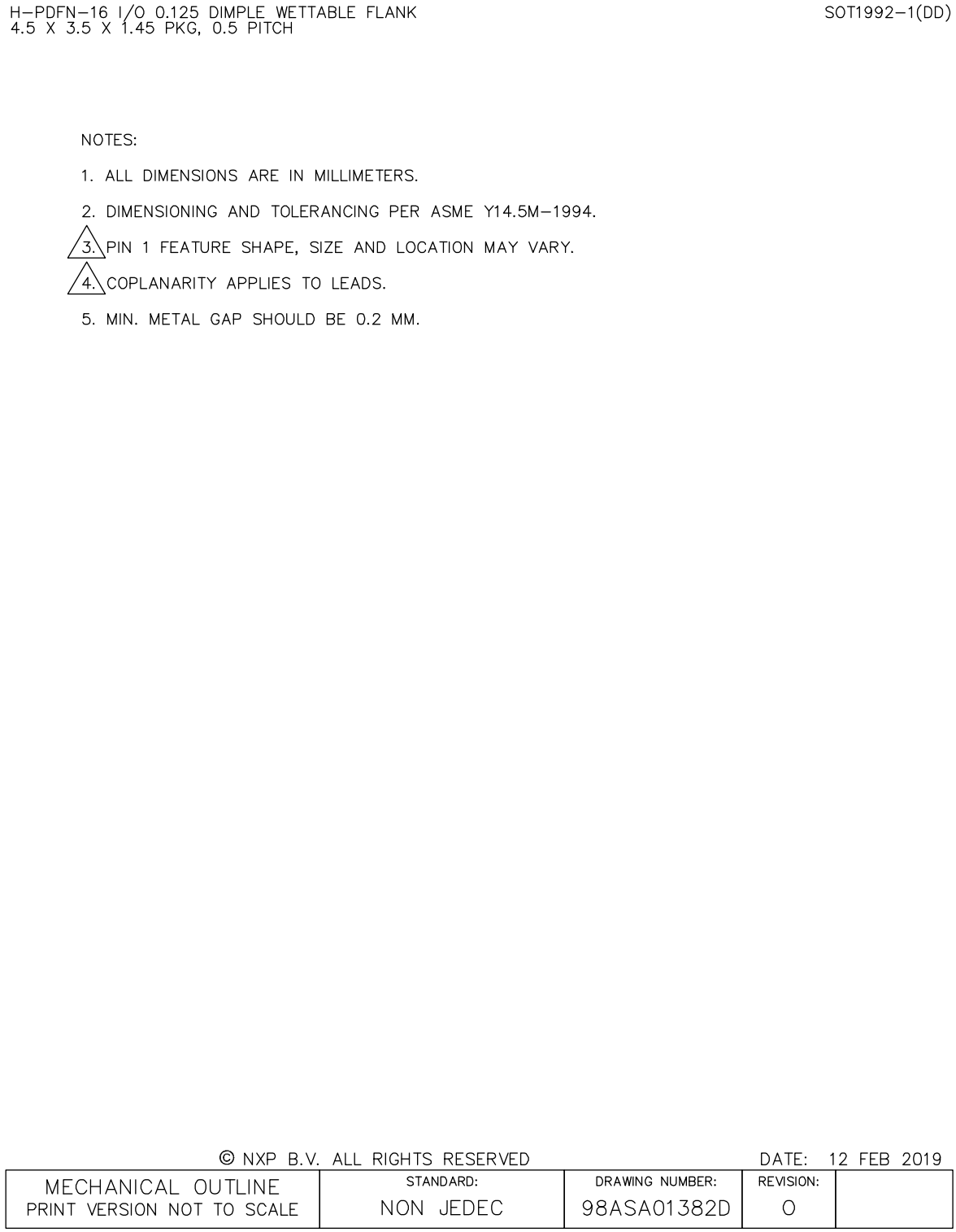


Figure 43. Package outline SOT1992-1 (HLSON16); notes

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14 Packing information

This section provides tape and reel information for the PCF2131.

14.1 Tape and reel information

For tape and reel packing information, see ref.[2].

15 Soldering

For information about soldering, see ref.[1].

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

15.1 Footprint information

This section shows the footprint information for the PCF2131.

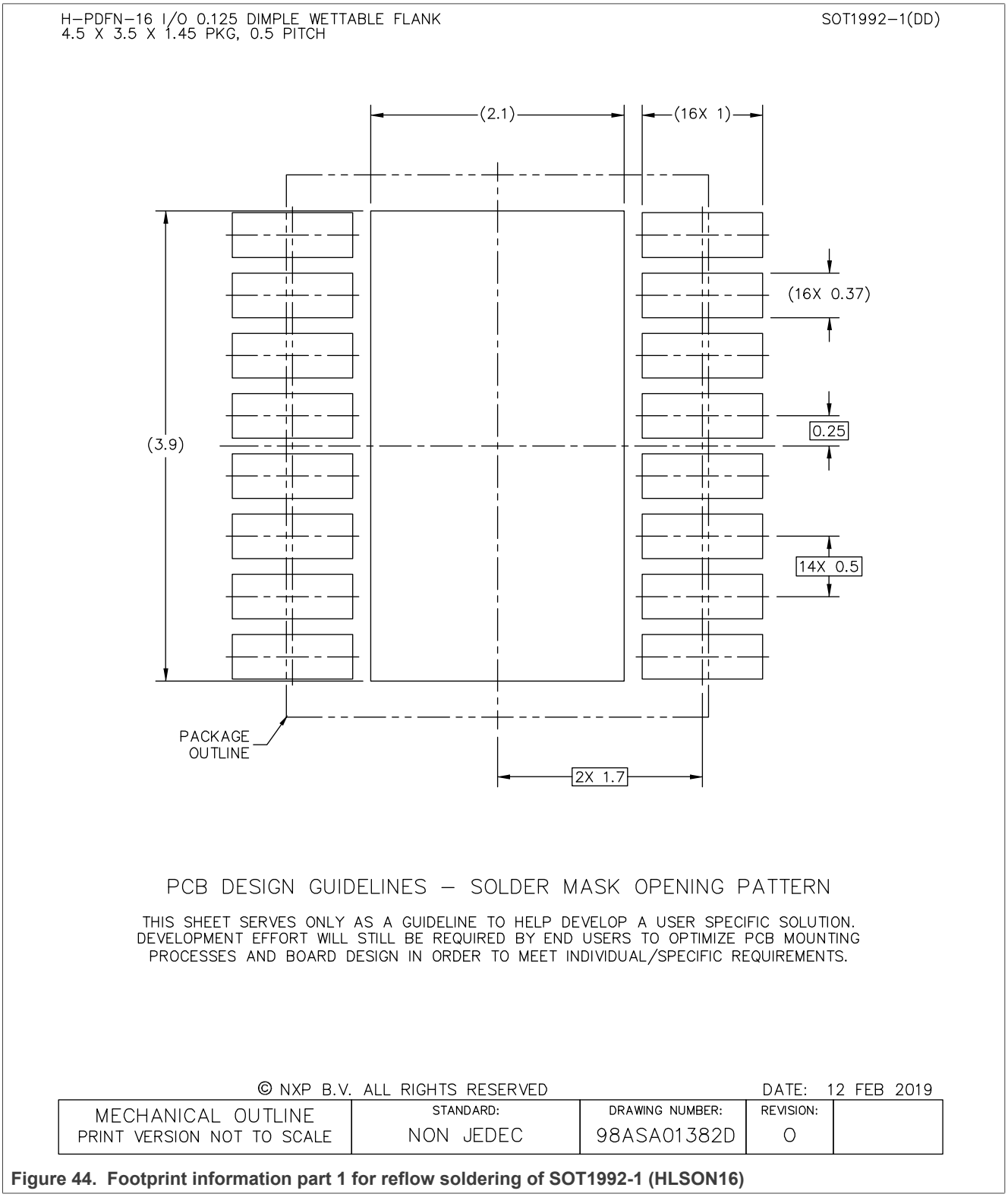


Figure 44. Footprint information part 1 for reflow soldering of SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

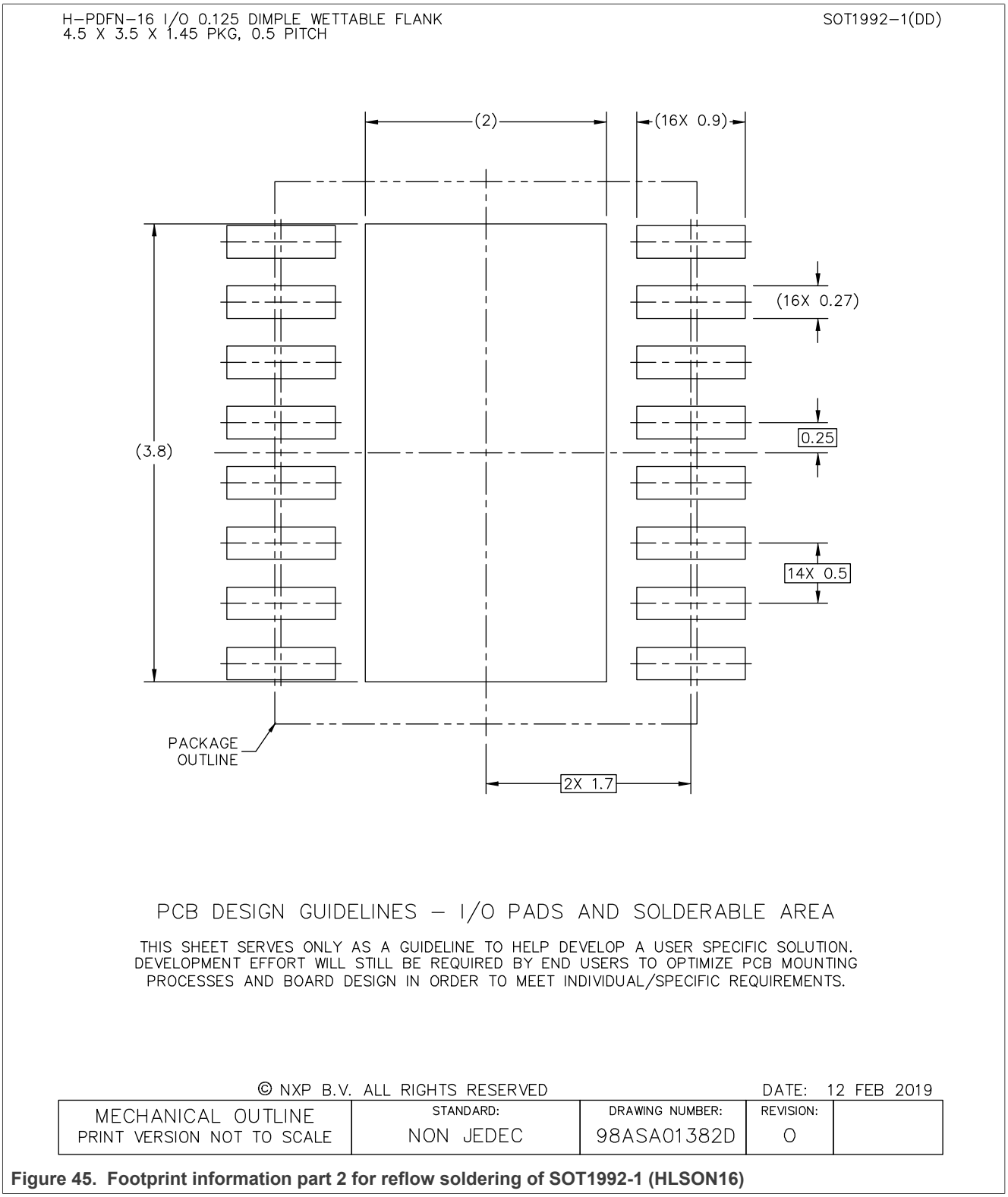


Figure 45. Footprint information part 2 for reflow soldering of SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

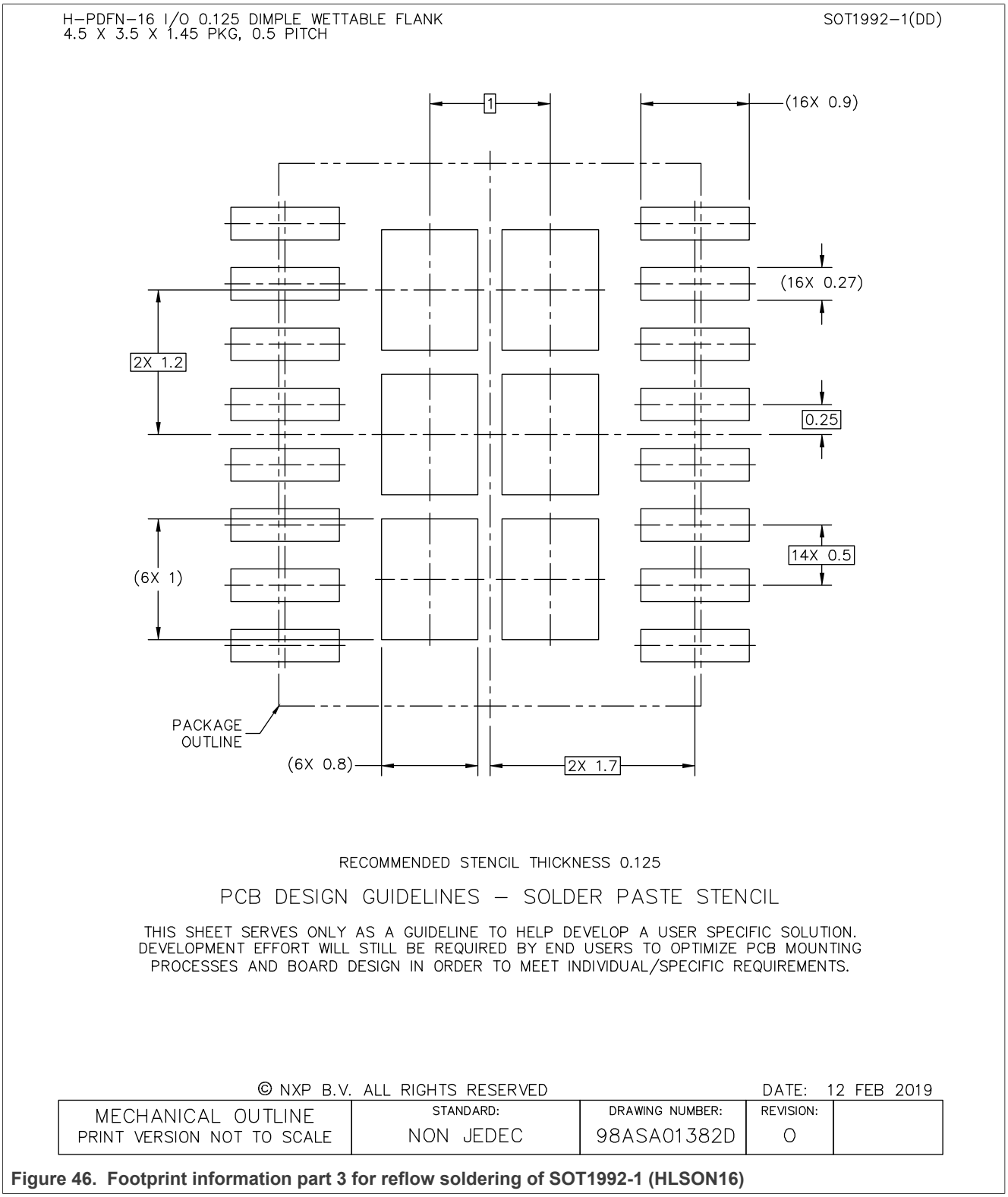


Figure 46. Footprint information part 3 for reflow soldering of SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

16 Acronyms

This section lists the acronyms used in this document.

Table 93. Acronyms

Acronym	Description
AEC	Automotive Electronics Council
AF	Alarm Flag
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged Device Model
CE	Chip Enable
CMOS	Complementary Metal-Oxide Semiconductor
COF	CLKOUT Frequency
CPR	Clear Prescaler
CTS	Clear Timestamp
DC	Direct Current
EPROM	Erasable Programmable Read-Only Memory
GPS	Global Positioning System
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MI	Minute Interrupt
MM	Machine Model
MSB	Most Significant Bit
OSF	Oscillator Stop Flag
OTP	One Time Programmable
PM	Post Meridiem
POR	Power-on Reset
PPM	Parts per Million
RC	Resistance-Capacitance
RTC	Real-Time Clock
SCL	Serial Clock Line
SDA	Serial Data Line
SDO	Serial Data Output
SI	Second Interrupt
SPI	Serial Peripheral Interface

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 93. Acronyms...*continued*

Acronym	Description
SR	Software Reset
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Xtal Oscillator
Xtal	Crystal

17 References

This section lists the references used to supplement this document.

[1] AN13203 Application and soldering information for the PCF2131 and PCA2131 RTC
[2] SOT1992-1_518 HLSON16; Reel pack; SMD, 13", packing information
[3] UM10204 I^2C-bus specification and user manual
[4] UM10569 Store and transport requirements

18 Revision history

This section summarizes revisions to this document.

Table 94. Revision history

Document ID	Release date	Description
PCF2131 v.2.5	26 June 2026	Updated as per CIN# 202606036I: • Updated supply current values in Table 89 • Minor editorial changes
PCF2131 v.2.4	23 December 2025	Updated as per CIN# 202506018I: • Added: Section 12 "Quality information" • Minor editorial changes
PCF2131 v.2.3	16 October 2025	Updated the following figure as per CIN# 202509004I: • Changed the Y-axis label from I_{DD} to I_{OL} of Figure 34 • Minor editorial changes
PCF2131 v.2.2	20 June 2025	• Updated the following sections as per CIN# 202506018I: – Section 2 "Features and benefits" – Section 7.2.1 – Table 8 "Control_2 - control and status register 2 (address 01h) bit description" – Section 7.7 "Power-on Reset (POR) function " – Section 7.8.1 "Software Reset (SR)" – Section 7.14 "Stop bit function" – Section 10.2 "I2C-bus timing characteristics" – Section 16 "Acronyms" • Deleted the following sections: – Power-On Reset Override (PORO) – External clock test mode • Updated the following figure: – Figure 37 "Temperature compensation comparison" • Made some editorial changes
PCF2131 v.2.1	27 January 2025	Updated per CIN 202411003I:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 94. Revision history...*continued*

Document ID	Release date	Description
		• Table 3: Updated exposed pad recommendation
PCF2131 v.2.0	5 October 2023	• Table 4: 05h - corrected values for bits 6 to 1 • Table 25: Corrected duplicate header bit 6 to bit 7 • Table 92: $t_{VD;DAT}$ unit corrected to µs • Table 95: PCF2127 and PCA/F2129 are NRND and removed from the selection table; PCA2131 corrected to Grade 2 that is 105 °C
PCF2131 v.1.1	15 October 2021	Product data sheet
PCF2131 v.1.0	28 May 2021	Product data sheet

19 Appendix

This section describes the RTC selection.

19.1 RTC selection

Table 95. Selection of RTCs

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD} typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF8563	X	1	I^2C	250	-	-	-	-	SO8, TSSOP8, HVSON10
PCF8564A	X	1	I^2C	250	-	-	-	Integrated oscillator caps	WLCSP
PCA8565	X	1	I^2C	600	-	-	Segment B, grade 1	High robustness, T_{amb}= -40 °C to 125 °C	TSSOP8, HVSON10
PCA8565A	X	1	I^2C	600	-	-	-	Integrated oscillator caps, T_{amb}= -40 °C to 125 °C	WLCSP
PCF85063	-	1	I^2C	220	-	-	-	Basic functions only, no alarm	HXSON8
PCF85063A	X	1	I^2C	220	-	-	-	Tiny package	SO8, DFN2626-10, TSSOP8
PCF85063B	X	1	SPI	220	-	-	-	Tiny package	DFN2626-10
PCA85073A	X	1	I^2C	220	-	-	Segment B, grade 2	Tiny package	TSSOP8
PCF85263A	X	2	I^2C	230	X	1	-	Timestamp, battery backup, stopwatch $^1/_{100}$ s	SO8, TSSOP10, WLCSP12, TSSOP8, DFN2626-10
PCF85363A	X	2	I^2C	230	X	1	-	Timestamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10, TSSOP8
PCF8523	X	2	I^2C	150	X	-	-	Lowest power 150 nA in operation, FM+ 1 MHz	SO8, HVSON8, TSSOP14, WLCSP
PCF2123	X	1	SPI	100	-	-	-	Lowest power 100 nA in operation	TSSOP14, HVQFN16, WLCSP12
PCA21125	X	1	SPI	820	-	-	Segment B, grade 1	High robustness, T_{amb}= -40 °C to 125 °C	TSSOP14
PCF2131	X	2	I^2C and SPI	60	X	4	-	Temperature compensated, quartz built in, calibrated	HLSON16 with wettable flanks
PCA2131	X	2	I^2C and SPI	106	X	4	Segment B, grade 2	Temperature compensated, quartz built in, calibrated T_{amb}= -40 °C to 105 °C	HLSON16 with wettable flanks

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tables

Tab. 1. Ordering information 2
Tab. 2. Ordering options 2
Tab. 3. Pin description 4
Tab. 4. Register overview 6
Tab. 5. Control_1 - control and status register 1 (address 00h) bit allocation 8
Tab. 6. Control_1 - control and status register 1 (address 00h) bit description 8
Tab. 7. Control_2 - control and status register 2 (address 01h) bit allocation 9
Tab. 8. Control_2 - control and status register 2 (address 01h) bit description 9
Tab. 9. Control_3 - control and status register 3 (address 02h) bit allocation 9
Tab. 10. Control_3 - control and status register 3 (address 02h) bit description 10
Tab. 11. Control_4 - control and status register 4 (address 03h) bit allocation 10
Tab. 12. Control_4 - control and status register 4 (address 03h) bit description 10
Tab. 13. Control_5 - control and status register 5 (address 04h) bit allocation 11
Tab. 14. Control_5 - control and status register 5 (address 04h) bit description 11
Tab. 15. CLKOUT_ctl - CLKOUT control register (address 13h) bit allocation 11
Tab. 16. CLKOUT_ctl - CLKOUT control register (address 13h) bit description 12
Tab. 17. Temperature measurement period 13
Tab. 18. CLKOUT frequency selection 13
Tab. 19. Aging_offset - crystal aging offset register (address 30h) bit allocation 14
Tab. 20. Aging_offset - crystal aging offset register (address 30h) bit description 14
Tab. 21. Frequency correction at 25 °C, typical 14
Tab. 22. Power management control bit description 15
Tab. 23. Output pin BBS 19
Tab. 24. Reset - software reset control (address 05h) bit description 21
Tab. 25. 100th Seconds - 100th seconds (address 06h) bit allocation 23
Tab. 26. 100th Seconds - 100th seconds register (address 06h) bit description 23
Tab. 27. 100th Seconds coded in BCD format 23
Tab. 28. Seconds - seconds and clock integrity register (address 07h) bit allocation 23
Tab. 29. Seconds - seconds and clock integrity register (address 07h) bit description 24
Tab. 30. Seconds coded in BCD format 24
Tab. 31. Minutes - minutes register (address 08h) bit allocation 24
Tab. 32. Minutes - minutes register (address 08h) bit description 24
Tab. 33. Hours - hours register (address 09h) bit allocation 25
Tab. 34. Hours - hours register (address 09h) bit description 25
Tab. 35. Days - days register (address 0Ah) bit allocation 25
Tab. 36. Days - days register (address 0Ah) bit description 25
Tab. 37. Weekdays - weekdays register (address 0Bh) bit allocation 26
Tab. 38. Weekdays - weekdays register (address 0Bh) bit description 26
Tab. 39. Weekday assignments 26
Tab. 40. Months - months register (address 0Ch) bit allocation 27
Tab. 41. Months - months register (address 0Ch) bit description 27
Tab. 42. Month assignments in BCD format 27
Tab. 43. Years - years register (address 0Dh) bit allocation 27
Tab. 44. Years - years register (address 0Dh) bit description 28
Tab. 45. Second_alarm - second alarm register (address 0Eh) bit allocation 30
Tab. 46. Second_alarm - second alarm register (address 0Eh) bit description 30
Tab. 47. Minute_alarm - minute alarm register (address 0Fh) bit allocation 31
Tab. 48. Minute_alarm - minute alarm register (address 0Fh) bit description 31
Tab. 49. Hour_alarm - hour alarm register (address 10h) bit allocation 31
Tab. 50. Hour_alarm - hour alarm register (address 10h) bit description 31
Tab. 51. Day_alarm - day alarm register (address 11h) bit allocation 32
Tab. 52. Day_alarm - day alarm register (address 11h) bit description 32
Tab. 53. Weekday_alarm - weekday alarm register (address 12h) bit allocation 32
Tab. 54. Weekday_alarm - weekday alarm register (address 12h) bit description 33
Tab. 55. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit allocation 33
Tab. 56. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit description 34
Tab. 57. Watchdg_tim_val - watchdog timer value register (address 36h) bit allocation 34
Tab. 58. Watchdg_tim_val - watchdog timer value register (address 36h) bit description 34
Tab. 59. Programmable watchdog timer 34
Tab. 60. Flag location in register Control_2 36
Tab. 61. Example values in register Control_2 36
Tab. 62. Example to clear only AF (bit 4) 37
Tab. 63. Example to clear only MSF (bit 7) 37
Tab. 64. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit allocation 38

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tab. 65. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit description 38
Tab. 66. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit allocation 38
Tab. 67. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit description 39
Tab. 68. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit allocation 39
Tab. 69. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit description 39
Tab. 70. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit allocation 39
Tab. 71. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit description 40
Tab. 72. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit allocation 40
Tab. 73. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit description 40
Tab. 74. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit allocation 40
Tab. 75. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit description 41
Tab. 76. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit allocation 41
Tab. 77. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit description 41
Tab. 78. Battery switch-over and timestamp 41
Tab. 79. Effect of bits MI and SI on pin INTA/B and bit MSF 43
Tab. 80. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit allocation 45
Tab. 81. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit description 46
Tab. 82. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit allocation 46
Tab. 83. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit description 46
Tab. 84. Interface selection input pin IFS 47
Tab. 85. Serial interface 48
Tab. 86. Command byte definition 49
Tab. 87. I2C target address byte 52
Tab. 88. Limiting values 54
Tab. 89. Static characteristics 55
Tab. 90. Frequency characteristics 59
Tab. 91. SPI-bus characteristics 61
Tab. 92. I2C-bus characteristics 62
Tab. 93. Acronyms 73
Tab. 94. Revision history 74
Tab. 95. Selection of RTCs 75

Figures

Fig. 1. Block diagram of PCF2131 3
Fig. 2. Pin configuration for PCF2131 (transparent top view) 4
Fig. 3. Handling address registers 5
Fig. 4. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled) 17
Fig. 5. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled) 18
Fig. 6. Battery switch-over circuit, simplified block diagram 18
Fig. 7. Battery low detection behavior with bit BLIE set logic 1 (enabled) 19
Fig. 8. Power failure event due to battery discharge: reset occurs 20
Fig. 9. Dependency between POR and oscillator 21
Fig. 10. Software reset command 22
Fig. 11. Data flow for the time function 28
Fig. 12. Alarm function block diagram 30
Fig. 13. Alarm flag timing diagram 33
Fig. 14. WD_CD set logic 1: watchdog activates an interrupt when timed out 36
Fig. 15. Interrupt block diagram 42
Fig. 16. INTA/B example for SI and MI when TI_TP is logic 1 43
Fig. 17. INTA/B example for SI and MI when TI_TP is logic 0 44
Fig. 18. Example of shortening the INTA/B pulse by clearing the MSF flag 44
Fig. 19. AF timing diagram 45
Fig. 20. CPR and stop bit functional diagram 47
Fig. 21. STOP release timing 47
Fig. 22. Interface selection 48
Fig. 23. SDI, SDO configurations 48
Fig. 24. Data transfer overview 49
Fig. 25. SPI-bus write example 49
Fig. 26. SPI-bus read example 50
Fig. 27. Bit transfer 50
Fig. 28. Definition of START and STOP conditions 51
Fig. 29. System configuration 51
Fig. 30. Acknowledgment on the I2C-bus 52
Fig. 31. Bus protocol, writing to registers 52
Fig. 32. Bus protocol, reading from registers 53
Fig. 33. Device diode protection diagram of PCF2131 53
Fig. 34. IOL on pin SDA/CE 57

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Fig. 35. IDD as a function of temperature 58
Fig. 36. IDD as a function of VDD 59
Fig. 37. Temperature compensation comparison 60
Fig. 38. SPI-bus timing 62
Fig. 39. I2C-bus timing diagram; rise and fall times refer to 30 % and 70 % 64
Fig. 40. General application diagram 65
Fig. 41. Package outline SOT1992-1 (HLSON16) 66
Fig. 42. Package outline SOT1992-1 (HLSON16); detail G 67
Fig. 43. Package outline SOT1992-1 (HLSON16); notes 68
Fig. 44. Footprint information part 1 for reflow soldering of SOT1992-1 (HLSON16) 70
Fig. 45. Footprint information part 2 for reflow soldering of SOT1992-1 (HLSON16) 71
Fig. 46. Footprint information part 3 for reflow soldering of SOT1992-1 (HLSON16) 72

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
4.1 Ordering options 2
5 Block diagram 2
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 5
7.1 Register overview 5
7.2 Control registers 8
7.2.1 Register Control_1 8
7.2.2 Register Control_2 8
7.2.3 Register Control_3 9
7.2.4 Register Control_4 10
7.2.5 Register Control_5 11
7.3 Register CLKOUT_ctl 11
7.3.1 Temperature compensated RTC 12
7.3.1.1 Temperature measurement 13
7.3.2 OTP refresh 13
7.3.3 Clock output 13
7.4 Register Aging_offset 14
7.4.1 Crystal aging correction 14
7.5 Power management functions 15
7.5.1 Battery switch-over function 16
7.5.1.1 Standard mode 16
7.5.1.2 Direct switching mode 17
7.5.1.3 Battery switch-over disabled: only one power supply (VDD) 18
7.5.1.4 Battery switch-over architecture 18
7.5.2 Battery low detection function 18
7.5.3 Battery backup supply 19
7.6 Oscillator stop detection function 20
7.7 Power-on Reset (POR) function 20
7.7.1 Power-on Reset (POR) 20
7.8 Software reset register 21
7.8.1 Software Reset (SR) 22
7.8.2 Clear Prescaler (CPR) 22
7.8.3 Clear timestamp (CTS) 22
7.9 Time and date function 22
7.9.1 Register 100th Seconds 23
7.9.2 Register Seconds 23
7.9.3 Register Minutes 24
7.9.4 Register Hours 25
7.9.5 Register Days 25
7.9.6 Register Weekdays 26
7.9.7 Register Months 26
7.9.8 Register Years 27
7.9.9 Setting and reading the time 28
7.10 Alarm function 29
7.10.1 Register Second_alarm 30
7.10.2 Register Minute_alarm 31
7.10.3 Register Hour_alarm 31
7.10.4 Register Day_alarm 32
7.10.5 Register Weekday_alarm 32
7.10.6 Alarm Flag (AF) 33
7.11 Watchdog timer functions 33
7.11.1 Register Watchdg_tim_ctl 33
7.11.2 Register Watchdg_tim_val 34
7.11.3 Watchdog timer function 35
7.11.4 Predefined timers: second and minute interrupts 36
7.11.5 Clearing flags 36
7.12 Timestamp function 37
7.12.1 Timestamp flag 37
7.12.2 Timestamp mode 37
7.12.3 Timestamp registers 38
7.12.3.1 Register Timestp_ctl1/2/3/4 38
7.12.3.2 Register Sec_timestp 38
7.12.3.3 Register Min_timestp 39
7.12.3.4 Register Hour_timestp 39
7.12.3.5 Register Day_timestp 40
7.12.3.6 Register Mon_timestp 40
7.12.3.7 Register Year_timestp 41
7.12.4 Dependency between Battery switch-over and timestamp 41
7.13 Interrupt output, INTA/INTB 41
7.13.1 Minute and second interrupts 42
7.13.2 INTA/B pulse shortening 44
7.13.3 Watchdog timer interrupts 44
7.13.4 Alarm interrupts 45
7.13.5 Timestamp interrupts 45
7.13.6 Battery switch-over interrupts 45
7.13.7 Battery low detection interrupts 45
7.13.8 Interrupt masks 45
7.14 Stop bit function 46
7.15 Interfaces 47
7.15.1 SPI-bus interface 48
7.15.1.1 Data transmission 49
7.15.2 I2C-bus interface 50
7.15.2.1 Bit transfer 50
7.15.2.2 START and STOP conditions 50
7.15.2.3 System configuration 51
7.15.2.4 Acknowledge 51
7.15.2.5 I2C-bus protocol 52
7.15.3 Bus communication and battery backup operation 53
7.16 Internal circuitry 53
7.17 Safety notes 54
8 Limiting values 54
9 Static characteristics 55
9.1 Current consumption characteristics, typical 57
9.2 Frequency characteristics 59
10 Dynamic characteristics 61
10.1 SPI-bus timing characteristics 61
10.2 I2C-bus timing characteristics 62
11 Application information 65
12 Quality information 65
13 Package outline 66
14 Packing information 69
14.1 Tape and reel information 69

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

15 Soldering 69
15.1 Footprint information 70
16 Acronyms 73
17 References 74
18 Revision history 74
19 Appendix 75
19.1 RTC selection 75
Legal information 76

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. **All rights reserved.**