ATDH1150USB

ATF15xx CPLD JTAG ISP Download Cable

USER GUIDE

Introduction

The Atmel® ATF15xx Complex Programmable Logic Device (CPLD) USB-based JTAG ISP Download Cable [Atmel PN: ATDH1150USB] connects to a standard USB port on a host computer on one side and to a JTAG header of a programming circuit board on the other side. It transfers the JTAG instructions and data generated by the ATMISP software running on the host PC to the Atmel ATF15xx series CPLDs on the programming circuit board. The ATMISP software can be downloaded from the Atmel website at http://www.atmel.com/tools/ATMISP.aspx. With this In-System Programming (ISP) download cable and the ATMISP software, design changes can easily be downloaded directly to the ATF15xx JTAG devices, resulting in easy prototyping of designs.

The ATDH1150USB cables are made by two vendors and have identical circuit design. The cables labeled with “ATDH1150USB-K” are built by Kanda (www.kanda.com) and can also be purchased directly from Kanda. When purchasing this cable from Atmel or an Atmel distributor, the Atmel ordering code is “ATDH1150USB”.

Features

- Supports Industry Standard IEEE 1149.1 (JTAG) Compliant Devices
- Allows Users to Perform JTAG ISP of Atmel ATF15xx CPLDs
- Supports Target Systems Using 5.0V, 3.3V, 2.5V, or 1.8V V_{CC} and I/O Standards
- Supported by the ATMISP Software (Version 6.6, 6.7, and 7.x)
- Interfaces with a Standard USB 2.0/3.0 Port on a PC
- Supports 10-pin and 14-pin JTAG Interface Headers (JTAG-A and JTAG-X)

Supports

The ATDH1150USB ISP Download Cable supports all ATF15xx CPLDs with the JTAG feature enabled. By default, the ATF15xx CPLDs are shipped with the non-volatile memory in the erased state, which would enable the JTAG feature. Once the JTAG feature of an ATF15xx is disabled by programming it with a JEDEC file that disables the JTAG feature, its memory contents can no longer be accessed via the JTAG port. To re-enable the JTAG feature, the ATF15xx CPLD will need to be erased on a stand-alone device programmer.

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Functional Description

The ATDH1150USB ISP Download Cable connects to the PC host's USB port on one side using the USB cable provided to communicate with ATMISP. On the other end, the cable is connected to a 10-pin or 14-pin JTAG header on the programming circuit board using the 10-wire ribbon cable provided or a 14-wire ribbon cable (not included) to communicate with the target JTAG devices. Users can choose to use either one of the two JTAG connectors (JTAG-A and JTAG-X) available on the ATDH1150USB based on their requirements; however, these two JTAG connectors should not be used at the same time.

The second 10-pin header labeled ***TWI*** on the ATDH1150USB is *not* supported and should *not* be used.

A functional block diagram of the ATDH1150USB ISP Download Cable is shown in the below figure, and Table 1 and Table 2 provide the pin assignments and signal descriptions for the two JTAG connectors.

Figure 1. ATDH1150USB ISP Download Cable Functional Block Diagram

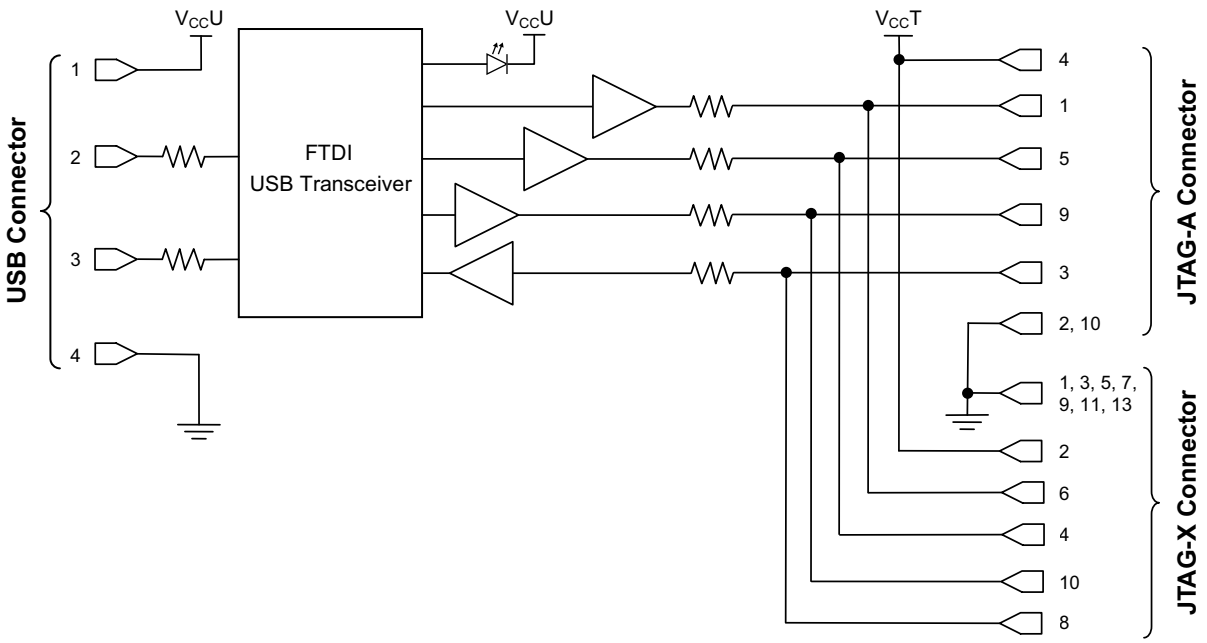


Table 1. 10-pin JTAG-A Connector Signal Description

Pin	Signal Name	Description
1	TCK	JTAG Clock Signal
2	GND	Ground from Target System
3	TDO	JTAG Data Output Signal
4	$V_{CC}T$	Power Supply from Target System
5	TMS	JTAG State Machine Control Signal
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	TDI	JTAG Data Input Signal
10	GND	Ground from Target System

Table 2. 14-pin JTAG-X Connector Signal Description

Pin	Signal Name	Description
1	GND	Ground from Target System
2	$V_{CC}T$	Power Supply from Target System
3	GND	Ground from Target System
4	TMS	JTAG State Machine Control Signal
5	GND	Ground from Target System
6	TCK	JTAG Clock Signal
7	GND	Ground from Target System
8	TDO	JTAG Data Output Signal
9	GND	Ground from Target System
10	TDI	JTAG Data Input Signal
11	GND	Ground from Target System
12	NC	No Connect
13	GND	Ground from Target System
14	NC	No Connect



The ISP circuit board must supply V_{CC} and GND to the ATDH1150USB ISP Download Cable through the 10-pin or 14-pin JTAG header via the $V_{CC}T$ and GND pins. A regulated V_{CC} voltage between 1.65V to 5.5V is required, and it should be the same V_{CC} supply used by the JTAG devices.

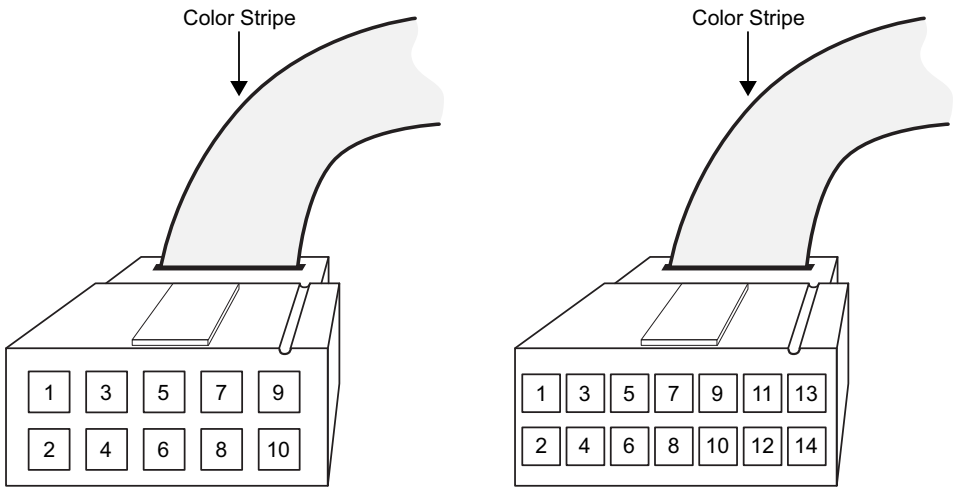
The multi-color status LED on the ATDH1150USB ISP Download Cable displays the status of the JTAG communication and operation:

- Green = Successful JTAG communication and operation.
- Red = Unsuccessful JTAG communication and/or operation.
- Amber = JTAG operation is in progress.

The programming circuit board must provide a regulated V_{CC} to the ATDH1150USB ISP Download Cable via the V_{CC}T pin of the 10-pin or 14-pin JTAG header. The ATDH1150USB ISP Download Cable V_{CC}T must be between 1.65V and 5.5V at 150mA (max) of current, and it powers the output buffers for the JTAG signals. The host PC's USB port must also supply a V_{CC} (V_{BUS}) which is in compliance with the USB 2.0/3.0 specification to the ATDH1150USB ISP Download Cable via Pin 1 of the USB connector. Furthermore, a stable GND from the programming circuit board and USB port must also be provided to the ATDH1150USB ISP Download Cable.

The color stripe on the ribbon cable of the ATDH1150USB ISP Download Cable indicates the orientation of
Pin 1 of the JTAG female connector. The color stripe or a polarized header can be used as a guide to assure the female connector is properly oriented when it is attached to the programming circuit board. The below figure illustrates the pinouts of the 10-pin and 14-pin female connectors on the ATDH1150USB ISP Download Cable. The pinout of the JTAG male header on the programming circuit board must match one of the pinouts shown.

Figure 2. ATDH1150USB ISP Download Cable 10-pin and 14-pin Female Connector Pinouts



10-pin Male Header

Figure 3 illustrates the dimensions of the 10-pin JTAG male header to be mounted on the programming circuit board if the 10-pin JTAG female connector is to be used, and Figure 4 illustrates the pin assignments for this 10-pin male header.

Figure 3. 10-pin Dimensions

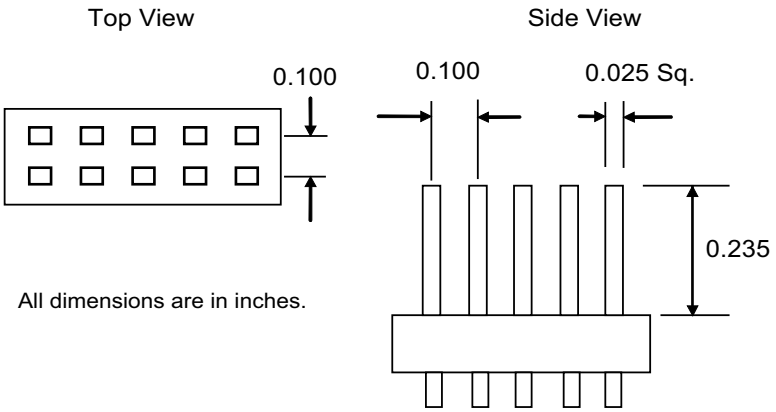
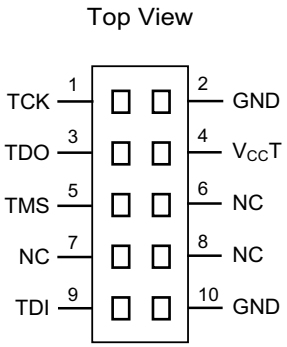


Figure 4. 10-pin Pinouts



14-pin Male Header

Figure 5 illustrates the dimensions for the 14-pin JTAG male header to be mounted on the programming circuit board if the 14-pin JTAG female connector is to be used, and Figure 6 illustrates the pin assignments for this 14-pin male header.

Figure 5. 14-pin Dimensions

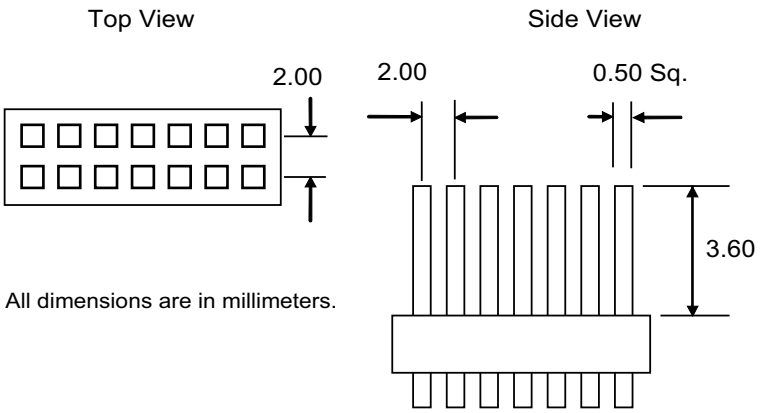
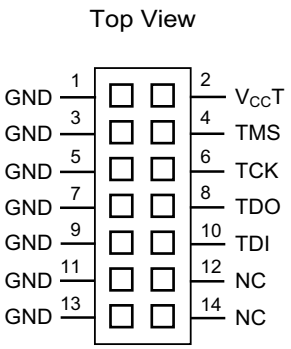


Figure 6. 14-pin Pinouts



Ordering Information

The ATF15xx CPLD USB-based JTAG ISP Download Cable can be purchased from authorized Atmel distributors.

Table 3. Atmel ATF15xx CPLD USB-based JTAG ISP Download Cable

Part Number	Description
ATDH1150USB	Atmel ATF15xx CPLD USB-based JTAG ISP Download Cable

Frequently Asked Questions

For a multiple device JTAG hardware chain, which device is considered the first device (Device #1) when setting up the Atmel CPLD ISP (ATMISP) software?

The device with its TDI pin connected to the TDI pin of the JTAG header is the first device (Device #1) of a JTAG chain. The device with its TDO pin connected to the TDO pin of the JTAG header is the last device of the chain.

For devices with different V_{CC}INT and V_{CC}IO supplies, which V_{CC} (V_{CC}IO or V_{CC}INT) should be used to supply the ATDH1150USB ISP Download Cable's V_{CC}T?

V_{CC}IO should be used to supply the V_{CC}T of the ATDH1150USB ISP Download Cable.

Can a JEDEC file with the JTAG port feature disabled be programmed into the ATF15xx through JTAG ISP?

Since all ATF15xx devices are shipped in a blank (erased) state, the JTAG port is enabled by default. Therefore, they can be programmed with a JEDEC file with the JTAG port feature disabled ONLY ONCE via JTAG ISP. However, this is not recommended since the pins used for the JTAG port of the ATF15xx devices can become outputs immediately after programming is completed and they can content with the output drivers in the ATDH1150USB ISP Download Cable. Furthermore, please note that once the JTAG port is disabled, the device can no longer be accessed through the JTAG port. To re-enable the JTAG port, you must erase the device or re-program the device with a JEDEC file with the JTAG port feature enabled using a stand-alone 3rd-party device programmer from vendors such as BPM Microsystems, Data I/O, Hi-Lo Systems,. etc.

Technical Support

For Atmel PLD technical support, please contact the Atmel PLD Applications Group at:

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Email: pld@atmel.com

Online: http://www.atmel.com/design-support/

Revision History

Doc. Rev.	Date	Comments
8909B	07/2015	Added ATDH1150USB and JTAG clarification. Updated from USB 2.0 to 2.0/3.0 Port, 14-wire ribbon cable to not included, regulated V_{CC} from recommended to required, and online support website.
8909A	04/2014	Initial document release.

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